

tb_cocotb.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

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tb_cocotb

```
module tb_cocotb #(
  parameter
  CLOCK_SPEED
  =
  20000000,
  parameter
  SAMPLE_RATE
  =
  2000000,
  parameter
  BIT_SLICE_OFFSET
  =
  0,
  parameter
```

```

INVERT_DATA
=
0,
parameter
SAMPLE_SELECT
=
0
) ( input aclk, input arstn, output [15:0] m_axis_tdata, output m_axis_tvalid

```

This core is a MIL-STD-1553 to AXI streaming decoder. It uses the positive edge of a clock to sample data. This restricts the core to 2 Mhz and above for a sample clock.

Parameters

CLOCK_SPEED parameter	This is the aclk frequency in Hz, must be 2 MHz or above.
SAMPLE_RATE parameter	2 MHz or above rate that is an even divisor of CLOCK_SPEED
BIT_SLICE_OFFSET parameter	Changes the bit that is selected for data reduction.
INVERT_DATA parameter	Will invert all decoded data.
SAMPLE_SELECT parameter	Changes the bit that is sampled for data capture.

Ports

aclk	Clock for all logic
arstn	Negative reset
m_axis_tdata	Output data for 1553 decoder.
m_axis_tvalid	When active high the output data is valid.
m_axis_tuser	Information about the AXIS data {TYY,NA,D,I,P} Bits explained below:

```

- TYY = TYPE OF DATA
  - 000 NA
  - 001 REG (NOT IMPLIMENTED)
  - 010 DATA
  - 100 CMD/STATUS
- NA = RESERVED FOR FUTURE USE.
- D = DELAY BEFORE DATA
  - 1 = Delay of 4us or more before data
  - 0 = No delay between data
- I = INVERT
  - 1 = Inverted data
  - 0 = Normal data
- P = PARITY
  - 1 = GOOD
  - 0 = BAD

```

m_axis_tready	When active high the destination device is ready for data.
diff	Output data in TTL differential format.

INSTANTIATED MODULES

dut

```
axis_1553_decoder #(
    CLOCK_SPEED(CLOCK_SPEED),
    SAMPLE_RATE(SAMPLE_RATE),
    BIT_SLICE_OFFSET(BIT_SLICE_OFFSET),
    INVERT_DATA(INVERT_DATA),
    SAMPLE_SELECT(SAMPLE_SELECT)
) dut ( .aclk(aclk), .arstn(arstn), .m_axis_tdata(m_axis_tdata), .m_axis_tva
```

Device under test, axis_1553_decoder