tb_coctb.v

AUTHORS

JAY CONVERTINO

DATES

2025/03/04

INFORMATION

Brief

Test bench wrapper for cocotb

License MIT

tb_cocotb

```verilog
module tb_cocotb #(
parameter
CLOCK_SPEED
  =
20000000,
parameter
SAMPLE_RATE
  =
20000000
) ( input aclk, input arstn, input [15:0] s_axis_tdata, input s_axis_tvalid,
```

This core is a MIL-STD-1553 to AXI streaming decoder. It uses the postive edge of a clock to sample data. This restricts the core to 2 Mhz and above for a sample clock.

Parameters

CLOCK_SPEED   This is the aclk frequency in Hz, must be 2 MHz or above.
parameter

SAMPLE_RATE   2 MHz or above rate that is an even divisor of CLOCK_SPEED
parameter

Ports

aclk   Clock for all logic

arstn   Negative reset

s_axis_tdata   Input data for 1553 encoder.

s_axis_tvalid   When active high the input data is valid.

s_axis_tuser   Information about the AXIS data {TYY,NA,I,P}

    Bits explained below:

```
- TYY = TYPE OF DATA
      - 000 NA
      - 001 REG (NOT IMPLIMENTED)
      - 010 DATA
      - 100 CMD/STATUS
- NA  = RESERVED FOR FUTURE USE.
- D   = DELAY BEFORE DATA
      - 1 = Delay of 4us or more before data
      - 0 = No delay between data
- I   = INVERT
      - 1 = Invert input data before output
      - 0 = No inversion of data before output.
- P   = PARITY
      - 1 = ODD
      - 0 = EVEN
```

s_axis_tready   When active high the device is ready for data.

diff   Output data in TTL differential format.

INSTANTIATED MODULES

dut

```
axis_1553_encoder #(
                                                            .
CLOCK_SPEED(CLOCK_SPEED),
                                                            .
 SAMPLE_RATE(SAMPLE_RATE)
) dut ( .aclk(aclk), .arstn(arstn), .s_axis_tdata(s_axis_tdata), .s_axis_tva
```

Device under test, axis_1553_encoder