

# tb\_axis.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Test bench for axis\_data\_to\_axis\_string using axis stim and clock stim.

### License MIT

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## tb\_axis

---

```
module tb_axis #(
  parameter
  IN_FILE_NAME
  =
  "in.bin",
  parameter
  OUT_FILE_NAME
  =
  "out.bin",
  parameter
  RAND_READY
  =
  0
)
```

---

Test bench for axis\_data\_to\_axis\_string. This will run a file through the system and write its output. These can then be compared to check for errors. If the files are identical, no errors. A FST file will be written.

### Parameters

<b>IN_FILE_NAME</b> parameter	File name for input.
<b>OUT_FILE_NAME</b> parameter	File name for output.
<b>RAND_READY</b> parameter	0 = no random ready. 1 = randomize ready.

## INSTANTIATED MODULES

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### clk\_stim

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```
clk_stimulus #(
    CLOCKS(1),
    CLOCK_BASE(1000000),
    CLOCK_INC(1000),
    RESETS(1),
    RESET_BASE(2000),
    RESET_INC(100)
) clk_stim ( .clkv(tb_dut_clk), .rstnv(tb_dut_rstn), .rstv() )
```

Generate a 50/50 duty cycle set of clocks and reset.

### slave\_axis\_stim

---

```
slave_axis_stimulus #(
    BUS_WIDTH(BUS_WIDTH),
    USER_WIDTH(USER_WIDTH),
    DEST_WIDTH(DEST_WIDTH),
    FILE(IN_FILE_NAME)
) slave_axis_stim ( .m_axis_aclv(tb_dut_clk), .m_axis_arstn(tb_dut_rstn), .m
```

Device under test SLAVE stimulus module.

### dut

---

```
axis_data_to_axis_string #(
    DELIMITER(";",
```

```

TERMINATION("\n"),
SBUS_WIDTH(BUS_WIDTH),
USER_WIDTH(USER_WIDTH),
DEST_WIDTH(DEST_WIDTH),
PREFIX_LEN(1),
DATA_PREFIX("#"),
DEST_PREFIX("&"),
USER_PREFIX("*")
) dut ( .aclk(tb_dut_clk), .arstn(tb_dut_rstn), .m_axis_tdata(tb_dut_data),

```

Device under test, axis\_data\_width\_converter

## master\_axis\_stim

```

master_axis_stimulus #(
BUS_WIDTH(BUS_WIDTH),
USER_WIDTH(USER_WIDTH),
DEST_WIDTH(DEST_WIDTH),
RAND_READY(RAND_READY),
FILE(OUT_FILE_NAME)
) master_axis_stim ( .s_axis_aclk(tb_dut_clk), .s_axis_arstn(tb_dut_rstn),

```

Devie under test MASTER stimulus module.