tb_axis.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench for axis_data_width_converter using axis stim and clock stim.

License MIT

tb_axis

```
module tb_axis #(
parameter
IN_FILE_NAME
 =
in.bin,
parameter
OUT_FILE_NAME
 =
out.bin,
parameter
RAND_READY
 =
0,
parameter
```

```
 SLAVE_WIDTH
  =
 2,
 parameter
 MASTER_WIDTH
  =
 4
)()
```

Test bench for axis_data_width_converter. This will run a file through the system and write its output. These can then be compared to check for errors. If the files are identical, no errors. A FST file will be written.

Parameters

IN_FILE_NAME File name for input.
parameter

OUT_FILE_NAME File name for output.
parameter

RAND_READY 0 = no random ready. 1 = randomize ready.
parameter

SLAVE_WIDTH Width of the slave input bus in bytes
parameter

MASTER_WIDTH Width of the master output bus in bytes
parameter

INSTANTIATED MODULES

clk_stim

```
clk_stimulus #(
                                                                    .
CLOCKS(1),
                                                                    .
CLOCK_BASE(1000000),
                                                                    .
CLOCK_INC(1000),
                                                                    .
RESETS(1),
                                                                    .
RESET_BASE(2000),
                                                                    .
RESET_INC(100)
) clk_stim ( .clkv(tb_dut_clk), .rstnv(tb_dut_rstn), .rstv() )
```

Generate a 50/50 duty cycle set of clocks and reset.

slave_axis_stim

```
slave_axis_stimulus #(
                                                                    .
BUS_WIDTH(SBUS_WIDTH),
                                                                    .
USER_WIDTH(USER_WIDTH),
                                                                    .
DEST_WIDTH(DEST_WIDTH),
                                                                    .
FILE(IN_FILE_NAME)
```

```
) slave_axis_stim ( .m_axis_aclk(tb_dut_clk), .m_axis_arstn(tb_dut_rstn), .m
```

Device under test SLAVE stimulus module.

dut

```
axis_data_width_converter #(
                                                                    .
MASTER_WIDTH(MBUS_WIDTH),
                                                                    .
SLAVE_WIDTH(SBUS_WIDTH)
) dut ( .aclk(tb_dut_clk), .arstn(tb_dut_rstn), .m_axis_tdata(tb_dut_data),
```

Device under test, axis_data_width_converter

master_axis_stim

```
master_axis_stimulus #(
                                                                    .
BUS_WIDTH(MBUS_WIDTH),
                                                                    .
USER_WIDTH(USER_WIDTH),
                                                                    .
DEST_WIDTH(DEST_WIDTH),
                                                                    .
RAND_READY(RAND_READY),
                                                                    .
FILE(OUT_FILE_NAME)
) master_axis_stim ( .s_axis_aclk(tb_dut_clk), .s_axis_arstn(tb_dut_rstn),
```

Devie under test MASTER stimulus module.