tb_cocotb.v

AUTHORS

JAY CONVERTINO

DATES

2024/12/11

INFORMATION

Brief

Test bench wrapper for cocotb

License MIT

tb_cocotb

```
module tb_cocotb #(
parameter
SLAVE_WIDTH
 =
1,
parameter
MASTER_WIDTH
 =
1,
parameter
REVERSE
 =
0
) ( input aclk, input arstn, output [(MASTER_WIDTH*8)-1:0] m_axis_tdata, out
```

Test bench for data width converter. This will run a file through the system and write its output. These can then be compared to check for errors. If the files are identical, no errors. A FST file will be written.

Parameters

SLAVE_WIDTH parameter	Width of the slave input bus in bytes
MASTER_WIDTH parameter	Width of the master output bus in bytes
REVERSE parameter	Change byte order

Ports

aclk	Clock for AXIS
arstn	Negative reset for AXIS
m_axis_tdata	Output data
m_axis_tvalid	When active high the output data is valid
m_axis_tready	When set active high the output device is ready for data.
m_axis_tlast	Indicates last word in stream.
s_axis_tdata	Input data
s_axis_tvalid	When set active high the input data is valid
s_axis_tready	When active high the device is ready for input data.
s_axis_tlast	Is this the last word in the stream (active high).

INSTANTIATED MODULES

dut

```
 axis_data_width_converter #(
                                                                    .
 MASTER_WIDTH(MASTER_WIDTH),
                                                                    .
 SLAVE_WIDTH(SLAVE_WIDTH)
) dut ( .aclk(aclk), .arstn(arstn), .m_axis_tdata(m_axis_tdata), .m_axis_tva
```

Device under test, axis_data_width_converter