

# tb\_cocotb.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Test bench wrapper for cocotb

### License MIT

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## tb\_cocotb

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```
module tb_cocotb #(
  parameter
    SLAVE_WIDTH
    =
    1,
  parameter
    MASTER_WIDTH
    =
    1,
  parameter
    REVERSE
    =
    0
) ( input aclk, input arstn, output [(MASTER_WIDTH*8)-1:0] m_axis_tdata, out
```

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Test bench for data width converter. This will run a file through the system and write its output. These can then be compared to check for errors. If the files are identical, no errors. A FST file will be written.

**Parameters**

<b>SLAVE_WIDTH</b> parameter	Width of the slave input bus in bytes
<b>MASTER_WIDTH</b> parameter	Width of the master output bus in bytes
<b>REVERSE</b> parameter	Change byte order

**Ports**

<b>aclk</b>	Clock for AXIS
<b>arstn</b>	Negative reset for AXIS
<b>m_axis_tdata</b>	Output data
<b>m_axis_tvalid</b>	When active high the output data is valid
<b>m_axis_tready</b>	When set active high the output device is ready for data.
<b>m_axis_tlast</b>	Indicates last word in stream.
<b>s_axis_tdata</b>	Input data
<b>s_axis_tvalid</b>	When set active high the input data is valid
<b>s_axis_tready</b>	When active high the device is ready for input data.
<b>s_axis_tlast</b>	Is this the last word in the stream (active high).

**INSTANTIATED MODULES**

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**dut**

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```
axis_data_width_converter #(
    MASTER_WIDTH(MASTER_WIDTH),
    SLAVE_WIDTH(SLAVE_WIDTH)
) dut ( .aclk(aclk), .arstn(arstn), .m_axis_tdata(m_axis_tdata), .m_axis_tvalid(m_axis_tvalid), .s_axis_tdata(s_axis_tdata), .s_axis_tvalid(s_axis_tvalid), .s_axis_tready(s_axis_tready), .s_axis_tlast(s_axis_tlast) );
```

Device under test, axis\_data\_width\_converter