

# AXIS\_DATA\_WIDTH\_CONVERTER



December 11, 2024

Jay Convertino

# Contents

<b>1 Usage</b>	<b>2</b>
1.1 Introduction . . . . .	2
1.2 Dependencies . . . . .	2
1.2.1 fusesoc_info Depenecies . . . . .	2
1.3 In a Project . . . . .	2
<b>2 Architecture</b>	<b>2</b>
<b>3 Building</b>	<b>4</b>
3.1 fusesoc . . . . .	4
3.2 Source Files . . . . .	4
3.2.1 fusesoc_info File List . . . . .	4
3.3 Targets . . . . .	5
3.3.1 fusesoc_info Targets . . . . .	5
3.4 Directory Guide . . . . .	6
<b>4 Simulation</b>	<b>7</b>
4.1 iverilog . . . . .	7
4.2 cocotb . . . . .	7
<b>5 Code Documentation</b>	<b>8</b>
5.1 axis_data_width_converter . . . . .	9
5.2 tb_axis . . . . .	11
5.3 tb_cocotb verilog . . . . .	14
5.4 tb_cocotb python . . . . .	16

# 1 Usage

## 1.1 Introduction

This data width converter is for even integer divides of slave to master or master to slave. Example this core can go from 4 bytes to 2 bytes or 2 bytes to 4 bytes. It can not go from 5 bytes to 2 bytes or 2 bytes to 5 bytes.  $4/2$  is 2, a round number.  $5/2$  is a fractional number that will not work with this core.

## 1.2 Dependencies

The following are the dependencies of the cores.

- fusesoc 2.X
- iverilog (simulation)
- cocotb (simulation)

### 1.2.1 fusesoc\_info Depenecies

- dep
  - AFRL:utility:helper:1.0.0
- dep\_tb
  - AFRL:simulation:axis\_stimulator
  - AFRL:simulation:clock\_stimulator
  - AFRL:utility:sim\_helper

## 1.3 In a Project

Simply use this core between a sink and source AXIS devices. This will convert from one BUS size to another. Check the code to see if others will work correctly.

# 2 Architecture

The only module is the axis\_data\_width\_converter module. It is listed below.

- **axis\_data\_width\_converter** Implement an algorithm to convert BUS data interfaces in even multiples (see core for documentation).

The data width converter uses a generate block to select between three possible scenarios. First is they are equal, which just assigns the fields to each other. The second is slave is smaller than the master. This uses a register build up method by building up data till the correct number of bytes is reached. The final method is slave is larger than the master. This works by slicing the incoming data into chunks for the slave.

The slave is smaller than master block has the following steps.

1. Create registers used to buffer data and signals
2. Generate a backpressure ready signal for the axis input using the current ready master and its previous state.
3. The output is valid if the register has valid.
4. Last is set if register has last and the data is valid.
5. always block processes data in the following manner.
  - (a) Once out of reset, check if the output device is ready. If it is clear out the data tlast and valid registers and set the previous ready to 0.
  - (b) If the input is valid, and we were previously not ready or are currently ready start processing slave data.
    - i. build up slave data in buffer
    - ii. build up last buffer
    - iii. increment counter, or decrement if reversed byte order.
    - iv. Once counter hits its threshold, reset counter to initial value, and the buffer data is now valid so register for valid is set to active high.

The slave is larger than master block has the following steps.

1. Use a for loop to generate an assignment to take input data and slice it into a wire that is segmented into the size of the output data.
2. Ready happens when counter hits its count and the proper signals are set. Backpressure is needed since going larger to smaller will take more clock cycles.
3. For the output, if the register for valid is active high, output the proper signal or data.
4. always block processes data in the following manner.
  - (a) Once out of reset, check if the output device is ready. If it is, register for valid is set to 0 and the previous ready is cleared.

- (b) If the input is valid, and we were previously not ready or are currently ready, and the counter has reach the start count, start processing slave data.
  - i. In an unrolled for loop take the split input data and store it in a buffer.
  - ii. increment counter, or decrement if reversed byte order.
  - iii. Data is valid, so set it active high
  - iv. previous tready is set to active high, since the core has to be ready to take data.
- (c) Check the counter, and check if the destination device is ready, if it is, decrement the counter and reassert the valid and previous tready.

Please see ?? for more information.

## 3 Building

The AXIS data width converter core is written in Verilog 2001. They should synthesize in any modern FPGA software. The core comes as a fusesoc packaged core and can be included in any other core. Be sure to make sure you have meet the dependencies listed in the previous section.

### 3.1 fusesoc

Fusesoc is a system for building FPGA software without relying on the internal project management of the tool. Avoiding vendor lock in to Vivado or Quartus. These cores, when included in a project, can be easily integrated and targets created based upon the end developer needs. The core by itself is not a part of a system and should be integrated into a fusesoc based system. Simulations are setup to use fusesoc and are a part of its targets.

### 3.2 Source Files

#### 3.2.1 fusesoc\_info File List

- src
  - src/axis\_data\_width\_converter.v
- tb
  - 'tb/tb\_axis.v': 'file\_type': 'verilogSource'

## 3.3 Targets

### 3.3.1 fusesoc\_info Targets

- default  
Info: Default for IP intergration.
- sim  
Info: Test 1:1 conversion.
- sim\_reduce  
Info: Test data reduction.
- sim\_rand\_data\_reduce  
Info: Test data reduction with random data
- sim\_rand\_ready\_rand\_data\_reduce  
Info: Test data reduction with random ready and random data.
- sim\_8bit\_count\_data\_reduce  
Info: Test data reduction with counter data.
- sim\_rand\_ready\_8bit\_count\_data\_reduce  
Info: Test data reduction with counter data, and random ready.
- sim\_increase  
Info: Test data increase.
- sim\_rand\_data\_increase  
Info: Test data increase with random data.
- sim\_rand\_ready\_rand\_data\_increase  
Info: Test data increase with random data, and random ready.
- sim\_8bit\_count\_data\_increase  
Info: Test data increase with count data.
- sim\_rand\_ready\_8bit\_count\_data\_increase  
Info: Test data increase with count data, and random ready.

### 3.4 Directory Guide

Below highlights important folders from the root of the directory.

1. **docs** Contains all documentation related to this project.
  - **manual** Contains user manual and github page that are generated from the latex sources.
2. **src** Contains source files for the core
3. **tb** Contains test bench files for iverilog and cocotb

## 4 Simulation

There are a few different simulations that can be run for this core. All currently use iVerilog (icarus) to run. The first is iverilog, which uses verilog only for the simulations. The other is cocotb. This does a unit test approach to the testing and gives a list of tests that pass or fail.

### 4.1 iverilog

All simulation targets that do NOT have cocotb in the name use a verilog test bench with verilog stimulus components. These all read in a file and then write a file that has been processed by the data width converter. Then the input and output file are compared with a MD5 sum to check that they match. If they do not match then the test has failed. All of these tests provide fst output files for viewing the waveform in the there target build folder.

### 4.2 cocotb

To use the cocotb tests you must install the following python libraries.

```
$ pip install cocotb
$ pip install cocotbext-axi
```

Then you must use the cocotb sim target. In this case it is sim\_cocotb. This target can be run with various bus and fifo parameters.

```
$ fusesoc run --target sim_cocotb AFRL:buffer:axis_fifo
  ↳ :1.0.0 --SLAVE_WIDTH=8 --MASTER_WIDTH=32
```

The following is an example command to run through various parameters without typing them one by one.

```
$ for i in {1..32}; do sleep 5; export RY=$((RANDOM*2
  ↳ %32)); fusesoc run --target sim_cocotb AFRL:
  ↳ buffer:axis_fifo:1.0.0 --SLAVE_WIDTH=$i --
  ↳ MASTER_WIDTH=$RY; echo "SLAVE_WIDTH:" $i "MASTER_
  ↳ WIDTH:" $RY; done
```



## 5 Code Documentation

Natural docs is used to generate documentation for this project. The next lists the following sections.

- **axis\_data\_width\_converter** AXIS data width converter, converts from one BUS data size to another.
- **tb\_axis** Verilog test bench.
- **tb\_cocotb verilog** Verilog test bench base for cocotb.
- **tb\_cocotb python** cocotb unit test functions.

# axis\_data\_width\_converter.v

---

## AUTHORS

---

JAY CONVERTINO

---

## DATES

---

2021/06/21

---

## INFORMATION

---

### Brief

---

AXIS DATA WIDTH CONVERTER

### License MIT

---

Copyright 2021 Jay Convertino

Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions:

The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software.

THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

## axis\_data\_width\_converter

---

```
module axis_data_width_converter #(
    parameter
    SLAVE_WIDTH
    =
    1,
    parameter
    MASTER_WIDTH
    =
    1,
    parameter
    REVERSE
```

```

    =
    0
) ( input aclk, input arstn, output [(MASTER_WIDTH*8)-1:0] m_axis_tdata, out

```

Change size of streaming bus in even integers of. 1/2 2/1 2/4 4/2 etc.

## Parameters

<b>SLAVE_WIDTH</b> parameter	Width of the slave input bus in bytes
<b>MASTER_WIDTH</b> parameter	Width of the master output bus in bytes
<b>REVERSE</b> parameter	Change byte order

## Ports

<b>aclk</b>	Clock for AXIS
<b>arstn</b>	Negative reset for AXIS
<b>m_axis_tdata</b>	Output data
<b>m_axis_tvalid</b>	When active high the output data is valid
<b>m_axis_tready</b>	When set active high the output device is ready for data.
<b>m_axis_tlast</b>	Indicates last word in stream.
<b>s_axis_tdata</b>	Input data
<b>s_axis_tvalid</b>	When set active high the input data is valid
<b>s_axis_tready</b>	When active high the device is ready for input data.
<b>s_axis_tlast</b>	Is this the last word in the stream (active high).

# tb\_axis.v

---

## AUTHORS

---

JAY CONVERTINO

---

## DATES

---

2024/12/09

---

## INFORMATION

---

### Brief

---

Test bench for axis\_data\_width\_converter using axis stim and clock stim.

### License MIT

---

Copyright 2024 Jay Convertino

Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions:

The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software.

THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

## tb\_axis

---

```
module tb_axis #(
    parameter
    IN_FILE_NAME
    =
    in.bin,
    parameter
    OUT_FILE_NAME
    =
    out.bin,
    parameter
    RAND_READY
```

```

    =
    0,
    parameter
    SLAVE_WIDTH
    =
    2,
    parameter
    MASTER_WIDTH
    =
    4
  )()

```

Test bench for axis\_fifo. This will run a file through the system and write its output. These can then be compared to check for errors. If the files are identical, no errors. A FST file will be written.

### Parameters

<b>IN_FILE_NAME</b> parameter	File name for input.
<b>OUT_FILE_NAME</b> parameter	File name for output.
<b>RAND_READY</b> parameter	0 = no random ready. 1 = randomize ready.
<b>SLAVE_WIDTH</b> parameter	Width of the slave input bus in bytes
<b>MASTER_WIDTH</b> parameter	Width of the master output bus in bytes

## INSTANTIATED MODULES

---

### clk\_stim

---

```

clk_stimulus #(
    CLOCKS(1),
    CLOCK_BASE(1000000),
    CLOCK_INC(1000),
    RESETS(1),
    RESET_BASE(2000),
    RESET_INC(100)
) clk_stim ( .clkv(tb_dut_clk), .rstnv(tb_dut_rstn), .rstv() )

```

Generate a 50/50 duty cycle set of clocks and reset.

### slave\_axis\_stim

---

```

slave_axis_stimulus #(
    BUS_WIDTH(SBUS_WIDTH),
    USER_WIDTH(USER_WIDTH),

```

```

DEST_WIDTH(DEST_WIDTH),
FILE(IN_FILE_NAME)
) slave_axis_stim ( .m_axis_aclk(tb_dut_clk), .m_axis_arstn(tb_dut_rstn), .r

```

Device under test SLAVE stimulus module.

## dut

```

axis_data_width_converter #(
MASTER_WIDTH(MBUS_WIDTH),
SLAVE_WIDTH(SBUS_WIDTH)
) dut ( .aclk(tb_dut_clk), .arstn(tb_dut_rstn), .m_axis_tdata(tb_dut_data),

```

Device under test, axis\_data\_width\_converter

## master\_axis\_stim

```

master_axis_stimulus #(
BUS_WIDTH(MBUS_WIDTH),
USER_WIDTH(USER_WIDTH),
DEST_WIDTH(DEST_WIDTH),
RAND_READY(RAND_READY),
FILE(OUT_FILE_NAME)
) master_axis_stim ( .s_axis_aclk(tb_dut_clk), .s_axis_arstn(tb_dut_rstn),

```

Devie under test MASTER stimulus module.

# tb\_cocotb.v

---

## AUTHORS

---

JAY CONVERTINO

---

## DATES

---

2024/12/11

---

## INFORMATION

---

### Brief

---

Test bench wrapper for cocotb

### License MIT

---

Copyright 2024 Jay Convertino

Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions:

The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software.

THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

## tb\_cocotb

---

```
module tb_cocotb #(
  parameter
    SLAVE_WIDTH
    =
    1,
  parameter
    MASTER_WIDTH
    =
    1,
  parameter
    REVERSE
```

```

0
) ( input aclk, input arstn, output [(MASTER_WIDTH*8)-1:0] m_axis_tdata, out

```

Test bench for data width converter. This will run a file through the system and write its output. These can then be compared to check for errors. If the files are identical, no errors. A FST file will be written.

## Parameters

<b>SLAVE_WIDTH</b> parameter	Width of the slave input bus in bytes
<b>MASTER_WIDTH</b> parameter	Width of the master output bus in bytes
<b>REVERSE</b> parameter	Change byte order

## Ports

<b>aclk</b>	Clock for AXIS
<b>arstn</b>	Negative reset for AXIS
<b>m_axis_tdata</b>	Output data
<b>m_axis_tvalid</b>	When active high the output data is valid
<b>m_axis_tready</b>	When set active high the output device is ready for data.
<b>m_axis_tlast</b>	Indicates last word in stream.
<b>s_axis_tdata</b>	Input data
<b>s_axis_tvalid</b>	When set active high the input data is valid
<b>s_axis_tready</b>	When active high the device is ready for input data.
<b>s_axis_tlast</b>	Is this the last word in the stream (active high).

## INSTANTIATED MODULES

---

### dut

```

axis_data_width_converter #(
    MASTER_WIDTH(MBUS_WIDTH),
    SLAVE_WIDTH(SBUS_WIDTH)
) dut ( .aclk(aclk), .arstn(arstn), .m_axis_tdata(m_axis_tdata), .m_axis_tva

```

Device under test, axis\_data\_width\_converter



# tb\_cocotb.py

---

## AUTHORS

---

JAY CONVERTINO

---

## DATES

---

2024/12/09

---

## INFORMATION

---

### Brief

---

Cocotb test bench

### License MIT

---

Copyright 2024 Jay Convertino

Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions:

The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software.

THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

## FUNCTIONS

---

### random\_bool

---

```
def random_bool()
```

Return a infinite cycle of random bools

Returns: List

## start\_clock

---

```
def start_clock(  
    dut  
)
```

Start the simulation clock generator.

### Parameters

**dut**     Device under test passed from cocotb test function

## reset\_dut

---

```
async def reset_dut(  
    dut  
)
```

Cocotb coroutine for resets, used with await to make sure system is reset.

## single\_word

---

```
@cocotb.test()  
async def single_word(  
    dut  
)
```

Coroutine that is identified as a test routine. This routine tests for writing a single word, and then reading a single word.

### Parameters

**dut**     Device under test passed from cocotb.

## full\_empty

---

```
@cocotb.test()  
async def full_empty(  
    dut  
)
```

Coroutine that is identified as a test routine. This routine tests for writing till the fifo is full, Then reading from the full FIFO.

### Parameters

**dut**     Device under test passed from cocotb.

## random\_ready

---

```
@cocotb.test()  
async def random_ready(  
    dut
```

```
)
```

Coroutine that is identified as a test routine. This routine tests for randomized ready from the sink.

### Parameters

**dut** Device under test passed from cocotb.

## in\_reset

---

```
@cocotb.test()
async def in_reset(
    dut
)
```

Coroutine that is identified as a test routine. This routine tests if device stays in unready state when in reset.

### Parameters

**dut** Device under test passed from cocotb.

## no\_clock

---

```
@cocotb.test()
async def no_clock(
    dut
)
```

Coroutine that is identified as a test routine. This routine tests if no ready when clock is lost and device is left in reset.

### Parameters

**dut** Device under test passed from cocotb.