axis_fifo.v

AUTHORS

JAY CONVERTINO

DATES

2021/06/29

INFORMATION

Brief

Wraps the standard FIFO with an axi streaming interface.

License MIT

Copyright 2021 Jay Convertino

Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions:

The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software.

THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

axis_fifo

```
module axis_fifo #(
parameter
FIFO_DEPTH
 =
256,
parameter
COUNT_WIDTH
 =
8,
parameter
BUS_WIDTH
 =
1,
parameter
```

```
USER_WIDTH
 =
1,
parameter
DEST_WIDTH
 =
1,
parameter
RAM_TYPE
 =
"block",
parameter
PACKET_MODE
 =
0,
parameter
COUNT_DELAY
 =
1,
parameter
COUNT_ENA
 =
1
) ( input m_axis_aclk, input m_axis_arstn, output m_axis_tvalid, input m_axi
```

AXIS fifo

Parameters

FIFO_DEPTH parameter	Depth of the fifo, must be a power of two number(divisable aka 256 = 2^8). Any non-power of two will be rounded up to the next closest.
COUNT_WIDTH parameter	Data count output width in bits. Should be the same power of two as fifo depth(256 for fifo depth... this should be 8).
BUS_WIDTH parameter	Width of the axis data bus input/output in bytes.
USER_WIDTH parameter	Width of the axis user bus input/output in bits.
DEST_WIDTH parameter	Width of the axis dest bus input/output in bits.
RAM_TYPE parameter	RAM type setting.
PACKET_MODE parameter	Set axis fifo to wait for tlast before allowing a read on master port output.
COUNT_DELAY parameter	Delay count by one clock cycle of the data count clock.
COUNT_ENA parameter	Enable count, set this to 0 to disable (only disable if read/write/data_count are on the same clock domain!).

Ports

m_axis_aclk	Clock for AXIS
m_axis_arstn	Negative reset for AXIS
m_axis_tvalid	When active high the output data is valid
m_axis_tready	When set active high the output device is ready for data.
m_axis_tdata	Output data
m_axis_tkeep	Output valid byte indicator
m_axis_tlast	Indicates last word in stream.
m_axis_tuser	Output user bus

m_axis_tdest	Output destination
s_axis_aclk	Clock for AXIS
s_axis_arstn	Negative reset for AXIS
s_axis_tvalid	When set active high the input data is valid
s_axis_tready	When active high the device is ready for input data.
s_axis_tdata	Input data
s_axis_tkeep	Input valid byte indicator
s_axis_tlast	Is this the last word in the stream (active high).
s_axis_tuser	Input user bus
s_axis_tdest	Input desitination
data_count_aclk	Clock for data count
data_count_arstn	Negative edge reset for data count.
data_count	Output that indicates the amount of data in the FIFO.

INSTANTIATED MODULES

axis_fifo

```
fifo #(
.FIFO_DEPTH(c_FIFO_DEPTH),
.BYTE_WIDTH(c_FIFO_WIDTH),
.COUNT_WIDTH(COUNT_WIDTH),
.FWFT(1),
.RD_SYNC_DEPTH(0),
.WR_SYNC_DEPTH(0),
.DC_SYNC_DEPTH(0),
.COUNT_DELAY(COUNT_DELAY),
.COUNT_ENA(COUNT_ENA),
.
```

```
DATA_ZERO                                                                       (
1),                                                                             .
ACK_ENA                                                                         (
0),                                                                             .
RAM_TYPE                                                                        (
RAM_TYPE)
) axis_fifo ( .rd_clk (m_axis_aclk), .rd_rstn (m_axis_arstn), .rd_en (s_rd_e
```

Generic FIFO that acts like a Xilinx FIFO.

axis_control

```
axis_fifo_ctrl #(                                                               .
BUS_WIDTH                                                                       (
BUS_WIDTH),                                                                     .
FIFO_WIDTH                                                                      (
c_FIFO_WIDTH),                                                                  .
USER_WIDTH                                                                      (
USER_WIDTH),                                                                    .
DEST_WIDTH                                                                      (
DEST_WIDTH),                                                                    .
PACKET_MODE(PACKET_MODE)
) axis_control ( .m_axis_aclk (m_axis_aclk), .m_axis_arstn (m_axis_arstn),
```

Create signals to control FIFO and provide AXIS interace.