

# axis\_ctrl\_fifo.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Wraps the standard FIFO with an axi streaming interface.

### License MIT

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## axis\_fifo\_ctrl

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```
module axis_fifo_ctrl #(
    parameter
    BUS_WIDTH
    =
    1,
    parameter
    FIFO_WIDTH
    =
    8,
    parameter
    FIFO_POWER
```

```

    =
    8,
    parameter
    USER_WIDTH
    =
    1,
    parameter
    DEST_WIDTH
    =
    1,
    parameter
    PACKET_MODE
    =
    0
) ( input m_axis_aclk, input m_axis_arstn, output m_axis_tvalid, input m_axi

```

AXIS fifo control

## Parameters

<b>BUS_WIDTH</b> parameter	Width of the axis data bus input/output in bytes. FIFO_WIDTH - FIFO_POWER -
<b>USER_WIDTH</b> parameter	Width of the axis user bus input/output in bits.
<b>DEST_WIDTH</b> parameter	Width of the axis dest bus input/output in bits.
<b>PACKET_MODE</b> parameter	Set axis fifo to wait for tlast before allowing a read on master port output.

## Ports

<b>m_axis_aclk</b>	Clock for AXIS
<b>m_axis_arstn</b>	Negative reset for AXIS
<b>m_axis_tvalid</b>	When active high the output data is valid
<b>m_axis_tready</b>	When set active high the output device is ready for data.
<b>m_axis_tdata</b>	Output data
<b>m_axis_tkeep</b>	Output valid byte indicator
<b>m_axis_tlast</b>	Indicates last word in stream.
<b>m_axis_tuser</b>	Output user bus
<b>m_axis_tdest</b>	Output destination
<b>s_axis_tlast</b>	Is this the last word in the stream (active high).
<b>rd_en</b>	Active high enable of read interface.
<b>rd_valid</b>	Active high output that the data is valid.
<b>rd_data</b>	Output data
<b>rd_empty</b>	Active high output when read is empty.
<b>wr_full</b>	Active high output that the FIFO is full.