axis_ctrl_fifo.v

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DATES

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INFORMATION

Brief

Wraps the standard FIFO with an axi streaming interface, Xilinx AXIS FIFO Emulation.

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axis_fifo_ctrl

```
module axis_fifo_ctrl #(
parameter
BUS_WIDTH
 =
1,
parameter
FIFO_WIDTH
 =
8,
parameter
FIFO_POWER
 =
8,
parameter
```

```
 USER_WIDTH
  =
 1,
 parameter
 DEST_WIDTH
  =
 1,
 parameter
 PACKET_MODE
  =
 0
)
                                                                    (
 input
 m_axis_aclk,
 input
 m_axis_arstn,
 output
 m_axis_tvalid,
 input
 m_axis_tready,
 output
  [(BUS_WIDTH*8)-1:0]
 m_axis_tdata,
 output
  [BUS_WIDTH-1:0]
 m_axis_tkeep,
 output
 m_axis_tlast,
 output
  [USER_WIDTH-1:0]
 m_axis_tuser,
 output
  [DEST_WIDTH-1:0]
 m_axis_tdest,
 input
 s_axis_tlast,
 output
 rd_en,
 input
 rd_valid,
 input
  [(FIFO_WIDTH*8)-1:0]
 rd_data,
 input
 rd_empty,
 input
 wr_full
)
```

AXIS fifo control

Parameters

BUS_WIDTH Width of the axis data bus input/output in bytes. FIFO_WIDTH - FIFO_POWER -
parameter

USER_WIDTH Width of the axis user bus input/output in bits.
parameter

DEST_WIDTH Width of the axis dest bus input/output in bits.
parameter

PACKET_MODE Set axis fifo to wait for tlast before allowing a read on master port output.
parameter

Ports

m_axis_aclk `input`	Clock for AXIS
m_axis_arstn `input`	Negative reset for AXIS
m_axis_tvalid `output`	When active high the output data is valid
m_axis_tready `input`	When set active high the output device is ready for data.
m_axis_tdata `output [(BUS_WIDTH* 8)- 1:0]`	Output data
m_axis_tkeep `output [BUS_WIDTH- 1:0]`	Output valid byte indicator
m_axis_tlast `output [BUS_WIDTH- 1:0]`	Indicates last word in stream.
m_axis_tuser `output [USER_WIDTH- 1:0]`	Output user bus
m_axis_tdest `output [DEST_WIDTH- 1:0]`	Output destination
s_axis_tlast `input [DEST_WIDTH- 1:0]`	Is this the last word in the stream (active high).
rd_en `output [DEST_WIDTH- 1:0]`	Active high enable of read interface.
rd_valid `input [DEST_WIDTH- 1:0]`	Active high output that the data is valid.
rd_data `input [(FIFO_WIDTH* 8)- 1:0]`	Output data
rd_empty `input [(FIFO_WIDTH* 8)- 1:0]`	Active high output when read is empty.
wr_full `input [(FIFO_WIDTH* 8)- 1:0]`	Active high output that the FIFO is full.