axis_ctrl_fifo.v

AUTHORS

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DATES

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INFORMATION

Brief

Wraps the standard FIFO with an axi streaming interface.

License MIT

axis_fifo_ctrl

```
module axis_fifo_ctrl #(
parameter
BUS_WIDTH
 =
1,
parameter
FIFO_WIDTH
 =
8,
parameter
FIFO_POWER
```

```
  =
 8,
 parameter
 USER_WIDTH
  =
 1,
 parameter
 DEST_WIDTH
  =
 1,
 parameter
 PACKET_MODE
  =
 0
) ( input m_axis_aclk, input m_axis_arstn, output m_axis_tvalid, input m_axi
```

AXIS fifo control

Parameters

BUS_WIDTH parameter	Width of the axis data bus input/output in bytes. FIFO_WIDTH - FIFO_POWER -
USER_WIDTH parameter	Width of the axis user bus input/output in bits.
DEST_WIDTH parameter	Width of the axis dest bus input/output in bits.
PACKET_MODE parameter	Set axis fifo to wait for tlast before allowing a read on master port output.

Ports

m_axis_aclk	Clock for AXIS
m_axis_arstn	Negative reset for AXIS
m_axis_tvalid	When active high the output data is valid
m_axis_tready	When set active high the output device is ready for data.
m_axis_tdata	Output data
m_axis_tkeep	Output valid byte indicator
m_axis_tlast	Indicates last word in stream.
m_axis_tuser	Output user bus
m_axis_tdest	Output destination
s_axis_tlast	Is this the last word in the stream (active high).
rd_en	Active high enable of read interface.
rd_valid	Active high output that the data is valid.
rd_data	Output data
rd_empty	Active high output when read is empty.
wr_full	Active high output that the FIFO is full.