

tb_axis.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench for axis_fifo using axis_stim and clock_stim.

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tb_axis

```
module tb_axis #(
    parameter
    IN_FILE_NAME
    =
    "in.bin",
    parameter
    OUT_FILE_NAME
    =
    "out.bin",
    parameter
    FIFO_DEPTH
```

```

    =
    128,
    parameter
    RAND_READY
    =
    0
)

```

Test bench for axis_fifo. This will run a file through the system and write its output. These can then be compared to check for errors. If the files are identical, no errors. A FST file will be written.

Parameters

IN_FILE_NAME parameter	File name for input.
OUT_FILE_NAME parameter	File name for output.
FIFO_DEPTH parameter	Number of transactions to buffer.
RAND_READY parameter	0 = no random ready. 1 = randomize ready.

INSTANTIATED MODULES

clk_stim

```

clk_stimulus #(
    CLOCKS(2),
    CLOCK_BASE(1000000),
    CLOCK_INC(10),
    RESETS(2),
    RESET_BASE(2000),
    RESET_INC(100)
) clk_stim ( .clkv({tb_dut_clk, tb_stim_clk}), .rstnv({tb_dut_rstn, tb_stim_rstn})

```

Generate a 50/50 duty cycle set of clocks and reset.

slave_axis_stim

```

slave_axis_stimulus #(
    BUS_WIDTH(BUS_WIDTH),
    USER_WIDTH(USER_WIDTH),
    DEST_WIDTH(DEST_WIDTH),
    FILE(IN_FILE_NAME)
) slave_axis_stim ( .m_axis_aclk(tb_stim_clk), .m_axis_arstn(tb_stim_rstn),

```

Device under test SLAVE stimulus module.

dut

```
axis_fifo #(
    FIFO_DEPTH(FIFO_DEPTH),
    COUNT_WIDTH(8),
    BUS_WIDTH(BUS_WIDTH),
    USER_WIDTH(USER_WIDTH),
    DEST_WIDTH(DEST_WIDTH),
    RAM_TYPE("block"),
    PACKET_MODE(0),
    COUNT_DELAY(1),
    COUNT_ENA(1)
) dut ( .s_axis_aclk(tb_stim_clk), .s_axis_arstn(tb_stim_rstn), .s_axis_tva
```

Device under test, axis_fifo

master_axis_stim

```
master_axis_stimulus #(
    BUS_WIDTH(BUS_WIDTH),
    USER_WIDTH(USER_WIDTH),
    DEST_WIDTH(DEST_WIDTH),
    RAND_READY(RAND_READY),
    FILE(OUT_FILE_NAME)
) master_axis_stim ( .s_axis_aclk(tb_dut_clk), .s_axis_arstn(tb_dut_rstn),
```

Devie under test MASTER stimulus module.