

tb_cocotb.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

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tb_cocotb

```
module tb_cocotb #(
  parameter
    FIFO_DEPTH
    =
    256,
  parameter
    COUNT_WIDTH
    =
    8,
  parameter
    BUS_WIDTH
    =
    1,
  parameter
```

```

USER_WIDTH
=
1,
parameter
DEST_WIDTH
=
1,
parameter
RAM_TYPE
=
"block",
parameter
PACKET_MODE
=
0,
parameter
COUNT_DELAY
=
1,
parameter
COUNT_ENA
=
1
)

input
m_axis_aclk,
input
m_axis_arstn,
output
m_axis_tvalid,
input
m_axis_tready,
output
[(BUS_WIDTH*8)-1:0]
m_axis_tdata,
output
[BUS_WIDTH-1:0]
m_axis_tkeep,
output
m_axis_tlast,
output
[USER_WIDTH-1:0]
m_axis_tuser,
output
[DEST_WIDTH-1:0]
m_axis_tdest,
input
s_axis_aclk,
input
s_axis_arstn,
input
s_axis_tvalid,
output
s_axis_tready,
input
[(BUS_WIDTH*8)-1:0]
s_axis_tdata,
input
[BUS_WIDTH-1:0]
s_axis_tkeep,
input
s_axis_tlast,
input
[USER_WIDTH-1:0]
s_axis_tuser,

```

(

```

input
[DEST_WIDTH-1:0]
s_axis_tdest,
input
data_count_aclk,
input
data_count_arstn,
output
[COUNT_WIDTH:0]
data_count
)

```

Test bench for axis_fifo. This will run a file through the system and write its output. These can then be compared to check for errors. If the files are identical, no errors. A FST file will be written.

Parameters

FIFO_DEPTH parameter	Depth of the fifo, must be a power of two number(divisable aka $256 = 2^8$). Any non-power of two will be rounded up to the next closest.
COUNT_WIDTH parameter	Data count output width in bits. Should be the same power of two as fifo depth(256 for fifo depth... this should be 8).
BUS_WIDTH parameter	Width of the axis data bus input/output in bytes.
USER_WIDTH parameter	Width of the axis user bus input/output in bits.
DEST_WIDTH parameter	Width of the axis dest bus input/output in bits.
RAM_TYPE parameter	RAM type setting.
PACKET_MODE parameter	Set axis fifo to wait for tlast before allowing a read on master port output.
COUNT_DELAY parameter	Delay count by one clock cycle of the data count clock.
COUNT_ENA parameter	Enable count, set this to 0 to disable (only disable if read/write/data_count are on the same clock domain!).

Ports

m_axis_aclk input	Clock for AXIS
m_axis_arstn input	Negative reset for AXIS
m_axis_tvalid output	When active high the output data is valid
m_axis_tready input	When set active high the output device is ready for data.
m_axis_tdata output [(BUS_WIDTH* 8)- 1:0]	Output data
m_axis_tkeep output [BUS_WIDTH- 1:0]	Output valid byte indicator
m_axis_tlast output [BUS_WIDTH- 1:0]	Indicates last word in stream.
m_axis_tuser output [USER_WIDTH- 1:0]	Output user bus
m_axis_tdest output [DEST_WIDTH- 1:0]	Output destination
s_axis_aclk	Clock for AXIS

<code>input [DEST_WIDTH- 1:0]</code>	
s_axis_arstn	Negative reset for AXIS
<code>input [DEST_WIDTH- 1:0]</code>	
s_axis_tvalid	When set active high the input data is valid
<code>input [DEST_WIDTH- 1:0]</code>	
s_axis_tready	When active high the device is ready for input data.
<code>output [DEST_WIDTH- 1:0]</code>	
s_axis_tdata	Input data
<code>input [(BUS_WIDTH* 8)- 1:0]</code>	
s_axis_tkeep	Input valid byte indicator
<code>input [BUS_WIDTH- 1:0]</code>	
s_axis_tlast	Is this the last word in the stream (active high).
<code>input [BUS_WIDTH- 1:0]</code>	
s_axis_tuser	Input user bus
<code>input [USER_WIDTH- 1:0]</code>	
s_axis_tdest	Input desitination
<code>input [DEST_WIDTH- 1:0]</code>	
data_count_aclk	Clock for data count
<code>input [DEST_WIDTH- 1:0]</code>	
data_count_arstn	Negative edge reset for data count.
<code>input [DEST_WIDTH- 1:0]</code>	
data_count	Output that indicates the amount of data in the FIFO.
<code>output [COUNT_WIDTH:0]</code>	

INSTANTIATED MODULES

dut

Device under test, axis_fifo