axis_uart_tx.v

AUTHORS

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DATES

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INFORMATION

Brief

UART TX from AXIS bus.

License MIT

axis_uart_tx

```
module axis_uart_tx #(
parameter
PARITY_ENA
 =
0,
parameter
PARITY_TYPE
 =
1,
parameter
STOP_BITS
 =
1,
parameter
```

```
DATA_BITS
  =
8,
parameter
DELAY
  =
0
) ( input aclk, input arstn, input [DATA_BITS-1:0] s_axis_tdata, input s_axi
```

AXIS UART TX, simple UART TX from AXI Streaming interface.

Parameters

PARITY_ENA parameter	Enable Parity for the data in and out.
PARITY_TYPE parameter	Set the parity type, 0 = even, 1 = odd, 2 = mark, 3 = space.
STOP_BITS parameter	Number of stop bits, 0 to crazy non-standard amounts.
DATA_BITS parameter	Number of data bits, 1 to crazy non-standard amounts.
DELAY parameter	Delay in tx data output. Delays the time to output of the data.

Ports

aclk	Clock for AXIS
arstn	Negative reset for AXIS
s_axis_tdata	Input data for UART TX.
s_axis_tvalid	When set active high the input data is valid
s_axis_tready	When active high the device is ready for input data.
uart_clk	Clock used for BAUD rate generation
uart_rstn	Negative reset for UART, for anything clocked on uart_clk
uart_ena	When active high enable UART transmit state.
txd	transmit for UART (output to RX)