

# axis\_uart\_rx.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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UART RX to AXIS bus.

### License MIT

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## axis\_uart\_rx

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```
module axis_uart_rx #(
    parameter
    PARITY_ENA
    =
    0,
    parameter
    PARITY_TYPE
    =
    0,
    parameter
    STOP_BITS
```

```

    =
    1,
    parameter
    DATA_BITS
    =
    8,
    parameter
    DELAY
    =
    0
) ( input aclk, input arstn, output parity_err, output frame_err, output [DATA_BITS] data_out )

```

AXIS UART, simple UART with AXI Streaming interface.

## Parameters

<b>PARITY_ENA</b> parameter	Enable Parity for the data in and out.
<b>PARITY_TYPE</b> parameter	Set the parity type, 0 = even, 1 = odd, 2 = mark, 3 = space.
<b>STOP_BITS</b> parameter	Number of stop bits, 0 to crazy non-standard amounts.
<b>DATA_BITS</b> parameter	Number of data bits, 1 to crazy non-standard amounts.
<b>DELAY</b> parameter	Delay in rx data input.

## Ports

<b>aclk</b>	Clock for AXIS
<b>arstn</b>	Negative reset for AXIS
<b>parity_err</b>	Indicates error with parity check (active high)
<b>frame_err</b>	Indicates error with frame (active high)
<b>m_axis_tdata</b>	Output data from UART RX
<b>m_axis_tvalid</b>	When active high the output data is valid
<b>m_axis_tready</b>	When set active high the output device is ready for data.
<b>uart_clk</b>	Clock used for BAUD rate generation
<b>uart_rstn</b>	Negative reset for UART, for anything clocked on uart_clk
<b>uart_ena</b>	Enable UART data processing from RX.
<b>uart_hold</b>	Output to hold clock till in receive state.
<b>rxdata</b>	receive for UART (input from TX)