# axis_spi_master.v

## AUTHORS

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[file:///home/convertinoj/Documents/research/sdcard/CARD](file:///home/convertinoj/Documents/research/sdcard/CARD) date:  2025/04/22

## INFORMATION

### Brief

Stream SPI input/output data over AXIS bus.

### License MIT

### axis_spi_master

```verilog
module axis_spi_master #(
parameter
CLOCK_SPEED
  =
2000000,
parameter
BUS_WIDTH
  =
4,
parameter
SELECT_WIDTH
  =
8
) ( input aclk, input arstn, input [BUS_WIDTH*8-1:0] s_axis_tdata, input s_a
```

SPI core with axis input/output data. Read/Write is size of BUS_WIDTH bytes. Write activates core for read.

**Parameters**

| | |
|---|---|
| **CLOCK_SPEED**<br>parameter | This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate. |
| **BUS_WIDTH**<br>parameter | AXIS data width in bytes. |
| **SELECT_WIDTH**<br>parameter | Bit width of the slave select. |

**Ports**

| | |
|---|---|
| **aclk** | Clock for AXIS |
| **arstn** | Negative reset for AXIS |
| **s_axis_tdata** | Input data for SPI MOSI. |
| **s_axis_tvalid** | When set active high the input data is valid |
| **s_axis_tready** | When active high the device is ready for input data. |
| **m_axis_tdata** | Output data from SPI MISO |
| **m_axis_tvalid** | When active high the output data is valid |
| **m_axis_tready** | When set active high the output device is ready for data. |
| **sclk** | spi clock, should only drive output pins to devices. |
| **mosi** | transmit for master output |
| **miso** | receive for master input |
| **ssn_i** | slave select input |
| **ssn_o** | slave select output |
| **rate** | output rate of spi core. |
| **cpol** | clock polarity of sclk |
| **cpha** | clock phase of sclk |
| **miso_dcount** | Current number of input bits available from parallel register. |
| **mosi_dcount** | current number of output bits available to serial shift output. |

## STATE MACHINE

Constants that makeup the data_state machine.

## ready

```
localparam ready = 3'd1
```

ready and waiting for data

## processing

```
localparam processing = 3'd3
```

data is being processed

## error

```
localparam error = 3'd0
```

someone made a whoops

# INSTANTIATED MODULES

## inst_spi_output_clk

```
mod_clock_ena_gen #(
                                                                    .
CLOCK_SPEED(CLOCK_SPEED)
) inst_spi_output_clk ( .clk(aclk), .rstn(arstn), .start0(1'b0), .clr(spi_e
```

Generates enable at rate for spi output data.

## inst_spi_input_clk

```
mod_clock_ena_gen #(
                                                                    .
CLOCK_SPEED(CLOCK_SPEED)
) inst_spi_input_clk ( .clk(aclk), .rstn(arstn), .start0(1'b1), .clr(spi_er
```

Generates enable at rate for spi input data.

## inst_piso

```
piso #(
                                                                    .
BUS_WIDTH(BUS_WIDTH)
) inst_piso ( .clk(aclk), .rstn(arstn), .ena(spi_ena_mosi), .load(spi_mosi_
```

take axis input parallel data at bus size, and output the word to the spi bus.

## inst_sipo

```
sipo #(
                                                                    .
BUS_WIDTH(BUS_WIDTH)
) inst_sipo ( .clk(aclk), .rstn(arstn), .ena(spi_ena_miso), .load(spi_miso_
```

take serial input data, and output the world to the parallel data bus.