uart_baud_gen.v

AUTHORS

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DATES

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INFORMATION

Brief

Generate UART BAUD rate by dividing input clock rate using modulo divide (subtract and carry remainder)

License MIT

uart_baud_gen

```
module uart_baud_gen #(
parameter
BAUD_CLOCK_SPEED
 =
2000000,
parameter
BAUD_RATE
 =
115200,
parameter
```

```
 DELAY
  =
 0
) ( input uart_clk, input uart_rstn, input uart_hold, output uart_ena )
```

Baud rate generator

Parameters

BAUD_CLOCK_SPEED This is the aclk frequency in Hz
parameter

BAUD_RATE Serial Baud, this can be any value including non-standard.
parameter

DELAY Delay in rx data input.
parameter

Ports

uart_clk Clock used for BAUD rate generation

uart_rstn Negative reset for UART, for anything clocked on uart_clk

uart_hold Output to hold clock till in receive state.

uart_ena Enable UART data processing from RX.