

tb_cocotb.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

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tb_cocotb

```
module tb_cocotb #(
  parameter
  PARITY_ENA
  =
  0,
  parameter
  PARITY_TYPE
  =
  0,
  parameter
  STOP_BITS
  =
  1,
  parameter
```

```
DATA_BITS
=
8,
parameter
DELAY
=
0
) ( input aclk, input arstn, output parity_err, output frame_err, output [DA
```

Test bench for axis_uart_rx.

Parameters

- PARITY_ENA** Enable Parity for the data in and out.
parameter
- PARITY_TYPE** Set the parity type, 0 = even, 1 = odd, 2 = mark, 3 = space.
parameter
- STOP_BITS** Number of stop bits, 0 to crazy non-standard amounts.
parameter
- DATA_BITS** Number of data bits, 1 to crazy non-standard amounts.
parameter
- DELAY** Delay in rx data input.
parameter

Ports

- aclk** Clock for AXIS
- arstn** Negative reset for AXIS
- parity_err** Indicates error with parity check (active high)
- frame_err** Indicates error with frame (active high)
- m_axis_tdata** Output data from UART RX
- m_axis_tvalid** When active high the output data is valid
- m_axis_tready** When set active high the output device is ready for data.
- uart_clk** Clock used for BAUD rate generation
- uart_rstn** Negative reset for UART, for anything clocked on uart_clk
- uart_ena** Enable UART data processing from RX.
- uart_hold** Output to hold clock till in receive state.
- rx** receive for UART (input from TX)

INSTANTIATED MODULES

dut

```
axis_uart_rx #(
    PARITY_ENA(PARITY_ENA),
    PARITY_TYPE(PARITY_TYPE),
    STOP_BITS(STOP_BITS),
    DATA_BITS(DATA_BITS),
    DELAY(DELAY)
```

```
) dut ( .aclk(aclk), .arstn(arstn), .parity_err(parity_err), .frame_err(frame_err)
```

Device under test, axis_uart_rx