axis_uart_rx.v

AUTHORS

JAY CONVERTINO

DATES

2021/06/24

INFORMATION

Brief

UART RX to AXIS bus.

License MIT

axis_uart_rx

```
module axis_uart_rx #(
parameter
PARITY_ENA
 =
0,
parameter
PARITY_TYPE
 =
0,
parameter
STOP_BITS
```

```
  =
1,
parameter
DATA_BITS
  =
8,
parameter
DELAY
  =
0
) ( input aclk, input arstn, output parity_err, output frame_err, output [DA
```

AXIS UART, simple UART with AXI Streaming interface.

Parameters

PARITY_ENA parameter	Enable Parity for the data in and out.
PARITY_TYPE parameter	Set the parity type, 0 = even, 1 = odd, 2 = mark, 3 = space.
STOP_BITS parameter	Number of stop bits, 0 to crazy non-standard amounts.
DATA_BITS parameter	Number of data bits, 1 to crazy non-standard amounts.
DELAY parameter	Delay in rx data input.

Ports

aclk	Clock for AXIS
arstn	Negative reset for AXIS
parity_err	Indicates error with parity check (active high)
frame_err	Indicates error with frame (active high)
m_axis_tdata	Output data from UART RX
m_axis_tvalid	When active high the output data is valid
m_axis_tready	When set active high the output device is ready for data.
uart_clk	Clock used for BAUD rate generation
uart_rstn	Negative reset for UART, for anything clocked on uart_clk
uart_ena	Enable UART data processing from RX.
uart_hold	Output to hold clock till in receive state.
rxd	receive for UART (input from TX)