# tb_coctb.v

## AUTHORS

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## DATES

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## INFORMATION

### Brief

Test bench wrapper for cocotb

### License MIT



### tb_cocotb

```
module tb_cocotb #(
parameter
PARITY_ENA
 =
0,
parameter
PARITY_TYPE
 =
1,
parameter
STOP_BITS
 =
1,
parameter
```

```
 DATA_BITS
  =
 8,
 parameter
 DELAY
  =
 0
) ( input aclk, input arstn, input [DATA_BITS-1:0] s_axis_tdata, input s_axi
```

Test bench for AXIS UART TX, simple UART TX from AXI Streaming interface.

### Parameters

| | |
|---|---|
| **PARITY_ENA**<br>parameter | Enable Parity for the data in and out. |
| **PARITY_TYPE**<br>parameter | Set the parity type, 0 = even, 1 = odd, 2 = mark, 3 = space. |
| **STOP_BITS**<br>parameter | Number of stop bits, 0 to crazy non-standard amounts. |
| **DATA_BITS**<br>parameter | Number of data bits, 1 to crazy non-standard amounts. |
| **DELAY**<br>parameter | Delay in tx data output. Delays the time to output of the data. |

### Ports

| | |
|---|---|
| **aclk** | Clock for AXIS |
| **arstn** | Negative reset for AXIS |
| **s_axis_tdata** | Input data for UART TX. |
| **s_axis_tvalid** | When set active high the input data is valid |
| **s_axis_tready** | When active high the device is ready for input data. |
| **uart_clk** | Clock used for BAUD rate generation |
| **uart_rstn** | Negative reset for UART, for anything clocked on uart_clk |
| **uart_ena** | When active high enable UART transmit state. |
| **txd** | transmit for UART (output to RX) |

## INSTANTIATED MODULES

### dut

```
 axis_uart_tx #(
                                                                    .
 PARITY_ENA(0),
                                                                    .
 PARITY_TYPE(1),
                                                                    .
 STOP_BITS(1),
                                                                    .
 DATA_BITS(8),
                                                                    .
 DELAY(0)
) dut ( .aclk(aclk), .arstn(arstn), .s_axis_tdata(s_axis_tdata), .s_axis_tva
```

Device under test, axis_uart_tx