tb_cocotb.v

AUTHORS

JAY CONVERTINO

DATES

2025/04/24

INFORMATION

Brief

Test bench wrapper for cocotb

License MIT

tb_cocotb

```
module tb_cocotb #(
parameter
CLOCK_SPEED
 =
2000000,
parameter
BUS_WIDTH
 =
4,
parameter
SELECT_WIDTH
 =
1,
parameter
```

```
 RATE
  =
 115200
) ( input aclk, input arstn, input [BUS_WIDTH*8-1:0] s_axis_tdata, input s_a
```

SPI core with axis input/output data. Read/Write is size of BUS_WIDTH bytes. Write activates core for read.

Parameters

CLOCK_SPEED parameter	This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate.
BUS_WIDTH parameter	AXIS data width in bytes.
SELECT_WIDTH parameter	Bit width of the slave select.
RATE parameter	Select the data rate of the spi core.

Ports

aclk	Clock for AXIS
arstn	Negative reset for AXIS
s_axis_tdata	Input data for UART TX.
s_axis_tvalid	When set active high the input data is valid
s_axis_tready	When active high the device is ready for input data.
m_axis_tdata	Output data from UART RX
m_axis_tvalid	When active high the output data is valid
m_axis_tready	When set active high the output device is ready for data.
sclk	spi clock, should only drive output pins to devices.
mosi	transmit for master output
miso	receive for master input
ssn_i	slave select input
ssn_o	slave select output
rate parameter	output rate of spi core.
cpol	clock polarity of spi_clk
cpha	clock phase of spi_clk
miso_dcount	Current number of input bits available from parallel register.
mosi_dcount	current number of output bits available to serial shift output.

INSTANTIATED MODULES

dut

```
axis_spi_master #(
.CLOCK_SPEED(CLOCK_SPEED),
.BUS_WIDTH(BUS_WIDTH),
.SELECT_WIDTH(SELECT_WIDTH)
```

```
) dut ( .aclk(aclk), .arstn(arstn), .s_axis_tdata(s_axis_tdata), .s_axis_t\
```

Device under test, axis_spi_master