tb_axis.v

AUTHORS

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DATES

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INFORMATION

Brief

Generic AXIS test bench top with verification.

License MIT

tb_axis

```
module tb_axis #(
parameter
OUT_FILE_NAME
 =
in.bin,
parameter
IN_FILE_NAME
 =
out.bin,
parameter
RAND_READY
```

```
  =
 0
)
```

Generic AXIS test bench top with verification.

Parameters

OUT_FILE_NAME Name of the output file to write.
parameter

IN_FILE_NAME Name of the input file to read from.
parameter

RAND_READY Randomize the Ready signal from the writer (master_axis_stim) core.
parameter

INSTANTIANTED MODULES

clk_stim

```
clk_stimulus #(
                                                                    .
CLOCKS(1),
                                                                    .
CLOCK_BASE(1000000),
                                                                    .
CLOCK_INC(1000),
                                                                    .
RESETS(1),
                                                                    .
RESET_BASE(2000),
                                                                    .
RESET_INC(100)
) clk_stim ( .clkv(tb_stim_clk), .rstnv(tb_stim_rstn), .rstv() )
```

Generate a clock for the modules.

slave_axis_stim

```
slave_axis_stimulus #(
                                                                    .
BUS_WIDTH(BUS_WIDTH),
                                                                    .
USER_WIDTH(USER_WIDTH),
                                                                    .
DEST_WIDTH(DEST_WIDTH),
                                                                    .
FILE(IN_FILE_NAME)
) slave_axis_stim ( .m_axis_aclk(tb_stim_clk), .m_axis_arstn(tb_stim_rstn),
```

Read a file and output to a SLAVE AXIS interface from the master.

master_axis_stim

Write a file from the input from a MASTER AXIS interface to the slave.