tm_stim_axis.v

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DATES

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INFORMATION

Brief

All modules for AXIS test bench top are here. There will be loop of tests the axis core must pass. In these tests is where the end user must alter the checks if the input does not equal the output. As these were designed with a FIFO in mind.

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slave_axis_stimulus

```
module slave_axis_stimulus #(
parameter
BUS_WIDTH
 =
1,
parameter
USER_WIDTH
 =
1,
```

```
parameter
DEST_WIDTH
 =
1,
parameter
BYTE_SWAP
 =
0,
parameter
FILE
 =
"test.bin"
) ( input m_axis_aclk, input m_axis_arstn, output reg m_axis_tvalid, input
```

Simulator core to read file data, and output it over master axis dut.

Parameters

BUS_WIDTH parameter	bus width in bytes for data bus
USER_WIDTH parameter	user width in bits
DEST_WIDTH parameter	dest width in bits
BYTE_SWAP parameter	swap bytes fed to the DUT
FILE parameter	input file name

Ports

m_axis_aclk	master axis clock
m_axis_arstn	master axis negative reset
m_axis_tvalid	master axis data valid active high
m_axis_tready	master axis, is the input device ready?
m_axis_tdata	master axis data input.
m_axis_tkeep	master axis byte indicator
m_axis_tlast	master axis data is last word
m_axis_tuser	master axis user defined
m_axis_tdest	master axis desitination
eof	end of input file has been reached.

master_axis_stimulus

```
module master_axis_stimulus #(
parameter
BUS_WIDTH
 =
1,
parameter
USER_WIDTH
 =
1,
```

```
parameter
DEST_WIDTH
 =
1,
parameter
RAND_READY
 =
0,
parameter
FILE
 =
"out.bin"
) ( input s_axis_aclk, input s_axis_arstn, input s_axis_tvalid, output reg
```

Simulator core to write file data, from input over slave axis dut. This module will keep a constant ready to the dut.

Parameters

BUS_WIDTH parameter	bus width in bytes for data bus
USER_WIDTH parameter	user width in bits
DEST_WIDTH parameter	dest width in bits
RAND_READY parameter	random ready if set anything other than 0
FILE parameter	output file name

Ports

s_axis_aclk	slave axis clock
s_axis_arstn	slave axis negative reset
s_axis_tvalid	slave data valid
s_axis_tready	slave ready
s_axis_tdata	slave data
s_axis_tkeep	slave keep
s_axis_tlast	slave last word of data
s_axis_tuser	slave user port
s_axis_tdest	slave destination port
eof	end of file will trigger $finish to end sim