axis_tiny_fifo.v

AUTHORS

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DATES

2021/06/04

INFORMATION

Brief

AXIS TINY FIFO, uses combinatorial logic to provide back pressure.

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axis_tiny_fifo

```
module axis_tiny_fifo #(
parameter
FIFO_DEPTH
  =
4,
parameter
BUS_WIDTH
  =
8
) ( input aclk, input arstn, output [(BUS_WIDTH*8)-1:0] m_axis_tdata, output
```

AXIS fifo that uses a shift register to buffer data. This Adds latency to the design in the amount of the FIFO_DEPTH. Though if the destination isn't ready it will build up data to that FIFO_DEPTH and overwrite any

non-valid data inserted.

Parameters

FIFO_DEPTH parameter	Number of transactions to buffer.
BUS_WIDTH parameter	Width of the input/output bus in bytes.

Ports

aclk	Clock for AXIS
arstn	Negative reset for AXIS
m_axis_tdata	Output data
m_axis_tvalid	When active high the output data is valid
m_axis_tlast	Indicates last word in stream.
m_axis_tready	When set active high the output device is ready for data.
s_axis_tdata	Input data
s_axis_tvalid	When set active high the input data is valid
s_axis_tlast	Is this the last word in the stream (active high).
s_axis_tready	When active high the device is ready for input data.

VARIABLES

s_axis_tready

```
assign s_axis_tready = (
                                                                    ~&
reg_valid_buffer ||
m_axis_tready
) & arstn
```

If any valid is 0, we are ready for data

m_axis_tdata

```
assign m_axis_tdata = reg_data_buffer[0]
```

assign output data as soon as its ready

m_axis_tvalid

```
assign m_axis_tvalid = reg_valid_buffer[0]
```

assign output data as soon as its ready

m_axis_tlast

```
assign m_axis_tlast = reg_last_buffer[0]
```

assign output data as soon as its ready