AXIS_UART

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Contents

1 Usage

1.1 Introduction

UART core for TTL rs232 software mode data communications. Handshake in progress. This contains its own internal baud rate generator that creates an enable to allow data output or sampling. Baud clock and aclk can be the same clock.

RTS/CTS is implemented, but untested at the moment.

1.2 Dependencies

The following are the dependencies of the cores.

- fusesoc 2.X
- iverilog (simulation)
- cocotb (simulation)

1.2.1 fusesoc_info Depenecies

- dep
  - AFRL:clock:mod_clock_ena_gen:1.1.1
  - AFRL:utility:helper:1.0.0
  - AFRL:simple:piso:1.0.0
  - AFRL:simple:sipo:1.0.0

1.3 In a Project

This core connects a UART to the AXIS bus. Meaning this is a streaming device only. Connect the RX/TX to the UART in question and connect the AXIS to its intended endpoints.

2 Architecture

This core is made up of other cores that are documented in detail in there source. The cores this is made up of are the,

- **axis_uart** Interface with UART and present the data over AXIS interface (see core for documentation).
- **mod_clk_gen_ena** Generates enable pulses at the baud rate based on the input clock.

- **PISO** Take parallel input data and output in a serial fashion.
- **SIPO** Take serial data input and output parallel data.

3 Building

The AXIS UART is written in Verilog 2001. It should synthesize in any modern FPGA software. The core comes as a fusesoc packaged core and can be included in any other core. Be sure to make sure you have meet the dependencies listed in the previous section. Linting is performed by verible using the lint target.

3.1 fusesoc

Fusesoc is a system for building FPGA software without relying on the internal project management of the tool. Avoiding vendor lock in to Vivado or Quartus. These cores, when included in a project, can be easily integrated and targets created based upon the end developer needs. The core by itself is not a part of a system and should be integrated into a fusesoc based system. Simulations are setup to use fusesoc and are a part of its targets.

3.2 Source Files

3.2.1 fusesoc_info File List

- src
  - src/axis_uart.v
- tb_cocotb_full
  - 'tb/tb_cocotb_full.py': 'file_type': 'user', 'copyto': '.'
  - 'tb/tb_cocotb_full.v': 'file_type': 'verilogSource'

3.3 Targets

3.3.1 fusesoc_info Targets

- default

  Info: Default for IP intergration.

- lint

  Info: Lint with Verible

- sim_cocotb_full

    Info: Cocotb unit tests

3.4 Directory Guide

Below highlights important folders from the root of the directory.

1. **docs** Contains all documentation related to this project.
    - **manual** Contains user manual and github page that are generated from the latex sources.
2. **src** Contains source files for the core
3. **tb** Contains test bench files for iverilog and cocotb
    - **cocotb** testbench files

4 Simulation

There are a few different simulations that can be run for this core.

4.1 cocotb

To use the cocotb tests you must install the following python libraries.

```
$ pip install cocotb
$ pip install cocotbext-axi
```

Each module has a cocotb based simulation. These use the cocotb extensions made by Alex. The two extensions used are cocotbext-axi and cocotbext-uart. These provide outside verification of the implimentation.

- **sim_cocotb_full** Standard simulation of TX/RX passing data to and from cocotbexts.

Then you must use the cocotb sim target. The targets above can be run with various bus and fifo parameters.

```
$ fusesoc run --target AFRL:device_converter:axis_uart:1.0.0
```

5 Module Documentation

- **axis_uart** Wrapper for all UART modules to create a singular device to interface with.

axis_uart.v

AUTHORS

JAY CONVERTINO

DATES

2021/06/24

INFORMATION

Brief

V2 upgrade to UART that will create a full UART compatible IP DTE device.

License MIT

axis_uart

```
module axis_uart #(
parameter
CLOCK_SPEED
 =
2000000,
parameter
BUS_WIDTH
 =
1,
parameter
RX_BAUD_DELAY
 =
0,
parameter
```

```
 TX_BAUD_DELAY
  =
 0
) ( input wire aclk, input wire arstn, input wire [ 2:0] reg_parity, input w
```

AXIS UART DTE, a UART with AXI Streaming interface.

Parameters

CLOCK_SPEED parameter	This is the aclk frequency in Hz
BUS_WIDTH parameter	AXIS data bus width in bytes.
RX_BAUD_DELAY parameter	DELAY RX internal baud rate by CLOCK_SPEED number of cycles.
TX_BAUD_DELAY parameter	DELAY TX internal baud rate by CLOCK_SPEED number of cycles.

Ports

aclk	Clock for AXIS
arstn	Negative reset for AXIS
reg_parity	Set the parity type, 0 = none, 1 = odd, 2 = even, 3 = mark , 4 = space
reg_stop_bits	Set the number of stop bits (0 to 3, 0=0, 1=1, 2=2, 3=??).
reg_data_bits	Set the number of data bits up to the BUS_WIDTH*8 (1 to 16, all values are biased by 1, 0+1=1).
reg_baud_rate	Frequency in Hz for the output/input data rate. This can be up to half of AXIS clock (any 32 bit unsigned value in Hz).
reg_istatus_bits	Collection of input status bits for dtr,cts,dts,dcd.
reg_ostatus_bits	Collection of output status bits for rx/tx frame, rx parity.
s_axis_tdata	Input data for UART TX.
s_axis_tvalid	When set active high the input data is valid
s_axis_tready	When active high the device is ready for input data.
m_axis_tdata	Output data from UART RX
m_axis_tvalid	When active high the output data is valid
m_axis_tready	When set active high the output device is ready for data.
uart_clk	Clock used for BAUD rate generation
uart_rstn	Negative reset for UART, for anything clocked on uart_clk
tx	transmit for UART (output to RX)
rx	receive for UART (input from TX)
rts	request to send is a loop with CTS
dtr	data terminal ready
cts	clear to send is a loop with RTS
ri	ring indicator

INSTANTIATED MODULES

uart_baud_gen_tx

```
mod_clock_ena_gen #(
```

```
                                                                                .
 CLOCK_SPEED(CLOCK_SPEED),
                                                                                .
 DELAY(TX_BAUD_DELAY)
) uart_baud_gen_tx ( .clk(aclk), .rstn(arstn), .start0(1'b1), .clr(s_axis_t
```

Generates TX BAUD rate for UART modules using modulo divide method.

uart_baud_gen_rx

```
 mod_clock_ena_gen #(
                                                                                .
 CLOCK_SPEED(CLOCK_SPEED),
                                                                                .
 DELAY(RX_BAUD_DELAY)
) uart_baud_gen_rx ( .clk(aclk), .rstn(arstn), .start0(1'b0), .clr(r_rx_uart
```

Generates RX BAUD rate for UART modules using modulo divide method.

inst_piso

```
 piso #(
                                                                                .
 BUS_WIDTH(BUS_WIDTH),
                                                                                .
 DEFAULT_RESET_VAL(1),
                                                                                .
 DEFAULT_SHIFT_VAL(1)
) inst_piso ( .clk(aclk), .rstn(arstn), .ena(s_tx_uart_ena), .rev(1'b1), .l
```

take axis input parallel data at bus size, and output the word to the UART TX

inst_sipo

```
 sipo #(
                                                                                .
 BUS_WIDTH(BUS_WIDTH)
 ) inst_sipo ( .clk(aclk), .rstn(arstn), .ena(s_rx_uart_ena), .rev(1'b1), .
```

take UART RX data, and output the word to the parallel data bus.

tb_cocotb.py

AUTHORS

JAY CONVERTINO

DATES

2024/12/09

INFORMATION

Brief

Cocotb test bench

License MIT

FUNCTIONS

random_bool

```
def random_bool()
```

Return a infinte cycle of random bools

Returns: List

start_clock

```
def start_clock(
dut
)
```

Start the simulation clock generator.

Parameters

dut Device under test passed from cocotb test function

reset_dut

```
async def reset_dut(
dut
)
```

Cocotb coroutine for resets, used with await to make sure system is reset.

single_word

```
@cocotb.test()
async def single_word(
dut
)
```

Coroutine that is identified as a test routine. This routine tests for writing a single word, and then reading a single word.

Parameters

dut Device under test passed from cocotb.

tb_cocotb.v

AUTHORS

JAY CONVERTINO

DATES

2025/01/21

INFORMATION

Brief

Test bench wrapper for cocotb

License MIT

tb_cocotb

```
module tb_cocotb #(
parameter
CLOCK_SPEED
 =
2000000,
parameter
BUS_WIDTH
 =
1,
parameter
RX_BAUD_DELAY
 =
0,
parameter
```

```
 TX_BAUD_DELAY
  =
 0
) ( input wire aclk, input wire arstn, input wire [ 2:0] reg_parity, input w
```

Test bench for axis uart.

AXIS UART DTE, a UART with AXI Streaming interface.

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CLOCK_SPEED parameter	This is the aclk frequency in Hz
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m_axis_tvalid	When active high the output data is valid
m_axis_tready	When set active high the output device is ready for data.
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dtr	data terminal ready
cts	clear to send is a loop with RTS
ri	ring indicator

INSTANTIATED MODULES

dut

```
axis_uart #(
                                                                                .
CLOCK_SPEED(CLOCK_SPEED),
                                                                                .
BUS_WIDTH(BUS_WIDTH),
                                                                                .
RX_BAUD_DELAY(0),
                                                                                .
TX_BAUD_DELAY(0)
) dut ( .aclk(aclk), .arstn(arstn), .reg_parity(reg_parity), .reg_stop_bits(
```

Device under test, axis_uart