

tb_cocotb_wishbone_standard.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

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tb_cocotb

```
module tb_cocotb #(
  parameter
    ADDRESS_WIDTH
    =
    32,
  parameter
    BUS_WIDTH
    =
    4,
  parameter
    CLOCK_SPEED
    =
    100000000
)
```

```
input
clk,
input
rst,
input
s_wb_cyc,
input
s_wb_stb,
input
s_wb_we,
input
[ADDRESS_WIDTH-1:0]
s_wb_addr,
input
[BUS_WIDTH*8-1:0]
s_wb_data_i,
input
[BUS_WIDTH-1:0]
s_wb_sel,
output
s_wb_ack,
output
[BUS_WIDTH*8-1:0]
s_wb_data_o,
output
s_wb_err,
input
[1:0]
rx_diff,
output
[1:0]
tx_diff,
output
tx_active,
output
irq
)
```

Wishbone Stanard based 1553 communications device.

Parameters

ADDRESS_WIDTH	Width of the address bus in bits, max 32 bit.
BUS_WIDTH	Width of the data bus in bytes.
CLOCK_SPEED	This is the aclk frequency in Hz

Ports

clk	Clock for all devices in the core
rst	Positive reset
s_wb_cyc	Bus Cycle in process
s_wb_stb	Valid data transfer cycle
s_wb_we	Active High write, low read

s_wb_addr input [ADDRESS_WIDTH- 1:0]	Bus address
s_wb_data_i input [BUS_WIDTH* 8- 1:0]	Input data
s_wb_sel input [BUS_WIDTH- 1:0]	Device Select
s_wb_ack output [BUS_WIDTH- 1:0]	Bus transaction terminated
s_wb_data_o output [BUS_WIDTH* 8- 1:0]	Output data
s_wb_err output [BUS_WIDTH* 8- 1:0]	Active high when a bus error is present
rx_diff input [1:0]	Input differential signal for 1553 bus
tx_diff output [1:0]	Output differential signal for 1553 bus
tx_active output [1:0]	Enable output of differential signal (for signal switching on 1553 module)
irq output [1:0]	Interrupt when data is received

INSTANTIATED MODULES

dut

Device under test, wishbone_standard_1553