

tb_cocotb_up.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

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tb_cocotb

```
module tb_cocotb #(
  parameter
    ADDRESS_WIDTH
    =
    32,
  parameter
    BUS_WIDTH
    =
    4,
  parameter
    CLOCK_SPEED
    =
    100000000
)
```

```
(
    input
    clk,
    input
    rstn,
    input
    up_rreq,
    output
    up_rack,
    input
    [ADDRESS_WIDTH-(BUS_WIDTH/2)-1:0]
    up_raddr,
    output
    [(BUS_WIDTH*8)-1:0]
    up_rdata,
    input
    up_wreq,
    output
    up_wack,
    input
    [ADDRESS_WIDTH-(BUS_WIDTH/2)-1:0]
    up_waddr,
    input
    [(BUS_WIDTH*8)-1:0]
    up_wdata,
    input
    [1:0]
    rx_diff,
    output
    [1:0]
    tx_diff,
    output
    tx_active,
    output
    irq
)
```

uP 1553 testbench

Parameters

ADDRESS_WIDTH parameter	Width of the uP address port, max 32 bit.
BUS_WIDTH parameter	Width of the uP bus data port.
CLOCK_SPEED parameter	This is the ack frequency in Hz

Ports

clk input	Clock for all devices in the core
rstn input	Negative reset
up_rreq input	uP bus read request
up_rack output	uP bus read ack
up_raddr input [ADDRESS_WIDTH-(BUS_WIDTH/ 2)- 1:0]	uP bus read address
up_rdata output [(BUS_WIDTH* 8)- 1:0]	uP bus read data

up_wreq input [(BUS_WIDTH* 8)- 1:0]	uP bus write request
up_wack output [(BUS_WIDTH* 8)- 1:0]	uP bus write ack
up_waddr input [ADDRESS_WIDTH-(BUS_WIDTH/ 2)- 1:0]	uP bus write address
up_wdata input [(BUS_WIDTH* 8)- 1:0]	uP bus write data
rx_diff input [1:0]	Input differential signal for 1553 bus
tx_diff output [1:0]	Output differential signal for 1553 bus
tx_active output [1:0]	Enable output of differential signal (for signal switching on 1553 module)
irq output [1:0]	Interrupt when data is received

INSTANTIATED MODULES

dut

Device under test, up_1553