

# tb\_cocotb\_axi\_lite.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Test bench wrapper for cocotb

### License MIT

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## tb\_cocotb

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```
module tb_cocotb #(
  parameter
    ADDRESS_WIDTH
    =
    32,
  parameter
    BUS_WIDTH
    =
    4,
  parameter
    CLOCK_SPEED
    =
    100000000
)
```

```

input
aclk,
input
arstn,
input
s_axi_awvalid,
input
[ADDRESS_WIDTH-1:0]
s_axi_awaddr,
input
[ 2:0]
s_axi_awprot,
output
s_axi_awready,
input
s_axi_wvalid,
input
[BUS_WIDTH*8-1:0]
s_axi_wdata,
input
[ 3:0]
s_axi_wstrb,
output
s_axi_wready,
output
s_axi_bvalid,
output
[ 1:0]
s_axi_bresp,
input
s_axi_bready,
input
s_axi_arvalid,
input
[ADDRESS_WIDTH-1:0]
s_axi_araddr,
input
[ 2:0]
s_axi_arprot,
output
s_axi_arready,
output
s_axi_rvalid,
output
[BUS_WIDTH*8-1:0]
s_axi_rdata,
output
[ 1:0]
s_axi_rresp,
input
s_axi_rready,
input
[1:0]
rx_diff,
output
[1:0]
tx_diff,
output
tx_active,
output
irq
)

```

(

AXI Lite slave to AXI Lite 1553 DUT

## Parameters

<b>ADDRESS_WIDTH</b> parameter	Width of the axi address bus, max 32 bit.
<b>BUS_WIDTH</b> parameter	Width in bytes of the data bus.
<b>CLOCK_SPEED</b> parameter	This is the aclk frequency in Hz

## Ports

<b>aclk</b> input	Clock for all devices in the core
<b>arstn</b> input	Negative reset
<b>s_axi_awvalid</b> input	Axi Lite aw valid
<b>s_axi_awaddr</b> input [ADDRESS_WIDTH- 1:0]	Axi Lite aw addr
<b>s_axi_awprot</b> input [2:0]	Axi Lite aw prot
<b>s_axi_awready</b> output [2:0]	Axi Lite aw ready
<b>s_axi_wvalid</b> input [2:0]	Axi Lite w valid
<b>s_axi_wdata</b> input [BUS_WIDTH* 8- 1:0]	Axi Lite w data
<b>s_axi_wstrb</b> input [3:0]	Axi Lite w strb
<b>s_axi_wready</b> output [3:0]	Axi Lite w ready
<b>s_axi_bvalid</b> output [3:0]	Axi Lite b valid
<b>s_axi_bresp</b> output [1:0]	Axi Lite b resp
<b>s_axi_bready</b> input [1:0]	Axi Lite b ready
<b>s_axi_arvalid</b> input [1:0]	Axi Lite ar valid
<b>s_axi_araddr</b> input [ADDRESS_WIDTH- 1:0]	Axi Lite ar addr
<b>s_axi_arprot</b> input [2:0]	Axi Lite ar prot
<b>s_axi_arready</b> output [2:0]	Axi Lite ar ready
<b>s_axi_rvalid</b> output [2:0]	Axi Lite r valid
<b>s_axi_rdata</b> output [BUS_WIDTH* 8- 1:0]	Axi Lite r data
<b>s_axi_rresp</b> output [1:0]	Axi Lite r resp
<b>s_axi_rready</b> input [1:0]	Axi Lite r ready
<b>rx_diff</b> input [1:0]	Input differential signal for 1553 bus

<b>tx_diff</b>	Output differential signal for 1553 bus
output [1:0]	
<b>tx_active</b>	Enable output of differential signal (for signal switching on 1553 module)
output [1:0]	
<b>irq</b>	Interrupt when data is received
output [1:0]	

## INSTANTIATED MODULES

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Device under test, axi\_lite\_1553