tb_cocotb_axi_lite.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

License MIT

tb_cocotb

```
module tb_cocotb #(
parameter
ADDRESS_WIDTH
 =
32,
parameter
BUS_WIDTH
 =
4,
parameter
CLOCK_SPEED
 =
100000000
)
```

```
                                                                    (
input
aclk,
input
arstn,
input
s_axi_awvalid,
input
 [ADDRESS_WIDTH-1:0]
s_axi_awaddr,
input
 [ 2:0]
s_axi_awprot,
output
s_axi_awready,
input
s_axi_wvalid,
input
 [BUS_WIDTH*8-1:0]
s_axi_wdata,
input
 [ 3:0]
s_axi_wstrb,
output
s_axi_wready,
output
s_axi_bvalid,
output
 [ 1:0]
s_axi_bresp,
input
s_axi_bready,
input
s_axi_arvalid,
input
 [ADDRESS_WIDTH-1:0]
s_axi_araddr,
input
 [ 2:0]
s_axi_arprot,
output
s_axi_arready,
output
s_axi_rvalid,
output
 [BUS_WIDTH*8-1:0]
s_axi_rdata,
output
 [ 1:0]
s_axi_rresp,
input
s_axi_rready,
input
 [1:0]
rx_diff,
output
 [1:0]
tx_diff,
output
tx_active,
output
irq
)
```

AXI Lite slave to AXI Lite 1553 DUT

Parameters

ADDRESS_WIDTH parameter	Width of the axi address bus, max 32 bit.
BUS_WIDTH parameter	Width in bytes of the data bus.
CLOCK_SPEED parameter	This is the aclk frequency in Hz

Ports

aclk input	Clock for all devices in the core
arstn input	Negative reset
s_axi_awvalid input	Axi Lite aw valid
s_axi_awaddr input [ADDRESS_WIDTH- 1:0]	Axi Lite aw addr
s_axi_awprot input [2:0]	Axi Lite aw prot
s_axi_awready output [2:0]	Axi Lite aw ready
s_axi_wvalid input [2:0]	Axi Lite w valid
s_axi_wdata input [BUS_WIDTH* 8- 1:0]	Axi Lite w data
s_axi_wstrb input [3:0]	Axi Lite w strb
s_axi_wready output [3:0]	Axi Lite w ready
s_axi_bvalid output [3:0]	Axi Lite b valid
s_axi_bresp output [1:0]	Axi Lite b resp
s_axi_bready input [1:0]	Axi Lite b ready
s_axi_arvalid input [1:0]	Axi Lite ar valid
s_axi_araddr input [ADDRESS_WIDTH- 1:0]	Axi Lite ar addr
s_axi_arprot input [2:0]	Axi Lite ar prot
s_axi_arready output [2:0]	Axi Lite ar ready
s_axi_rvalid output [2:0]	Axi Lite r valid
s_axi_rdata output [BUS_WIDTH* 8- 1:0]	Axi Lite r data
s_axi_rresp output [1:0]	Axi Lite r resp
s_axi_rready input [1:0]	Axi Lite r ready
rx_diff input [1:0]	Input differential signal for 1553 bus

tx_diff `output [1:0]`	Output differential signal for 1553 bus
tx_active `output [1:0]`	Enable output of differential signal (for signal switching on 1553 module)
irq `output [1:0]`	Interrupt when data is received

INSTANTIATED MODULES

dut

Device under test, axi_lite_1553