tb_cocotb_wishbone_standard.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

License MIT

tb_cocotb

```verilog
module tb_cocotb #(
parameter
ADDRESS_WIDTH
 =
32,
parameter
BUS_WIDTH
 =
4,
parameter
CLOCK_SPEED
 =
100000000,
parameter
```

```
    SAMPLE_RATE
      =
    2000000,
    parameter
    BIT_SLICE_OFFSET
      =
    0,
    parameter
    INVERT_DATA
      =
    0,
    parameter
    SAMPLE_SELECT
      =
    0
) ( input clk, input rst, input s_wb_cyc, input s_wb_stb, input s_wb_we, inp
```

Wishbone Stanard based 1553 communications device.

Parameters

ADDRESS_WIDTH parameter	Width of the address bus in bits, max 32 bit.
BUS_WIDTH parameter	Width of the data bus in bytes.
CLOCK_SPEED parameter	This is the aclk frequency in Hz
SAMPLE_RATE parameter	Rate of in which to sample the 1553 bus. Must be 2 MHz or more and less than aclk. This is in Hz. BIT_SLICE_OFFSET- Adjust where the sample is taken from the input.
INVERT_DATA parameter	Invert all 1553 bits coming in and out.
SAMPLE_SELECT parameter	Adjust where in the array of samples to select a bit.

Ports

clk	Clock for all devices in the core
rst	Positive reset
s_wb_cyc	Bus Cycle in process
s_wb_stb	Valid data transfer cycle
s_wb_we	Active High write, low read
s_wb_addr	Bus address
s_wb_data_i	Input data
s_wb_sel	Device Select
s_wb_ack	Bus transaction terminated
s_wb_data_o	Output data
s_wb_err	Active high when a bus error is present
i_diff	Input differential signal for 1553 bus
o_diff	Output differential signal for 1553 bus
en_o_diff	Enable output of differential signal (for signal switching on 1553 module)
irq	Interrupt when data is received

INSTANTIATED MODULES

dut

```
wishbone_standard_1553 #(
                                                          .
ADDRESS_WIDTH(ADDRESS_WIDTH),
                                                          .
BUS_WIDTH(BUS_WIDTH),
                                                          .
CLOCK_SPEED(CLOCK_SPEED),
                                                          .
SAMPLE_RATE(SAMPLE_RATE),
                                                          .
BIT_SLICE_OFFSET(BIT_SLICE_OFFSET),
                                                          .
INVERT_DATA(INVERT_DATA),
                                                          .
SAMPLE_SELECT(SAMPLE_SELECT)
) dut ( .clk(clk), .rst(rst), .s_wb_cyc(s_wb_cyc), .s_wb_stb(s_wb_stb), .s_w
```

Device under test, wishbone_standard_1553