tb_wishbone_slave.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench for wishbone_slave

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tb_wishbone_slave

```verilog
module tb_wishbone_slave #(
parameter
ADDRESS_WIDTH
  =
32,
parameter
BUS_WIDTH
  =
4,
parameter
DEPTH
  =
512,
parameter
```

```
  RAM_TYPE
   =
  "block",
  parameter
  HEX_FILE
   =
  ""
)
```

Test bench for wishbone slave

Parameters

ADDRESS_WIDTH   Width of the axi address bus in bits.
parameter

BUS_WIDTH   Bus width for data paths in bytes.
parameter

DEPTH   Depth of the RAM in terms of data width words.
parameter

RAM_TYPE   Used to set the ram_style atribute.
parameter

HEX_FILE   Hex file to write to RAM.
parameter

inst_dc_block_ram

Module instance of dc_block_ram