

wishbone_classic_block_ram.v

AUTHORS

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DATES

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INFORMATION

Brief

Wishbone classic block RAM core.

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wishbone_classic_block_ram

```
module wishbone_classic_block_ram #(
    parameter
    ADDRESS_WIDTH
    =
    32,
    parameter
    BUS_WIDTH
    =
    4,
    parameter
    DEPTH
```

```

    =
    512,
    parameter
    RAM_TYPE
    =
    "block",
    parameter
    HEX_FILE
    =
    ""
) ( input clk, input rst, input s_wb_cyc, input s_wb_stb, input s_wb_we, inp

```

Wishbone classic block RAM core.

Parameters

ADDRESS_WIDTH parameter	Width of the axi address bus in bits.
BUS_WIDTH parameter	Bus width for data paths in bytes.
DEPTH parameter	Depth of the RAM in terms of data width words.
RAM_TYPE parameter	Used to set the ram_style attribute.
HEX_FILE parameter	Hex file to write to RAM.

Ports

clk	Clock for all devices in the core
rst	Positive reset
s_wb_cyc	Bus Cycle in process
s_wb_stb	Valid data transfer cycle
s_wb_we	Active High write, low read
s_wb_addr	Bus address
s_wb_data_i	Input data
s_wb_sel	Device Select
s_wb_bte	Burst Type Extension
s_wb_cti	Cycle Type
s_wb_ack	Bus transaction terminated
s_wb_data_o	Output data
s_wb_err	Active high when a bus error is present

c_PWR_RAM

```

localparam c_PWR_RAM = clogb2(
    DEPTH
)

```

power of 2 conversion of DEPTH

c_RAM_DEPTH

```
localparam c_RAM_DEPTH = 2 ** c_PWR_RAM
```

create RAM depth based on power of two depth size.

up_rreq

```
wire up_rreq
```

uP read bus request

up_rack

```
reg up_rack
```

uP read bus acknowledge

up_raddr

```
wire [ADDRESS_WIDTH-(  
ADDRESS_WIDTH  
  
16  
)-1:0] up_raddr
```

uP read bus address

up_rdata

```
wire [(  
BUS_WIDTH*4  
)-1:0] up_rdata
```

uP read bus request

up_wreq

```
wire up_wreq
```

uP write bus request

up_wack

```
reg up_wack
```

uP write bus acknowledge

