

tb_wishbone_cocotb.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

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tb_cocotb

```
module tb_cocotb #(
  parameter
  ADDRESS_WIDTH
  =
  32,
  parameter
  BUS_WIDTH
  =
  4,
  parameter
  DEPTH
  =
  512,
  parameter
```

```
RAM_TYPE
=
"block",
parameter
HEX_FILE
=
""
) ( input clk, input rst, input s_wb_cyc, input s_wb_stb, input s_wb_we, input
```

Test bench for wishbone.

Parameters

ADDRESS_WIDTH parameter	Width of the axi address bus in bits.
BUS_WIDTH parameter	Bus width for data paths in bytes.
DEPTH parameter	Depth of the RAM in terms of data width words.
RAM_TYPE parameter	Used to set the ram_style attribute.
HEX_FILE parameter	Hex file to write to RAM.

Ports

clk	Clock for all devices in the core
rst	Positive reset
s_wb_cyc	Bus Cycle in process
s_wb_stb	Valid data transfer cycle
s_wb_we	Active High write, low read
s_wb_addr	Bus address
s_wb_data_i	Input data
s_wb_sel	Device Select
s_wb_bte	Burst Type Extension
s_wb_cti	Cycle Type
s_wb_ack	Bus transaction terminated
s_wb_data_o	Output data
s_wb_err	Active high when a bus error is present

INSTANTIATED MODULES

dut

```
wishbone_classic_block_ram #(
    ADDRESS_WIDTH(ADDRESS_WIDTH),
    BUS_WIDTH(BUS_WIDTH),
    DEPTH(DEPTH),
    RAM_TYPE(RAM_TYPE),
```

```

    HEX_FILE(HEX_FILE)
) dut ( .clk(clk), .rst(rst), .s_wb_cyc(s_wb_cyc), .s_wb_stb(s_wb_stb), .s_wb

```

Device under test, wishbone_classic_block_ram