

wishbone_classic_block_ram.v

AUTHORS

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DATES

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INFORMATION

Brief

Wishbone classic block RAM core.

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wishbone_classic_block_ram

```
module wishbone_classic_block_ram #(
  parameter
  ADDRESS_WIDTH
  =
  32,
  parameter
  BUS_WIDTH
  =
  4,
  parameter
  DEPTH
```

```

    =
    512,
    parameter
    RAM_TYPE
    =
    "block",
    parameter
    HEX_FILE
    =
    ""
) ( input clk, input rst, input s_wb_cyc, input s_wb_stb, input s_wb_we, inp

```

Wishbone classic block RAM core.

Parameters

ADDRESS_WIDTH parameter	Width of the axi address bus in bits.
BUS_WIDTH parameter	Bus width for data paths in bytes.
DEPTH parameter	Depth of the RAM in terms of data width words.
RAM_TYPE parameter	Used to set the ram_style attribute.
HEX_FILE parameter	Hex file to write to RAM.

Ports

clk	Clock for all devices in the core
rst	Positive reset
s_wb_cyc	Bus Cycle in process
s_wb_stb	Valid data transfer cycle
s_wb_we	Active High write, low read
s_wb_addr	Bus address
s_wb_data_i	Input data
s_wb_sel	Device Select
s_wb_bte	Burst Type Extension
s_wb_cti	Cycle Type
s_wb_ack	Bus transaction terminated
s_wb_data_o	Output data
s_wb_err	Active high when a bus error is present

c_PWR_RAM

```

localparam c_PWR_RAM = clogb2(
    DEPTH
)

```

power of 2 conversion of DEPTH

c_RAM_DEPTH

```
localparam c_RAM_DEPTH = 2 ** c_PWR_RAM
```

create RAM depth based on power of two depth size.

up_rreq

```
wire up_rreq
```

uP read bus request

up_rack

```
reg up_rack
```

uP read bus acknowledge

up_raddr

```
wire [ADDRESS_WIDTH-3:0] up_raddr
```

uP read bus address

up_rdata

```
wire [(  
  BUS_WIDTH*4  
)-1:0] up_rdata
```

uP read bus request

up_wreq

```
wire up_wreq
```

uP write bus request

up_wack

```
reg up_wack
```

uP write bus acknowledge

up_waddr

```
wire [ADDRESS_WIDTH-3:0] up_waddr
```

uP write bus address

up_wdata

```
wire [(
BUS_WIDTH*4
)-1:0] up_wdata
```

uP write bus data

INSTANTIATED MODULES

inst_up_wishbone_classic

```
up_wishbone_classic #(
    ADDRESS_WIDTH(ADDRESS_WIDTH),
    BUS_WIDTH(BUS_WIDTH)
) inst_up_wishbone_classic ( .clk(clk), .rst(rst), .s_wb_cyc(s_wb_cyc), .s_wb_data(s_wb_data), .s_wb_err(s_wb_err), .s_wb_ack(s_wb_ack), .s_wb_stb(s_wb_stb), .s_wb_we(s_wb_we), .s_wb_be(s_wb_be), .s_wb_oe(s_wb_oe), .s_wb_ce(s_wb_ce), .s_wb_oe2(s_wb_oe2), .s_wb_oe3(s_wb_oe3), .s_wb_oe4(s_wb_oe4), .s_wb_oe5(s_wb_oe5), .s_wb_oe6(s_wb_oe6), .s_wb_oe7(s_wb_oe7), .s_wb_oe8(s_wb_oe8), .s_wb_oe9(s_wb_oe9), .s_wb_oe10(s_wb_oe10), .s_wb_oe11(s_wb_oe11), .s_wb_oe12(s_wb_oe12), .s_wb_oe13(s_wb_oe13), .s_wb_oe14(s_wb_oe14), .s_wb_oe15(s_wb_oe15), .s_wb_oe16(s_wb_oe16), .s_wb_oe17(s_wb_oe17), .s_wb_oe18(s_wb_oe18), .s_wb_oe19(s_wb_oe19), .s_wb_oe20(s_wb_oe20), .s_wb_oe21(s_wb_oe21), .s_wb_oe22(s_wb_oe22), .s_wb_oe23(s_wb_oe23), .s_wb_oe24(s_wb_oe24), .s_wb_oe25(s_wb_oe25), .s_wb_oe26(s_wb_oe26), .s_wb_oe27(s_wb_oe27), .s_wb_oe28(s_wb_oe28), .s_wb_oe29(s_wb_oe29), .s_wb_oe30(s_wb_oe30), .s_wb_oe31(s_wb_oe31), .s_wb_oe32(s_wb_oe32), .s_wb_oe33(s_wb_oe33), .s_wb_oe34(s_wb_oe34), .s_wb_oe35(s_wb_oe35), .s_wb_oe36(s_wb_oe36), .s_wb_oe37(s_wb_oe37), .s_wb_oe38(s_wb_oe38), .s_wb_oe39(s_wb_oe39), .s_wb_oe40(s_wb_oe40), .s_wb_oe41(s_wb_oe41), .s_wb_oe42(s_wb_oe42), .s_wb_oe43(s_wb_oe43), .s_wb_oe44(s_wb_oe44), .s_wb_oe45(s_wb_oe45), .s_wb_oe46(s_wb_oe46), .s_wb_oe47(s_wb_oe47), .s_wb_oe48(s_wb_oe48), .s_wb_oe49(s_wb_oe49), .s_wb_oe50(s_wb_oe50), .s_wb_oe51(s_wb_oe51), .s_wb_oe52(s_wb_oe52), .s_wb_oe53(s_wb_oe53), .s_wb_oe54(s_wb_oe54), .s_wb_oe55(s_wb_oe55), .s_wb_oe56(s_wb_oe56), .s_wb_oe57(s_wb_oe57), .s_wb_oe58(s_wb_oe58), .s_wb_oe59(s_wb_oe59), .s_wb_oe60(s_wb_oe60), .s_wb_oe61(s_wb_oe61), .s_wb_oe62(s_wb_oe62), .s_wb_oe63(s_wb_oe63), .s_wb_oe64(s_wb_oe64), .s_wb_oe65(s_wb_oe65), .s_wb_oe66(s_wb_oe66), .s_wb_oe67(s_wb_oe67), .s_wb_oe68(s_wb_oe68), .s_wb_oe69(s_wb_oe69), .s_wb_oe70(s_wb_oe70), .s_wb_oe71(s_wb_oe71), .s_wb_oe72(s_wb_oe72), .s_wb_oe73(s_wb_oe73), .s_wb_oe74(s_wb_oe74), .s_wb_oe75(s_wb_oe75), .s_wb_oe76(s_wb_oe76), .s_wb_oe77(s_wb_oe77), .s_wb_oe78(s_wb_oe78), .s_wb_oe79(s_wb_oe79), .s_wb_oe80(s_wb_oe80), .s_wb_oe81(s_wb_oe81), .s_wb_oe82(s_wb_oe82), .s_wb_oe83(s_wb_oe83), .s_wb_oe84(s_wb_oe84), .s_wb_oe85(s_wb_oe85), .s_wb_oe86(s_wb_oe86), .s_wb_oe87(s_wb_oe87), .s_wb_oe88(s_wb_oe88), .s_wb_oe89(s_wb_oe89), .s_wb_oe90(s_wb_oe90), .s_wb_oe91(s_wb_oe91), .s_wb_oe92(s_wb_oe92), .s_wb_oe93(s_wb_oe93), .s_wb_oe94(s_wb_oe94), .s_wb_oe95(s_wb_oe95), .s_wb_oe96(s_wb_oe96), .s_wb_oe97(s_wb_oe97), .s_wb_oe98(s_wb_oe98), .s_wb_oe99(s_wb_oe99), .s_wb_oe100(s_wb_oe100), .s_wb_oe101(s_wb_oe101), .s_wb_oe102(s_wb_oe102), .s_wb_oe103(s_wb_oe103), .s_wb_oe104(s_wb_oe104), .s_wb_oe105(s_wb_oe105), .s_wb_oe106(s_wb_oe106), .s_wb_oe107(s_wb_oe107), .s_wb_oe108(s_wb_oe108), .s_wb_oe109(s_wb_oe109), .s_wb_oe110(s_wb_oe110), .s_wb_oe111(s_wb_oe111), .s_wb_oe112(s_wb_oe112), .s_wb_oe113(s_wb_oe113), .s_wb_oe114(s_wb_oe114), .s_wb_oe115(s_wb_oe115), .s_wb_oe116(s_wb_oe116), .s_wb_oe117(s_wb_oe117), .s_wb_oe118(s_wb_oe118), .s_wb_oe119(s_wb_oe119), .s_wb_oe120(s_wb_oe120), .s_wb_oe121(s_wb_oe121), .s_wb_oe122(s_wb_oe122), .s_wb_oe123(s_wb_oe123), .s_wb_oe124(s_wb_oe124), .s_wb_oe125(s_wb_oe125), .s_wb_oe126(s_wb_oe126), .s_wb_oe127(s_wb_oe127), .s_wb_oe128(s_wb_oe128), .s_wb_oe129(s_wb_oe129), .s_wb_oe130(s_wb_oe130), .s_wb_oe131(s_wb_oe131), .s_wb_oe132(s_wb_oe132), .s_wb_oe133(s_wb_oe133), .s_wb_oe134(s_wb_oe134), .s_wb_oe135(s_wb_oe135), .s_wb_oe136(s_wb_oe136), .s_wb_oe137(s_wb_oe137), .s_wb_oe138(s_wb_oe138), .s_wb_oe139(s_wb_oe139), .s_wb_oe140(s_wb_oe140), .s_wb_oe141(s_wb_oe141), .s_wb_oe142(s_wb_oe142), .s_wb_oe143(s_wb_oe143), .s_wb_oe144(s_wb_oe144), .s_wb_oe145(s_wb_oe145), .s_wb_oe146(s_wb_oe146), .s_wb_oe147(s_wb_oe147), .s_wb_oe148(s_wb_oe148), .s_wb_oe149(s_wb_oe149), .s_wb_oe150(s_wb_oe150), .s_wb_oe151(s_wb_oe151), .s_wb_oe152(s_wb_oe152), .s_wb_oe153(s_wb_oe153), .s_wb_oe154(s_wb_oe154), .s_wb_oe155(s_wb_oe155), .s_wb_oe156(s_wb_oe156), .s_wb_oe157(s_wb_oe157), .s_wb_oe158(s_wb_oe158), .s_wb_oe159(s_wb_oe159), .s_wb_oe160(s_wb_oe160), .s_wb_oe161(s_wb_oe161), .s_wb_oe162(s_wb_oe162), .s_wb_oe163(s_wb_oe163), .s_wb_oe164(s_wb_oe164), .s_wb_oe165(s_wb_oe165), .s_wb_oe166(s_wb_oe166), .s_wb_oe167(s_wb_oe167), .s_wb_oe168(s_wb_oe168), .s_wb_oe169(s_wb_oe169), .s_wb_oe170(s_wb_oe170), .s_wb_oe171(s_wb_oe171), .s_wb_oe172(s_wb_oe172), .s_wb_oe173(s_wb_oe173), .s_wb_oe174(s_wb_oe174), .s_wb_oe175(s_wb_oe175), .s_wb_oe176(s_wb_oe176), .s_wb_oe177(s_wb_oe177), .s_wb_oe178(s_wb_oe178), .s_wb_oe179(s_wb_oe179), .s_wb_oe180(s_wb_oe180), .s_wb_oe181(s_wb_oe181), .s_wb_oe182(s_wb_oe182), .s_wb_oe183(s_wb_oe183), .s_wb_oe184(s_wb_oe184), .s_wb_oe185(s_wb_oe185), .s_wb_oe186(s_wb_oe186), .s_wb_oe187(s_wb_oe187), .s_wb_oe188(s_wb_oe188), .s_wb_oe189(s_wb_oe189), .s_wb_oe190(s_wb_oe190), .s_wb_oe191(s_wb_oe191), .s_wb_oe192(s_wb_oe192), .s_wb_oe193(s_wb_oe193), .s_wb_oe194(s_wb_oe194), .s_wb_oe195(s_wb_oe195), .s_wb_oe196(s_wb_oe196), .s_wb_oe197(s_wb_oe197), .s_wb_oe198(s_wb_oe198), .s_wb_oe199(s_wb_oe199), .s_wb_oe200(s_wb_oe200), .s_wb_oe201(s_wb_oe201), .s_wb_oe202(s_wb_oe202), .s_wb_oe203(s_wb_oe203), .s_wb_oe204(s_wb_oe204), .s_wb_oe205(s_wb_oe205), .s_wb_oe206(s_wb_oe206), .s_wb_oe207(s_wb_oe207), .s_wb_oe208(s_wb_oe208), .s_wb_oe209(s_wb_oe209), .s_wb_oe210(s_wb_oe210), .s_wb_oe211(s_wb_oe211), .s_wb_oe212(s_wb_oe212), .s_wb_oe213(s_wb_oe213), .s_wb_oe214(s_wb_oe214), .s_wb_oe215(s_wb_oe215), .s_wb_oe216(s_wb_oe216), .s_wb_oe217(s_wb_oe217), .s_wb_oe218(s_wb_oe218), .s_wb_oe219(s_wb_oe219), .s_wb_oe220(s_wb_oe220), .s_wb_oe221(s_wb_oe221), .s_wb_oe222(s_wb_oe222), .s_wb_oe223(s_wb_oe223), .s_wb_oe224(s_wb_oe224), .s_wb_oe225(s_wb_oe225), .s_wb_oe226(s_wb_oe226), .s_wb_oe227(s_wb_oe227), .s_wb_oe228(s_wb_oe228), .s_wb_oe229(s_wb_oe229), .s_wb_oe230(s_wb_oe230), .s_wb_oe231(s_wb_oe231), .s_wb_oe232(s_wb_oe232), .s_wb_oe233
```

Module instance of up_wishbone_classic for the Wishbone Classic bus to the uP bus.

inst_dc_block_ram

```
dc_block_ram #(
    RAM_DEPTH(c_RAM_DEPTH),
    BYTE_WIDTH(BUS_WIDTH),
    ADDR_WIDTH(c_PWR_RAM),
    HEX_FILE(HEX_FILE),
    RAM_TYPE(RAM_TYPE)
) inst_dc_block_ram ( .rd_clk(clk), .rd_rstn(~rst), .rd_en(up_rreq), .rd_data
```

Module instance of dc_block_ram that connects to the uP BUS directly.