tb_cocotb_axi_lite.v

AUTHORS

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DATES

2025/04/01

INFORMATION

Brief

Test bench wrapper for cocotb

License MIT

tb_cocotb

```
module tb_cocotb #(
parameter
ADDRESS_WIDTH
 =
32,
parameter
BUS_WIDTH
 =
4,
parameter
GPIO_WIDTH
 =
32,
parameter
```

```
 IRQ_ENABLE
  =
 0
) ( input aclk, input arstn, input s_axi_awvalid, input [ADDRESS_WIDTH-1:0]
```

AXI Lite slave to AXI Lite gpio DUT

Parameters

ADDRESS_WIDTH	Width of the axi address bus, max 32 bit.
parameter		
BUS_WIDTH	Widht of the data bus in bytes.
parameter		
GPIO_WIDTH	Width of the GPIO for inputs and outputs
parameter		
IRQ_ENABLE	Enable interrupt
parameter		

Ports

aclk	Clock for all devices in the core
arstn	Negative reset
s_axi_awvalid	Axi Lite aw valid
s_axi_awaddr	Axi Lite aw addr
s_axi_awprot	Axi Lite aw prot
s_axi_awready	Axi Lite aw ready
s_axi_wvalid	Axi Lite w valid
s_axi_wdata	Axi Lite w data
s_axi_wstrb	Axi Lite w strb
s_axi_wready	Axi Lite w ready
s_axi_bvalid	Axi Lite b valid
s_axi_bresp	Axi Lite b resp
s_axi_bready	Axi Lite b ready
s_axi_arvalid	Axi Lite ar valid
s_axi_araddr	Axi Lite ar addr
s_axi_arprot	Axi Lite ar prot
s_axi_arready	Axi Lite ar ready
s_axi_rvalid	Axi Lite r valid
s_axi_rdata	Axi Lite r data
s_axi_rresp	Axi Lite r resp
s_axi_rready	Axi Lite r ready
irq	Interrupt when data is received
gpio_io_i	Input for GPIO
gpio_io_o	Output for GPIO
gpio_io_t	Tristate for GPIO

INSTANTIATED MODULES

dut

```
 axi_lite_gpio #(
                                                                                .
 ADDRESS_WIDTH(ADDRESS_WIDTH),
                                                                                .
 BUS_WIDTH(BUS_WIDTH),
                                                                                .
 GPIO_WIDTH(GPIO_WIDTH),
                                                                                .
 IRQ_ENABLE(IRQ_ENABLE)
) dut ( .aclk(aclk), .arstn(arstn), .s_axi_awvalid(s_axi_awvalid), .s_axi_av
```

Device under test, axi_lite_gpio