

# up\_gpio.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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uP Core for interfacing with general purpose input/output.

### License MIT

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## up\_gpio

---

```
module up_gpio #(
  parameter
  ADDRESS_WIDTH
  =
  32,
  parameter
  BUS_WIDTH
  =
  4,
  parameter
  GPIO_WIDTH
  =
  32,
  parameter
```

```

    IRQ_ENABLE
    =
    0
) ( input clk, input rstn, input up_rreq, output up_rack, input [ADDRESS_WIDTH-1:0] up_raddr, output [BUS_WIDTH-1:0] up_rdata, output [BUS_WIDTH-1:0] up_wdata, output [BUS_WIDTH-1:0] up_wack, output irq )

```

uP based GPIO device that emulates Xilinx GPIO core.

## Parameters

<b>ADDRESS_WIDTH</b> parameter	Width of the uP address port, max 32 bit.
<b>BUS_WIDTH</b> parameter	Width of the uP bus data port.
<b>GPIO_WIDTH</b> parameter	Width of the GPIO for inputs and outputs
<b>IRQ_ENABLE</b> parameter	Enable interrupt

## Ports

<b>clk</b>	Clock for all devices in the core
<b>rstn</b>	Negative reset
<b>up_rreq</b>	uP bus read request
<b>up_rack</b>	uP bus read ack
<b>up_raddr</b>	uP bus read address
<b>up_rdata</b>	uP bus read data
<b>up_wreq</b>	uP bus write request
<b>up_wack</b>	uP bus write ack
<b>up_waddr</b>	uP bus write address
<b>up_wdata</b>	uP bus write data
<b>irq</b>	Interrupt when data is received
<b>gpio_io_i</b>	Input for GPIO
<b>gpio_io_o</b>	Output for GPIO
<b>gpio_io_t</b>	Tristate for GPIO

## DIVISOR

```
localparam DIVISOR = BUS_WIDTH/2
```

Divide the address register default location for 1 byte access to multi byte access. (register offsets are byte offsets).

## REGISTER INFORMATION

Core has 4 registers at the offsets that follow.

<b>GPIO_DATA</b>	h000
<b>GPIO_TRI</b>	h004
<b>GPIO2_DATA</b>	h008 N/A
<b>GPIO2_TRI</b>	h00C N/A
<b>GIER</b>	h11C

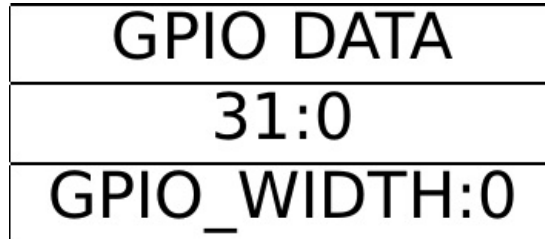
**IP\_ISR**            h120  
**IP\_IER**            h128

## GPIO\_DATA

---

```
localparam GPIO_DATA = 12'h000 >> DIVISOR
```

Defines the address offset for GPIO DATA



Valid bits are from GPIO\_WIDTH:0, input or output data.

## GPIO\_TRI

---

```
localparam GPIO_TRI = 12'h004 >> DIVISOR
```

Defines the address offset for GPIO TRI.



Valid bits are from GPIO\_WIDTH:0, 1 indicates input, 0 is output.

## GPIO2\_DATA

---

```
localparam GPIO2_DATA = 12'h008 >> DIVISOR
```

Defines the address offset for GPIO2 DATA

GPIO2 DATA
31:0
UNUSED

Valid bits are from GPIO2\_WIDTH:0, input or output data. This Register is not implimented in this design.

## GPIO2\_TRI

```
localparam GPIO2_TRI = 12'h00C >> DIVISOR
```

Defines the address offset for GPIO2 TRI.

GPIO2 TRI
31:0
UNUSED

Valid bits are from GPIO2\_WIDTH:0, 1 indicates input, 0 is output. This register is not implimented in this design.

## GIER

```
localparam GIER = 12'h11C >> DIVISOR
```

Defines the address offset for GIER.

GIER	
31	30:0
Global IRQ Ena	UNUSED

Bit 31 is the Global interrupt enable. Write a 1 to enable interrupts.

## IP\_ISR

```
localparam IP_ISR = 12'h120 >> DIVISOR
```

Defines the address offset for IP\_ISR.

IP ISR	
31:1	0
UNUSED	IRQ Status

Bit 0 is GPIO IRQ status, On write this will toggle(acknowledge) the interrupt.

## IP\_IER

---

```
localparam IP_IER = 12'h128 >> DIVISOR
```

Defines the address offset to set the control bits.

IP IER	
31:1	0
UNUSED	IRQ Ena

Bit 0 is GPIO IRQ enable interrupt. Write a 1 to bit 0 to enable interrupt.