

# tb\_cocotb\_wishbone\_standard.v

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## AUTHORS

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JAY CONVERTINO

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## DATES

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## INFORMATION

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### Brief

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Test bench wrapper for cocotb

### License MIT

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## tb\_cocotb

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```
module tb_cocotb #(
  parameter
    ADDRESS_WIDTH
    =
    32,
  parameter
    BUS_WIDTH
    =
    4,
  parameter
    WORD_WIDTH
    =
    4,
  parameter
```

```

CLOCK_SPEED
=
100000000,
parameter
SELECT_WIDTH
=
16,
parameter
DEFAULT_RATE_DIV
=
0,
parameter
DEFAULT_CPOL
=
0,
parameter
DEFAULT_CPHA
=
0
)

input
clk,
input
rst,
input
s_wb_cyc,
input
s_wb_stb,
input
s_wb_we,
input
[ADDRESS_WIDTH-1:0]
s_wb_addr,
input
[BUS_WIDTH*8-1:0]
s_wb_data_i,
input
[BUS_WIDTH-1:0]
s_wb_sel,
output
s_wb_ack,
output
[BUS_WIDTH*8-1:0]
s_wb_data_o,
output
s_wb_err,
output
irq,
output
sclk,
output
mosi,
input
miso,
output
[SELECT_WIDTH-1:0]
ss_n
)

```

(

Wishbone Standard based SPI Master device.

## Parameters

**ADDRESS\_WIDTH** Width of the uP address port, max 32 bit.  
parameter

<b>BUS_WIDTH</b> parameter	Width of the uP bus data port(can not be less than 2 bytes, max tested is 4).
<b>WORD_WIDTH</b> parameter	Width of each SPI Master word. This will also set the bits used in the TX/RX data registers. Must be less than or equal to BUS_WIDTH 1 to 4.
<b>CLOCK_SPEED</b> parameter	This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate.
<b>SELECT_WIDTH</b> parameter	Bit width of the slave select, defaults to 16 to match altera spi ip.
<b>DEFAULT_RATE_DIV</b> parameter	Default divider value of the main clock to use for the spi data output clock rate. 0 is 2 (2^(X+1) X is the DEFAULT_RATE_DIV)
<b>DEFAULT_CPOL</b> parameter	Default clock polarity for the core (0 or 1).
<b>DEFAULT_CPHA</b> parameter	Default clock phase for the core (0 or 1).

## Ports

<b>clk</b> input	Clock for all devices in the core
<b>rst</b> input	Positive reset
<b>s_wb_cyc</b> input	Bus Cycle in process
<b>s_wb_stb</b> input	Valid data transfer cycle
<b>s_wb_we</b> input	Active High write, low read
<b>s_wb_addr</b> input [ADDRESS_WIDTH- 1:0]	Bus address
<b>s_wb_data_i</b> input [BUS_WIDTH* 8- 1:0]	Input data
<b>s_wb_sel</b> input [BUS_WIDTH- 1:0]	Device Select
<b>s_wb_ack</b> output [BUS_WIDTH- 1:0]	Bus transaction terminated
<b>s_wb_data_o</b> output [BUS_WIDTH* 8- 1:0]	Output data
<b>s_wb_err</b> output [BUS_WIDTH* 8- 1:0]	Active high when a bus error is present
<b>irq</b> output [BUS_WIDTH* 8- 1:0]	Interrupt when data is received
<b>sclk</b> output [BUS_WIDTH* 8- 1:0]	spi clock, should only drive output pins to devices.
<b>mosi</b> output [BUS_WIDTH* 8- 1:0]	transmit for master output
<b>miso</b> input [BUS_WIDTH* 8- 1:0]	receive for master input
<b>ss_n</b> output [SELECT_WIDTH- 1:0]	slave select output

## INSTANTIATED MODULES

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## **dut**

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Device under test, wishbone\_standard\_spi\_master