# tb_cocotb_up.v

## AUTHORS

### JAY CONVERTINO

## DATES

### 2025/04/29

## INFORMATION

### Brief

Test bench wrapper for cocotb

### License MIT



### tb_cocotb

```
module tb_cocotb #(
parameter
ADDRESS_WIDTH
 =
32,
parameter
BUS_WIDTH
 =
4,
parameter
WORD_WIDTH
 =
4,
parameter
```

```
CLOCK_SPEED
  =
100000000,
parameter
SELECT_WIDTH
  =
16,
parameter
DEFAULT_RATE_DIV
  =
0,
parameter
DEFAULT_CPOL
  =
0,
parameter
DEFAULT_CPHA
  =
0
) ( input clk, input rstn, input up_rreq, output up_rack, input [ADDRESS_WI
```

SPI Master core with axis input/output data. Read/Write is size of BUS_WIDTH bytes. Write activates core for read.

## Parameters

| | |
|---|---|
| **ADDRESS_WIDTH**<br>parameter | Width of the uP address port, max 32 bit. |
| **BUS_WIDTH**<br>parameter | Width of the uP bus data port(can not be less than 2 bytes, max tested is 4). |
| **WORD_WIDTH**<br>parameter | Width of each SPI Master word. This will also set the bits used in the TX/RX data registers. Must be less than or equal to BUS_WIDTH 1 to 4. |
| **CLOCK_SPEED**<br>parameter | This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate. |
| **SELECT_WIDTH**<br>parameter | Bit width of the slave select, defaults to 16 to match altera spi ip. |
| **DEFAULT_RATE_DIV**<br>parameter | Default divider value of the main clock to use for the spi data output clock rate. 0 is 2 (2^(X+1) X is the DEFAULT_RATE_DIV) |
| **DEFAULT_CPOL**<br>parameter | Default clock polarity for the core (0 or 1). |
| **DEFAULT_CPHA**<br>parameter | Default clock phase for the core (0 or 1). |

## Ports

| | |
|---|---|
| **clk** | Clock for all devices in the core |
| **rstn** | Negative reset |
| **up_rreq** | uP bus read request |
| **up_rack** | uP bus read ack |
| **up_raddr** | uP bus read address |
| **up_rdata** | uP bus read data |
| **up_wreq** | uP bus write request |
| **up_wack** | uP bus write ack |
| **up_waddr** | uP bus write address |
| **up_wdata** | uP bus write data |
| **irq** | Interrupt when data is received |
| **sclk** | spi clock, should only drive output pins to devices. |

| | |
|---|---|
| **mosi** | transmit for master output |
| **miso** | receive for master input |
| **ss_n** | slave select output |

## INSTANTIATED MODULES

### dut

```
up_spi_master #(
                                                                                .
ADDRESS_WIDTH(ADDRESS_WIDTH),
                                                                                .
BUS_WIDTH(BUS_WIDTH),
                                                                                .
WORD_WIDTH(WORD_WIDTH),
                                                                                .
CLOCK_SPEED(CLOCK_SPEED),
                                                                                .
SELECT_WIDTH(SELECT_WIDTH),
                                                                                .
DEFAULT_RATE_DIV(DEFAULT_RATE_DIV),
                                                                                .
DEFAULT_CPOL(DEFAULT_CPOL),
                                                                                .
DEFAULT_CPHA(DEFAULT_CPHA)
) dut ( .clk(clk), .rstn(rstn), .up_rreq(up_rreq), .up_rack(up_rack), .up_ra
```

Device under test, up_spi_master