

# axi\_lite\_spi\_master.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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AXI Lite SPI Master is a core for interfacing with SPI Slave devices.

### License MIT

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## axi\_lite\_spi\_master

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```
module axi_lite_spi_master #(
  parameter
    ADDRESS_WIDTH
    =
    32,
  parameter
    BUS_WIDTH
    =
    4,
  parameter
    WORD_WIDTH
    =
    4,
  parameter
```

```

CLOCK_SPEED
=
100000000,
parameter
SELECT_WIDTH
=
16,
parameter
DEFAULT_RATE_DIV
=
0,
parameter
DEFAULT_CPOL
=
0,
parameter
DEFAULT_CPHA
=
0
) ( input aclk, input arstn, input s_axi_awvalid, input [ADDRESS_WIDTH-1:0]

```

AXI Lite based SPI Master device. BUS\_WIDTH is 4 bytes.

## Parameters

<b>ADDRESS_WIDTH</b> parameter	Width of the uP address port, max 32 bit.
<b>BUS_WIDTH</b> parameter	Width of the uP bus data port, only valid values are 2 or 4.
<b>WORD_WIDTH</b> parameter	Width of each SPI Master word. This will also set the bits used in the TX/RX data registers. Must be less than or equal to BUS_WIDTH. VALID: 1 to 4.
<b>CLOCK_SPEED</b> parameter	This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate.
<b>SELECT_WIDTH</b> parameter	Bit width of the slave select, defaults to 16 to match altera spi ip.
<b>DEFAULT_RATE_DIV</b> parameter	Default divider value of the main clock to use for the spi data output clock rate. 0 is 2 (2^(X+1) X is the DEFAULT_RATE_DIV)
<b>DEFAULT_CPOL</b> parameter	Default clock polarity for the core (0 or 1).
<b>DEFAULT_CPHA</b> parameter	Default clock phase for the core (0 or 1).

## Ports

<b>aclk</b>	Clock for all devices in the core
<b>arstn</b>	Negative reset
<b>s_axi_awvalid</b>	Axi Lite aw valid
<b>s_axi_awaddr</b>	Axi Lite aw addr
<b>s_axi_awprot</b>	Axi Lite aw prot
<b>s_axi_awready</b>	Axi Lite aw ready
<b>s_axi_wvalid</b>	Axi Lite w valid
<b>s_axi_wdata</b>	Axi Lite w data
<b>s_axi_wstrb</b>	Axi Lite w strb
<b>s_axi_wready</b>	Axi Lite w ready
<b>s_axi_bvalid</b>	Axi Lite b valid
<b>s_axi_bresp</b>	Axi Lite b resp

<b>s_axi_bready</b>	Axi Lite b ready
<b>s_axi_arvalid</b>	Axi Lite ar valid
<b>s_axi_araddr</b>	Axi Lite ar addr
<b>s_axi_arprot</b>	Axi Lite ar prot
<b>s_axi_arready</b>	Axi Lite ar ready
<b>s_axi_rvalid</b>	Axi Lite r valid
<b>s_axi_rdata</b>	Axi Lite r data
<b>s_axi_rresp</b>	Axi Lite r resp
<b>s_axi_rready</b>	Axi Lite r ready
<b>irq</b>	Interrupt when data is received
<b>sclk</b>	spi clock, should only drive output pins to devices.
<b>mosi</b>	transmit for master output
<b>miso</b>	receive for master input
<b>ss_n</b>	slave select output

## up\_rreq

```
wire up_rreq
```

uP read bus request

## up\_rack

```
wire up_rack
```

uP read bus acknowledge

## up\_raddr

```
wire [ADDRESS_WIDTH-(
BUS_WIDTH
2
)-1:0] up_raddr
```

uP read bus address

## up\_rdata

```
wire [31:0] up_rdata
```

uP read bus request

## up\_wreq

```
wire up_wreq
```

uP write bus request

## up\_wack

---

```
wire up_wack
```

uP write bus acknowledge

## up\_waddr

---

```
wire [ADDRESS_WIDTH-(  
BUS_WIDTH  
2  
)-1:0] up_waddr
```

uP write bus address

## up\_wdata

---

```
wire [31:0] up_wdata
```

uP write bus data

## INSTANTIATED MODULES

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### inst\_up\_axi

---

```
up_axi #(  
AXI_ADDRESS_WIDTH(ADDRESS_WIDTH)  
) inst_up_axi ( .up_rstn (arstn), .up_clk (acclk), .up_axi_awvalid(s_axi_awv
```

Module instance of up\_axi for the AXI Lite bus to the uP bus.

### inst\_up\_spi\_master

---

```
up_spi_master #(  
ADDRESS_WIDTH(ADDRESS_WIDTH),  
BUS_WIDTH(BUS_WIDTH),  
WORD_WIDTH(WORD_WIDTH),  
CLOCK_SPEED(CLOCK_SPEED),  
SELECT_WIDTH(SELECT_WIDTH),  
DEFAULT_RATE_DIV(DEFAULT_RATE_DIV),
```

```
    DEFAULT_CPOL(DEFAULT_CPOL),  
    DEFAULT_CPHA(DEFAULT_CPHA)  
) inst_up_spi_master ( .clk(aclk), .rstn(arstn), .up_rreq(up_rreq), .up_rack
```

Module instance of up\_spi\_master creating a Logic wrapper for spi master axis bus cores to interface with uP bus.