

tb_cocotb_wishbone_standard.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

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tb_cocotb

```
module tb_cocotb #(
  parameter
  ADDRESS_WIDTH
  =
  32,
  parameter
  BUS_WIDTH
  =
  4,
  parameter
  WORD_WIDTH
  =
  4,
  parameter
```

```

CLOCK_SPEED
=
100000000,
parameter
SELECT_WIDTH
=
16,
parameter
DEFAULT_RATE_DIV
=
0,
parameter
DEFAULT_CPOL
=
0,
parameter
DEFAULT_CPHA
=
0
) ( input clk, input rst, input s_wb_cyc, input s_wb_stb, input s_wb_we, input s_wb_data_i, input s_wb_sel, input s_wb_ack, input s_wb_data_o, input s_wb_err, input irq )

```

Wishbone Standard based SPI Master device.

Parameters

| | |
|--------------------------------------|--|
| ADDRESS_WIDTH parameter | Width of the uP address port, max 32 bit. |
| BUS_WIDTH parameter | Width of the uP bus data port(can not be less than 2 bytes, max tested is 4). |
| WORD_WIDTH parameter | Width of each SPI Master word. This will also set the bits used in the TX/RX data registers. Must be less than or equal to BUS_WIDTH 1 to 4. |
| CLOCK_SPEED parameter | This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate. |
| SELECT_WIDTH parameter | Bit width of the slave select, defaults to 16 to match altera spi ip. |
| DEFAULT_RATE_DIV parameter | Default divider value of the main clock to use for the spi data output clock rate. 0 is 2 (2^(X+1) X is the DEFAULT_RATE_DIV) |
| DEFAULT_CPOL parameter | Default clock polarity for the core (0 or 1). |
| DEFAULT_CPHA parameter | Default clock phase for the core (0 or 1). |

Ports

| | |
|--------------------|---|
| clk | Clock for all devices in the core |
| rst | Positive reset |
| s_wb_cyc | Bus Cycle in process |
| s_wb_stb | Valid data transfer cycle |
| s_wb_we | Active High write, low read |
| s_wb_addr | Bus address |
| s_wb_data_i | Input data |
| s_wb_sel | Device Select |
| s_wb_ack | Bus transaction terminated |
| s_wb_data_o | Output data |
| s_wb_err | Active high when a bus error is present |
| irq | Interrupt when data is received |

