wishbone_standard_spi_master.v

AUTHORS

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DATES

2025/04/30

INFORMATION

Brief

Wishbone Standard SPI Master core.

License MIT

wishbone_standard_spi_master

```
module wishbone_standard_spi_master #(
parameter
ADDRESS_WIDTH
 =
32,
parameter
BUS_WIDTH
 =
4,
parameter
WORD_WIDTH
 =
4,
parameter
```

```
 CLOCK_SPEED
  =
 100000000,
 parameter
 SELECT_WIDTH
  =
 16,
 parameter
 DEFAULT_RATE_DIV
  =
 0,
 parameter
 DEFAULT_CPOL
  =
 0,
 parameter
 DEFAULT_CPHA
  =
 0,
 parameter
 FIFO_ENABLE
  =
 0
)
                                                                    (
 input
 wire
 clk,
 input
 wire
 rst,
 input
 wire
 s_wb_cyc,
 input
 wire
 s_wb_stb,
 input
 wire
 s_wb_we,
 input
 wire
  [ADDRESS_WIDTH-1:0]
 s_wb_addr,
 input
 wire
  [BUS_WIDTH*8-1:0]
 s_wb_data_i,
 input
 wire
  [BUS_WIDTH-1:0]
 s_wb_sel,
 output
 wire
 s_wb_ack,
 output
 wire
  [BUS_WIDTH*8-1:0]
 s_wb_data_o,
 output
 wire
 s_wb_err,
 output
 wire
 irq,
 output
```

```
 wire
 sclk,
 output
 wire
 mosi,
 input
 wire
 miso,
 output
 wire
  [SELECT_WIDTH-1:0]
 ss_n
)
```

Wishbone Standard based SPI Master device.

Parameters

ADDRESS_WIDTH
parameter
Width of the uP address port, max 32 bit.

BUS_WIDTH
parameter
Width of the uP bus data port, only valid values are 2 or 4.

WORD_WIDTH
parameter
Width of each SPI Master word. This will also set the bits used in the TX/RX data registers. Must be less than or equal to BUS_WIDTH. VALID: 1 to 4.

CLOCK_SPEED
parameter
This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate.

SELECT_WIDTH
parameter
Bit width of the slave select, defaults to 16 to match altera spi ip.

DEFAULT_RATE_DIV
parameter
Default divider value of the main clock to use for the spi data output clock rate. 0 is 2 (2^(X+1) X is the DEFAULT_RATE_DIV)

DEFAULT_CPOL
parameter
Default clock polarity for the core (0 or 1).

DEFAULT_CPHA
parameter
Default clock phase for the core (0 or 1).

FIFO_ENABLE
parameter
Enable a 16 word fifo for rx and tx. All words put into the fifo together will keep chip select low.

Ports

clk
input wire
Clock for all devices in the core

rst
input wire
Positive reset

s_wb_cyc
input wire
Bus Cycle in process

s_wb_stb
input wire
Valid data transfer cycle

s_wb_we
input wire
Active High write, low read

s_wb_addr
input wire [ADDRESS_WIDTH- 1:0]
Bus address

s_wb_data_i
input wire [BUS_WIDTH* 8- 1:0]
Input data

s_wb_sel
input wire [BUS_WIDTH- 1:0]
Device Select

s_wb_ack
output wire
Bus transaction terminated

s_wb_data_o `output wire [BUS_WIDTH* 8- 1:0]`	Output data
s_wb_err `output wire`	Active high when a bus error is present
irq `output wire`	Interrupt when data is received
sclk `output wire`	spi clock, should only drive output pins to devices.
mosi `output wire`	transmit for master output
miso `input wire`	receive for master input
ss_n `output wire [SELECT_WIDTH- 1:0]`	slave select output

up_rreq

```
wire up_rreq
```

uP read bus request

up_rack

```
wire up_rack
```

uP read bus acknowledge

up_raddr

```
wire [ADDRESS_WIDTH-(
BUS_WIDTH
                                                                    /
2
)-1:0] up_raddr
```

uP read bus address

up_rdata

```
wire [31:0] up_rdata
```

uP read bus request

up_wreq

```
wire up_wreq
```

uP write bus request

up_wack

```
wire up_wack
```

uP write bus acknowledge

up_waddr

```
wire [ADDRESS_WIDTH-(
BUS_WIDTH
                                                                    /
2
)-1:0] up_waddr
```

uP write bus address

up_wdata

```
wire [31:0] up_wdata
```

uP write bus data

INSTANTIANTED MODULES

inst_up_wishbone_standard

Module instance of up_wishbone_standard for the Wishbone Classic Standard bus to the uP bus.

inst_up_spi_master

Module instance of up_spi_master creating a Logic wrapper for spi master axis bus cores to interface with uP bus.