# tb_cocotb_axi_lite.v

## AUTHORS

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## DATES

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## INFORMATION

### Brief

Test bench wrapper for cocotb

### License MIT



### tb_cocotb

```
module tb_cocotb #(
parameter
ADDRESS_WIDTH
 =
32,
parameter
BUS_WIDTH
 =
4,
parameter
WORD_WIDTH
 =
4,
parameter
```

```
 CLOCK_SPEED
  =
 100000000,
 parameter
 SELECT_WIDTH
  =
 16,
 parameter
 DEFAULT_RATE_DIV
  =
 0,
 parameter
 DEFAULT_CPOL
  =
 0,
 parameter
 DEFAULT_CPHA
  =
 0
)
                                                                    (
 input
 aclk,
 input
 arstn,
 input
 s_axi_awvalid,
 input
  [ADDRESS_WIDTH-1:0]
 s_axi_awaddr,
 input
  [ 2:0]
 s_axi_awprot,
 output
 s_axi_awready,
 input
 s_axi_wvalid,
 input
  [(BUS_WIDTH*8)-1:0]
 s_axi_wdata,
 input
  [ 3:0]
 s_axi_wstrb,
 output
 s_axi_wready,
 output
 s_axi_bvalid,
 output
  [ 1:0]
 s_axi_bresp,
 input
 s_axi_bready,
 input
 s_axi_arvalid,
 input
  [ADDRESS_WIDTH-1:0]
 s_axi_araddr,
 input
  [ 2:0]
 s_axi_arprot,
 output
 s_axi_arready,
 output
 s_axi_rvalid,
 output
  [(BUS_WIDTH*8)-1:0]
```

```
 s_axi_rdata,
 output
  [ 1:0]
 s_axi_rresp,
 input
 s_axi_rready,
 output
 irq,
 output
 sclk,
 output
 mosi,
 input
 miso,
 output
  [SELECT_WIDTH-1:0]
 ss_n
)
```

AXI Lite based SPI Master device.

## Parameters

| | |
|---|---|
| **ADDRESS_WIDTH**<br>parameter | Width of the uP address port, max 32 bit. |
| **BUS_WIDTH**<br>parameter | Width of the uP bus data port, only valid values are 2 or 4. |
| **WORD_WIDTH**<br>parameter | Width of each SPI Master word. This will also set the bits used in the TX/RX data registers. Must be less than or equal to BUS_WIDTH 1 to 4. |
| **CLOCK_SPEED**<br>parameter | This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate. |
| **SELECT_WIDTH**<br>parameter | Bit width of the slave select, defaults to 16 to match altera spi ip. |
| **DEFAULT_RATE_DIV**<br>parameter | Default divider value of the main clock to use for the spi data output clock rate. 0 is 2 (2^(X+1) X is the DEFAULT_RATE_DIV) |
| **DEFAULT_CPOL**<br>parameter | Default clock polarity for the core (0 or 1). |
| **DEFAULT_CPHA**<br>parameter | Default clock phase for the core (0 or 1). |

## Ports

| | |
|---|---|
| **aclk**<br>input | Clock for all devices in the core |
| **arstn**<br>input | Negative reset |
| **s_axi_awvalid**<br>input | Axi Lite aw valid |
| **s_axi_awaddr**<br>input [ADDRESS_WIDTH- 1:0] | Axi Lite aw addr |
| **s_axi_awprot**<br>input [2:0] | Axi Lite aw prot |
| **s_axi_awready**<br>output [2:0] | Axi Lite aw ready |
| **s_axi_wvalid**<br>input [2:0] | Axi Lite w valid |
| **s_axi_wdata**<br>input [(BUS_WIDTH* 8)- 1:0] | Axi Lite w data |

| | |
|---|---|
| **s_axi_wstrb**<br>input [3:0] | Axi Lite w strb |
| **s_axi_wready**<br>output [3:0] | Axi Lite w ready |
| **s_axi_bvalid**<br>output [3:0] | Axi Lite b valid |
| **s_axi_bresp**<br>output [1:0] | Axi Lite b resp |
| **s_axi_bready**<br>input [1:0] | Axi Lite b ready |
| **s_axi_arvalid**<br>input [1:0] | Axi Lite ar valid |
| **s_axi_araddr**<br>input [ADDRESS_WIDTH- 1:0] | Axi Lite ar addr |
| **s_axi_arprot**<br>input [2:0] | Axi Lite ar prot |
| **s_axi_arready**<br>output [2:0] | Axi Lite ar ready |
| **s_axi_rvalid**<br>output [2:0] | Axi Lite r valid |
| **s_axi_rdata**<br>output [(BUS_WIDTH* 8)- 1:0] | Axi Lite r data |
| **s_axi_rresp**<br>output [1:0] | Axi Lite r resp |
| **s_axi_rready**<br>input [1:0] | Axi Lite r ready |
| **irq**<br>output [1:0] | Interrupt when data is received |
| **sclk**<br>output [1:0] | spi clock, should only drive output pins to devices. |
| **mosi**<br>output [1:0] | transmit for master output |
| **miso**<br>input [1:0] | receive for master input |
| **ss_n**<br>output [SELECT_WIDTH- 1:0] | slave select output |

# INSTANTIATED MODULES

## dut

Device under test, axi_lite_spi_master