

tb_cocotb_wishbone_standard.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

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tb_cocotb

```
module tb_cocotb #(
  parameter
    ADDRESS_WIDTH
    =
    32,
  parameter
    BUS_WIDTH
    =
    4,
  parameter
    WORD_WIDTH
    =
    4,
  parameter
```

```

CLOCK_SPEED
=
100000000,
parameter
SELECT_WIDTH
=
16,
parameter
DEFAULT_RATE_DIV
=
0,
parameter
DEFAULT_CPOL
=
0,
parameter
DEFAULT_CPHA
=
0
)

input
clk,
input
rst,
input
s_wb_cyc,
input
s_wb_stb,
input
s_wb_we,
input
[ADDRESS_WIDTH-1:0]
s_wb_addr,
input
[BUS_WIDTH*8-1:0]
s_wb_data_i,
input
[BUS_WIDTH-1:0]
s_wb_sel,
output
s_wb_ack,
output
[BUS_WIDTH*8-1:0]
s_wb_data_o,
output
s_wb_err,
output
irq,
output
sclk,
output
mosi,
input
miso,
output
[SELECT_WIDTH-1:0]
ss_n
)

```

(

Wishbone Standard based SPI Master device.

Parameters

ADDRESS_WIDTH Width of the uP address port, max 32 bit.
parameter

BUS_WIDTH parameter	Width of the uP bus data port(can not be less than 2 bytes, max tested is 4).
WORD_WIDTH parameter	Width of each SPI Master word. This will also set the bits used in the TX/RX data registers. Must be less than or equal to BUS_WIDTH 1 to 4.
CLOCK_SPEED parameter	This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate.
SELECT_WIDTH parameter	Bit width of the slave select, defaults to 16 to match altera spi ip.
DEFAULT_RATE_DIV parameter	Default divider value of the main clock to use for the spi data output clock rate. 0 is 2 ($2^{(X+1)}$ X is the DEFAULT_RATE_DIV)
DEFAULT_CPOL parameter	Default clock polarity for the core (0 or 1).
DEFAULT_CPHA parameter	Default clock phase for the core (0 or 1).

Ports

clk input	Clock for all devices in the core
rst input	Positive reset
s_wb_cyc input	Bus Cycle in process
s_wb_stb input	Valid data transfer cycle
s_wb_we input	Active High write, low read
s_wb_addr input [ADDRESS_WIDTH- 1:0]	Bus address
s_wb_data_i input [BUS_WIDTH* 8- 1:0]	Input data
s_wb_sel input [BUS_WIDTH- 1:0]	Device Select
s_wb_ack output [BUS_WIDTH- 1:0]	Bus transaction terminated
s_wb_data_o output [BUS_WIDTH* 8- 1:0]	Output data
s_wb_err output [BUS_WIDTH* 8- 1:0]	Active high when a bus error is present
irq output [BUS_WIDTH* 8- 1:0]	Interrupt when data is received
sclk output [BUS_WIDTH* 8- 1:0]	spi clock, should only drive output pins to devices.
mosi output [BUS_WIDTH* 8- 1:0]	transmit for master output
miso input [BUS_WIDTH* 8- 1:0]	receive for master input
ss_n output [SELECT_WIDTH- 1:0]	slave select output

INSTANTIATED MODULES

dut

Device under test, wishbone_standard_spi_master