

# up\_spi\_master.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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uP Core for interfacing with axis spi that emulates the ALTERA SPI IP in MASTER mode.

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## up\_spi\_master

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```
module up_spi_master #(
  parameter
  ADDRESS_WIDTH
  =
  32,
  parameter
  BUS_WIDTH
  =
  4,
  parameter
  WORD_WIDTH
  =
  4,
  parameter
```

```

CLOCK_SPEED
=
100000000,
parameter
SELECT_WIDTH
=
16,
parameter
DEFAULT_RATE_DIV
=
0,
parameter
DEFAULT_CPOL
=
0,
parameter
DEFAULT_CPHA
=
0,
parameter
FIFO_ENABLE
=
0
)

input
wire
clk,
input
wire
rstn,
input
wire
up_rreq,
output
wire
up_rack,
input
wire
[ADDRESS_WIDTH-(BUS_WIDTH/2)-1:0]
up_raddr,
output
wire
[(BUS_WIDTH*8)-1:0]
up_rdata,
input
wire
up_wreq,
output
wire
up_wack,
input
wire
[ADDRESS_WIDTH-(BUS_WIDTH/2)-1:0]
up_waddr,
input
wire
[(BUS_WIDTH*8)-1:0]
up_wdata,
output
wire
irq,
output
wire
sclk,
output

```

(

```

wire
mosi,
input
wire
miso,
output
wire
[SELECT_WIDTH-1:0]
ss_n
)

```

SPI Master core with axis input/output data. Read/Write is size of BUS\_WIDTH bytes. Write activates core for read.

## Parameters

<b>ADDRESS_WIDTH</b> parameter	Width of the uP address port, max 32 bit.
<b>BUS_WIDTH</b> parameter	Width of the uP bus data port, only valid values are 2 or 4.
<b>WORD_WIDTH</b> parameter	Width of each SPI Master word. This will also set the bits used in the TX/RX data registers. Must be less than or equal to BUS_WIDTH, VALID: 1 to 4.
<b>CLOCK_SPEED</b> parameter	This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate.
<b>SELECT_WIDTH</b> parameter	Bit width of the slave select, defaults to 16 to match altera spi ip.
<b>DEFAULT_RATE_DIV</b> parameter	Default divider value of the main clock to use for the spi data output clock rate. 0 is 2 ( $2^{(X+1)}$ X is the DEFAULT_RATE_DIV)
<b>DEFAULT_CPOL</b> parameter	Default clock polarity for the core (0 or 1).
<b>DEFAULT_CPHA</b> parameter	Default clock phase for the core (0 or 1).
<b>FIFO_ENABLE</b> parameter	Enable a 16 word (byte) fifo for RX/TX. Not a standard part of the Altera IP core.

## Ports

<b>clk</b> input wire	Clock for all devices in the core
<b>rstn</b> input wire	Negative reset
<b>up_rreq</b> input wire	uP bus read request
<b>up_rack</b> output wire	uP bus read ack
<b>up_raddr</b> input wire [ADDRESS_WIDTH-(BUS_WIDTH/ 2)- 1:0]	uP bus read address
<b>up_rdata</b> output wire [(BUS_WIDTH* 8)- 1:0]	uP bus read data
<b>up_wreq</b> input wire	uP bus write request
<b>up_wack</b> output wire	uP bus write ack
<b>up_waddr</b> input wire [ADDRESS_WIDTH-(BUS_WIDTH/ 2)- 1:0]	uP bus write address
<b>up_wdata</b> input wire [(BUS_WIDTH* 8)- 1:0]	uP bus write data

<b>irq</b> output wire	Interrupt when data is received
<b>sclk</b> output wire	spi clock, should only drive output pins to devices.
<b>mosi</b> output wire	transmit for master output
<b>miso</b> input wire	receive for master input
<b>ss_n</b> output wire [SELECT_WIDTH- 1:0]	slave select output

## DIVISOR

---

```
localparam DIVISOR = BUS_WIDTH/2
```

Divide the address register default location for 1 byte access to multi byte access. (register offsets are byte offsets).

## REG\_SIZE

---

```
localparam REG_SIZE = 8
```

Number of bits for the register address

## FIFO\_DEPTH

---

```
localparam FIFO_DEPTH = 16
```

Depth of the fifo, matches UART LITE (xilinx), so I kept this just cause

## REGISTER INFORMATION

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Core has 7 registers at the offsets that follow when at a full 32 bit bus width, Internal address is OFFSET >> BUS\_WIDTH/2 (32bit would be h4 >> 2 = 1 for internal address).

<b>RX_DATA_REG</b>	h00
<b>TX_DATA_REG</b>	h04
<b>STATUS_REG</b>	h08
<b>CONTROL_REG</b>	h0C
<b>RESERVED</b>	h10
<b>SLAVE_SELECT_REG</b>	h14
<b>EOP_VALUE_REG</b>	h18
<b>CONTROL_EXT_REG</b>	h1C
<b>SPEED_EXT_REG</b>	h20

## RX\_DATA\_REG

---

```
localparam RX_DATA_REG = 8'h0 >> DIVISOR
```

Defines the address offset for RX DATA OUTPUT

RX DATA REGISTER	
31:N	N:0
UNUSED	RECEIVED DATA

Valid bits are from WORD\_WIDTH\*8-1:0, which are data.

## TX\_DATA\_REG

```
localparam TX_DATA_REG = 8'h4 >> DIVISOR
```

Defines the address offset to write the TX DATA INPUT.

TX DATA REGISTER	
31:N	N:0
UNUSED	TRANSMIT DATA

Valid bits are from WORD\_WIDTH\*8-1:0, which are data.

## STATUS\_REG

```
localparam STATUS_REG = 8'h8 >> DIVISOR
```

Defines the address offset to read the status bits.

STATUS REGISTER								
31:10	9	8	7	6	5	4	3	2:0
UNUSED	EOP	E	RRDY	TRDY	TMT	TOE	ROE	UNUSED

## Status Register, 1 is considered active.

<b>EOP</b>	9, This bit is active(1) when the EOP_VALUE_REG is equal to RX_DATA_REG or TX_DATA_REG.
<b>E</b>	8, Logical or of TOE and ROE (Clear by writing status).
<b>RRDY</b>	7, Receive is ready (full) when the bit is 1, empty when the bit is 0.
<b>TRDY</b>	6, Transmit is ready (empty) when the bit is 1, full when the bit is 0.
<b>TMT</b>	5, Transmit shift register empty is set to 1 when all bits have been output.
<b>TOE</b>	4, Transmit overrun is set to 1 when a TX_DATA_REG write happens whne TRDY is 1 (Clear by writing status reg).

**ROE**      3, Receive overrun is set to 1 when RRDY is 1 and a new received word is going to be written to RX\_DATA\_REG (Clear by writing status reg)

## CONTROL\_REG

```
localparam CONTROL_REG = 8'hC >> DIVISOR
```

Defines the address offset to set the control bits.

CONTROL REGISTER									
31:11	10	9	8	7	6	5	4	3	2:0
UNUSED	SSO	IEOP	IE	IRRDY	ITRDY	UNUSED	ITOE	IROE	UNUSED

Control Register, 1 is considered active. **All zeros on reset.**

**SSO**      10, Setting this to 1 will force all ss\_n lines to 0 (selected).  
**IEOP**     9, Generate a interrupt on EOP status bit going active if set to 1.  
**IE**        8, Generate a interrupt on ANY error, active if set to 1.  
**IRRDY**    7, Generate a interrupt on RRDY status bit going active if set to 1.  
**ITRDY**    6, Generate a interrupt on TRDY status bit going active if set to 1.  
**ITOE**     4, Generate a interrupt on TOE status bit going active if set to 1.  
**IROE**     3, Generate a interrupt on ROE status bit going active if set to 1.

## RESERVED

```
localparam RESERVED = 8'h10 >> DIVISOR
```

Defines the address offset that is not used.

## SLAVE\_SELECT\_REG

```
localparam SLAVE_SELECT_REG = 8'h14 >> DIVISOR
```

Defines the address offset to set the slave select value

SLAVE SELECT REGISTER	
31:N	N:0
UNUSED	SLAVE SELECT

Valid bits are from SELECT\_WIDTH-1:0, which are the slave select output lines to drive low during data transmission.

## EOP\_VALUE\_REG

---

```
localparam EOP_VALUE_REG = 8'h18 >> DIVISOR
```

Defines the address offset to set the end of packet match value

EOP REGISTER	
31:N	N:0
UNUSED	EOP

Valid bits are from BUS\_WIDTH\*8:0, which are used to check for a word match between rx and/or tx and update status.

## CONTROL\_EXT\_REG

---

```
localparam CONTROL_EXT_REG = 8'h1c >> DIVISOR
```

Defines the address offset for control register extensions

CONTROL REGISTER EXTENDED		
31:2	1	0
UNUSED	CPHA	CPOL

## Control Extension to add capabilities to Altera IP core.

**CPHA** 1, Clock Phase Bit, 0 or 1 per SPI specs (default value set by IP parameter).  
**CPOL** 0, Clock Polarity bit, 0 or 1 per SPI specs (default value set by IP parameter).

## SPEED\_EXT\_REG

---

```
localparam SPEED_EXT_REG = 8'h20 >> DIVISOR
```

Defines the address offset for speed control reg extension

SPEED CONTROL REGISTER
31:0
SPI OUTPUT CLOCK IN HZ

Valid bits are from BUS\_WIDTH\*8-1:0, which is the speed of the spi core in HZ.

## INSTANTIATED MODULES

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### **inst\_axis\_spi**

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SPI Master instance with AXIS interface

### **inst\_axis\_tx\_fifo**

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SPI trasnmit data fifo.

### **inst\_axis\_rx\_fifo**

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SPI received data fifo.