

axi_lite_spi_master.v

AUTHORS

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DATES

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INFORMATION

Brief

AXI Lite SPI Master is a core for interfacing with SPI Slave devices.

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axi_lite_spi_master

```
module axi_lite_spi_master #(
  parameter
  ADDRESS_WIDTH
  =
  32,
  parameter
  BUS_WIDTH
  =
  4,
  parameter
  WORD_WIDTH
  =
  4,
  parameter
```

```

CLOCK_SPEED
=
100000000,
parameter
SELECT_WIDTH
=
16,
parameter
DEFAULT_RATE_DIV
=
0,
parameter
DEFAULT_CPOL
=
0,
parameter
DEFAULT_CPHA
=
0,
parameter
FIFO_ENABLE
=
0
)

input
wire
aclk,
input
wire
arstn,
input
wire
s_axi_awvalid,
input
wire
[ADDRESS_WIDTH-1:0]
s_axi_awaddr,
input
wire
[ 2:0]
s_axi_awprot,
output
wire
s_axi_awready,
input
wire
s_axi_wvalid,
input
wire
[(BUS_WIDTH*8)-1:0]
s_axi_wdata,
input
wire
[ 3:0]
s_axi_wstrb,
output
wire
s_axi_wready,
output
wire
s_axi_bvalid,
output
wire
[ 1:0]
s_axi_bresp,

```

(

```

input
wire
s_axi_bready,
input
wire
s_axi_arvalid,
input
wire
[ADDRESS_WIDTH-1:0]
s_axi_araddr,
input
wire
[ 2:0]
s_axi_arprot,
output
wire
s_axi_arready,
output
wire
s_axi_rvalid,
output
wire
[(BUS_WIDTH*8)-1:0]
s_axi_rdata,
output
wire
[ 1:0]
s_axi_rresp,
input
wire
s_axi_rready,
output
wire
irq,
output
wire
sclk,
output
wire
mosi,
input
wire
miso,
output
wire
[SELECT_WIDTH-1:0]
ss_n
)

```

AXI Lite based SPI Master device. BUS_WIDTH is 4 bytes.

Parameters

ADDRESS_WIDTH parameter	Width of the uP address port, max 32 bit.
BUS_WIDTH parameter	Width of the uP bus data port, only valid values are 2 or 4.
WORD_WIDTH parameter	Width of each SPI Master word. This will also set the bits used in the TX/RX data registers. Must be less than or equal to BUS_WIDTH. VALID: 1 to 4.
CLOCK_SPEED parameter	This is the aclk frequency in Hz, this is the the frequency used for the bus and is divided by the rate.
SELECT_WIDTH parameter	Bit width of the slave select, defaults to 16 to match altera spi ip.

DEFAULT_RATE_DIV parameter	Default divider value of the main clock to use for the spi data output clock rate. 0 is 2 (2^(X+1) X is the DEFAULT_RATE_DIV)
DEFAULT_CPOL parameter	Default clock polarity for the core (0 or 1).
DEFAULT_CPHA parameter	Default clock phase for the core (0 or 1).
FIFO_ENABLE parameter	Enable a 16 word fifo for RX and TX. The chip select will stay asserted between words.

Ports

aclk input wire	Clock for all devices in the core
arstn input wire	Negative reset
s_axi_awvalid input wire	Axi Lite aw valid
s_axi_awaddr input wire [ADDRESS_WIDTH- 1:0]	Axi Lite aw addr
s_axi_awprot input wire [2:0]	Axi Lite aw prot
s_axi_awready output wire	Axi Lite aw ready
s_axi_wvalid input wire	Axi Lite w valid
s_axi_wdata input wire [(BUS_WIDTH* 8)- 1:0]	Axi Lite w data
s_axi_wstrb input wire [3:0]	Axi Lite w strb
s_axi_wready output wire	Axi Lite w ready
s_axi_bvalid output wire	Axi Lite b valid
s_axi_bresp output wire [1:0]	Axi Lite b resp
s_axi_bready input wire	Axi Lite b ready
s_axi_arvalid input wire	Axi Lite ar valid
s_axi_araddr input wire [ADDRESS_WIDTH- 1:0]	Axi Lite ar addr
s_axi_arprot input wire [2:0]	Axi Lite ar prot
s_axi_arready output wire	Axi Lite ar ready
s_axi_rvalid output wire	Axi Lite r valid
s_axi_rdata output wire [(BUS_WIDTH* 8)- 1:0]	Axi Lite r data
s_axi_rresp output wire [1:0]	Axi Lite r resp
s_axi_rready input wire	Axi Lite r ready
irq	Interrupt when data is received

```

output wire
sclk                                spi clock, should only drive output pins to devices.
output wire
mosi                                transmit for master output
output wire
miso                                receive for master input
input wire
ss_n                                slave select output
output wire [SELECT_WIDTH- 1:0]

```

up_rreq

```
wire up_rreq
```

uP read bus request

up_rack

```
wire up_rack
```

uP read bus acknowledge

up_raddr

```

wire [ADDRESS_WIDTH-(
BUS_WIDTH
2
)-1:0] up_raddr
/

```

uP read bus address

up_rdata

```
wire [31:0] up_rdata
```

uP read bus request

up_wreq

```
wire up_wreq
```

uP write bus request

up_wack

```
wire up_wack
```

uP write bus acknowledge

up_waddr

```
wire [ADDRESS_WIDTH-(  
BUS_WIDTH  
2  
)-1:0] up_waddr
```

/

uP write bus address

up_wdata

```
wire [31:0] up_wdata
```

uP write bus data

INSTANTIATED MODULES

inst_up_axi

Module instance of up_axi for the AXI Lite bus to the uP bus.

inst_up_spi_master

Module instance of up_spi_master creating a Logic wrapper for spi master axis bus cores to interface with uP bus.