tm_stim_clk.v

AUTHORS

JAY CONVERTINO

DATES

2022/10/24

INFORMATION

Brief

clock simulator creates multiple clocks and resets for testing.

License MIT

clk_stimulus

```
module clk_stimulus #(
parameter
CLOCKS
 =
2,
parameter
CLOCK_BASE
 =
1000000,
parameter
CLOCK_INC
```

```
  =
 100,
 parameter
 CLOCK_ASYNC
  =
 0,
 parameter
 RESETS
  =
 2,
 parameter
 RESET_BASE
  =
 200,
 parameter
 RESET_INC
  =
 100
) ( output reg [CLOCKS-1:0] clkv, output reg [RESETS-1:0] rstnv, output reg
```

clock simulator creates multiple clocks and resets for testing.

Parameters

CLOCKS Number of clocks
parameter

CLOCK_BASE Clock time base mhz
parameter

CLOCK_INC Time diff for other clocks, only used for async mode
parameter

CLOCK_ASYNC Used time diff to generate async clocks (1), 0 is sync clock
parameter

RESETS Number of resets
parameter

RESET_BASE Time to stay in reset
parameter

RESET_INC Time diff for other resets
parameter

Ports

clkv clock output vector

rstnv negative reset output vector

rstv positive reset output vector