

tm_stim_clk.v

AUTHORS

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DATES

2022/10/24

INFORMATION

Brief

clock simulator creates multiple clocks and resets for testing.

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clk_stimulus

```
module clk_stimulus #(
  parameter
    CLOCKS
    =
    2,
  parameter
    CLOCK_BASE
    =
    1000000,
  parameter
    CLOCK_INC
```

```

    =
    100,
    parameter
    CLOCK_ASYNC
    =
    0,
    parameter
    RESETS
    =
    2,
    parameter
    RESET_BASE
    =
    200,
    parameter
    RESET_INC
    =
    100
) ( output reg [CLOCKS-1:0] clkv, output reg [RESETS-1:0] rstnv, output reg

```

clock simulator creates multiple clocks and resets for testing.

Parameters

CLOCKS parameter	Number of clocks
CLOCK_BASE parameter	Clock time base mhz
CLOCK_INC parameter	Time diff for other clocks, only used for async mode
CLOCK_ASYNC parameter	Used time diff to generate async clocks (1), 0 is sync clock
RESETS parameter	Number of resets
RESET_BASE parameter	Time to stay in reset
RESET_INC parameter	Time diff for other resets

Ports

clkv	clock output vector
rstnv	negative reset output vector
rstv	positive reset output vector