test.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench for busbase

License MIT

test

```
module test #(
parameter
ADDRESS_WIDTH
  =
32,
parameter
BUS_WIDTH
  =
4
) ( input clk, input rst, inout [ADDRESS_WIDTH-1:0] b_addr, inout b_we, inou
```

Test bench loop busbase example

Parameters

ADDRESS_WIDTH parameter	Width of the address in bits.
BUS_WIDTH parameter	Width of the data in bytes.

Ports

clk	Clock for all devices in the core
rst	Negative reset
b_addr	address to read write from
b_we	write enable 1, read 0
b_cs	chip select, 1 selected
b_data	data input/output