

# test.v

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## AUTHORS

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JAY CONVERTINO

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## DATES

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## INFORMATION

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### Brief

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Test bench for busbase

### License MIT

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### test

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```
module test #(
  parameter
  ADDRESS_WIDTH
  =
  32,
  parameter
  BUS_WIDTH
  =
  4
) ( input clk, input rst, inout [ADDRESS_WIDTH-1:0] b_addr, inout b_we, inout b_data )
```

Test bench loop busbase example

## Parameters

<b>ADDRESS_WIDTH</b> <small>parameter</small>	Width of the address in bits.
<b>BUS_WIDTH</b> <small>parameter</small>	Width of the data in bytes.

## Ports

<b>clk</b>	Clock for all devices in the core
<b>rst</b>	Negative reset
<b>b_addr</b>	address to read write from
<b>b_we</b>	write enable 1, read 0
<b>b_cs</b>	chip select, 1 selected
<b>b_data</b>	data input/output