

# test.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Test bench for xilinx fifo using cocotb

### License MIT

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### test

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```
module test #(
  parameter
    FIFO_DEPTH
    =
    8,
  parameter
    BYTE_WIDTH
    =
    4,
  parameter
    FWFT
    =
    1
) ( input rd_clk, input rd_rstn, inout rd_en, inout rd_valid, inout [(BYTE_V
```

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Test bench loop for xilinx fifo

## Parameters

<b>FIFO_DEPTH</b> parameter	Depth of the fifo, must be a power of two number(divisable aka $256 = 2^8$ ). Any non-power of two will be rounded up to the next closest.
<b>BYTE_WIDTH</b> parameter	How many bytes wide the data in/out will be.
<b>FWFT</b> parameter	1 for first word fall through mode. 0 for normal.

## Ports

<b>rd_clk</b>	Clock for read data
<b>rd_rstn</b>	Negative edge reset for read.
<b>rd_en</b>	Active high enable of read interface.
<b>rd_valid</b>	Active high output that the data is valid.
<b>rd_data</b>	Output data
<b>rd_empty</b>	Active high output when read is empty.
<b>wr_clk</b>	Clock for write data
<b>wr_rstn</b>	Negative edge reset for write
<b>wr_en</b>	Active high enable of write interface.
<b>wr_ack</b>	Active high when enabled, that data write has been done.
<b>wr_data</b>	Input data
<b>wr_full</b>	Active high output that the FIFO is full.