

# test.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Test bench for apb using cocotb

### License MIT

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### test

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```
module test #(
  parameter
  ADDRESS_WIDTH
  =
  16,
  parameter
  BUS_WIDTH
  =
  4
) ( input clk, input rst, inout s_wb_cyc, inout s_wb_stb, inout s_wb_we, inc
```

Test of Wishbone Classic

## Parameters

<b>ADDRESS_WIDTH</b> parameter	Width of the Wishbone address port in bits.
<b>BUS_WIDTH</b> parameter	Width of the Wishbone bus data port in bytes.

## Ports

<b>clk</b>	Clock
<b>rst</b>	Positive reset
<b>s_wb_cyc</b>	Bus Cycle in process
<b>s_wb_stb</b>	Valid data transfer cycle
<b>s_wb_we</b>	Active High write, low read
<b>s_wb_addr</b>	Bus address
<b>s_wb_data_i</b>	Input data
<b>s_wb_sel</b>	Device Select
<b>s_wb_ack</b>	Bus transaction terminated
<b>s_wb_data_o</b>	Output data
<b>s_wb_err</b>	Active high when a bus error is present