test.v

AUTHORS

JAY CONVERTINO

DATES

2025/03/17

INFORMATION

Brief

Test bench for apb using cocotb

License MIT

test

```
module test #(
parameter
ADDRESS_WIDTH
  =
16,
parameter
BUS_WIDTH
  =
4
) ( input clk, input rst, inout s_wb_cyc, inout s_wb_stb, inout s_wb_we, inc
```

Test of Wishbone Classic

Parameters

ADDRESS_WIDTH parameter	Width of the Wishbone address port in bits.
BUS_WIDTH parameter	Width of the Wishbone bus data port in bytes.

Ports

clk	Clock
rst	Positive reset
s_wb_cyc	Bus Cycle in process
s_wb_stb	Valid data transfer cycle
s_wb_we	Active High write, low read
s_wb_addr	Bus address
s_wb_data_i	Input data
s_wb_sel	Device Select
s_wb_ack	Bus transaction terminated
s_wb_data_o	Output data
s_wb_err	Active high when a bus error is present