

# tb\_cocotb.v

---

## AUTHORS

---

JAY CONVERTINO

---

## DATES

---

2025/05/21

---

## INFORMATION

---

### Brief

---

Test bench wrapper for cocotb

### License MIT

---

Copyright 2025 Jay Convertino

Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions:

The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software.

THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE. BUS\_WIDTH

## tb\_cocotb

---

```
module tb_cocotb #(
  parameter
  RAM_DEPTH
  =
  1,
  parameter
  BYTE_WIDTH
  =
  1,
  parameter
  ADDR_WIDTH
  =
  1,
  parameter
```

```

    HEX_FILE
    =
    "",
    parameter
    RAM_TYPE
    =
    "block",
    parameter
    RD_CLOCK_SPEED
    =
    10000000,
    parameter
    WR_CLOCK_SPEED
    =
    10000000
) ( input rd_clk, input rd_rstn, input rd_en, output [(BYTE_WIDTH*8)-1:0] rd_data,
    input wr_clk, input wr_rstn, input wr_en, input wr_ben, input wr_data, input wr_addr

```

Generic Dual Port RAM wrapper

Parameters

<b>RAM_DEPTH</b> <i>parameter</i>	Number of words using the size of BYTE_WIDTH.
<b>BYTE_WIDTH</b> <i>parameter</i>	Width of the data bus in bytes.
<b>ADDR_WIDTH</b> <i>parameter</i>	Width of the address bus in bits.
<b>HEX_FILE</b> <i>parameter</i>	Read a hex value text file as the initial state of the RAM.
<b>RAM_TYPE</b> <i>parameter</i>	Used to set the ram_style attribute.
<b>RD_CLOCK_SPEED</b> <i>parameter</i>	COCOTB CLOCK SPEED FOR READ IN HZ.
<b>WR_CLOCK_SPEED</b> <i>parameter</i>	COCOTB CLOCK SPEED FOR WRITE IN HZ.

Ports

<b>rd_clk</b>	Read clock positive edge
<b>rd_rstn</b>	Read reset active low
<b>rd_en</b>	Read enable active high
<b>rd_data</b>	Read data output
<b>rd_addr</b>	Read data address select
<b>wr_clk</b>	Write clock positive edge
<b>wr_rstn</b>	Write reset active low
<b>wr_en</b>	Write enable active high
<b>wr_ben</b>	Write byte enable, each bit represents one byte of write data.
<b>wr_data</b>	Write data input
<b>wr_addr</b>	Write data address select

INSTANTIATED MODULES

dut

```

dc_block_ram #(
    RAM_DEPTH(RAM_DEPTH),
    BYTE_WIDTH(BYTE_WIDTH),
    ADDR_WIDTH(ADDR_WIDTH),
    HEX_FILE(HEX_FILE),
    RAM_TYPE(RAM_TYPE)
) dut ( .rd_clk(rd_clk), .rd_rstn(rd_rstn), .rd_en(rd_en), .rd_data(rd_data)

```

Device under test, dc\_block\_ram