DC_BLOCK_RAM

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Contents

1 Usage

1.1 Introduction

Dual clock block RAM for any FPGA target. Includes a byte enable for selecting bytes to write from the bus.

1.2 Dependencies

The following are the dependencies of the cores.

- fusesoc 2.X
- iverilog (simulation)
- cocotb (simulation)

1.2.1 fusesoc_info Depenecies

- dep
  - AFRL:utility:helper:1.0.0
- dep_tb
  - AFRL:simulation:clock_stimulator
  - AFRL:utility:sim_helper

1.3 In a Project

Connect the device using the read write signals see 5 for details

2 Architecture

This core is made up of a single module.

- **ft245_sync_to_axis** Interface AXIS to F245 device (see core for documentation).

This core has 2 always blocks that are sensitive to the positive clock edge.

- **Produce Data** Takes write input data and stores it in RAM at a specified address. BE will filter out bytes if the corresponding bits not set to active high.
- **Consume Data** Read data from RAM at a specified address and output over read interface.

Please see 5 for information on read/write interface ports.

3 Building

The DC block RAM is written in Verilog 2001. It should synthesize in any modern FPGA software. The core comes as a fusesoc packaged core and can be included in any other core. Be sure to make sure you have meet the dependencies listed in the previous section.

3.1 fusesoc

Fusesoc is a system for building FPGA software without relying on the internal project management of the tool. Avoiding vendor lock in to Vivado or Quartus. These cores, when included in a project, can be easily integrated and targets created based upon the end developer needs. The core by itself is not a part of a system and should be integrated into a fusesoc based system. Simulations are setup to use fusesoc and are a part of its targets.

3.2 Source Files

3.2.1 fusesoc_info File List

- src

  Type: verilogSource
  - src/dc_block_ram.v
- tb
  - 'tb/tb_fifo.v': 'file_type': 'verilogSource'

3.3 Targets

3.3.1 fusesoc_info Targets

- default

  Info: Default for IP intergration.
  - src
  - dep
- sim

  Info: Default for IP intergration.
  - src
  - dep
  - tb
  - dep_tb

3.4 Directory Guide

Below highlights important folders from the root of the directory.

1. **docs** Contains all documentation related to this project.
    - **manual** Contains user manual and github page that are generated from the latex sources.
2. **src** Contains source files for the core
3. **tb** Contains test bench files for iverilog and cocotb
    - **cocotb** testbench files

4 Simulation

There are a few different simulations that can be run for this core.

4.1 iverilog

iverilog is used for simple test benches for quick verification, visually, of the core.

4.2 cocotb

Future simulations will use cocotb. This feature is not yet implemented.

5 Module Documentation

- **dc_block_ram** Generic dual clock block RAM

The next sections document the module in great detail.

dc_block_ram.v

AUTHORS

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DATES

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INFORMATION

Brief

Generic Dual Port RAM

License MIT

dc_block_ram

```
module dc_block_ram #(
parameter
RAM_DEPTH
 =
1,
parameter
BYTE_WIDTH
 =
1,
parameter
ADDR_WIDTH
```

```
 =
1,
parameter
BIN_FILE
 =
"",
parameter
RAM_TYPE
 =
"block"
) ( input rd_clk, input rd_rstn, input rd_en, output [(BYTE_WIDTH*8)-1:0] r
```

Generic Dual Port RAM

Parameters

RAM_DEPTH Number of words using the size of BYTE_WIDTH.
parameter

BYTE_WIDTH Width of the data bus in bytes.
parameter

ADDR_WIDTH Width of the address bus in bits.
parameter

BIN_FILE Read a hex value text file as the initial state of the RAM.
parameter

RAM_TYPE Used to set the ram_style atribute.
parameter

Ports

rd_clk Read clock positive edge

rd_rstn Read reset active low

rd_en Read enable active high

rd_data Read data output

rd_addr Read data address select

wr_clk Write clock positive edge

wr_rstn Write reset active low

wr_en Write enable active high

wr_ben Write byte enable, each bit represents one byte of write data.

wr_data Write data input

wr_addr Write data address select