dc_block_ram.v

AUTHORS

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DATES

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INFORMATION

Brief

Generic Dual Port RAM

License MIT

dc_block_ram

```
module dc_block_ram #(
parameter
RAM_DEPTH
 =
1,
parameter
BYTE_WIDTH
 =
1,
parameter
ADDR_WIDTH
```

```
 =
1,
parameter
HEX_FILE
 =
"",
parameter
RAM_TYPE
 =
"block"
) ( input rd_clk, input rd_rstn, input rd_en, output [(BYTE_WIDTH*8)-1:0] r
```

Generic Dual Port RAM

Parameters

RAM_DEPTH parameter	Number of words using the size of BYTE_WIDTH.
BYTE_WIDTH parameter	Width of the data bus in bytes.
ADDR_WIDTH parameter	Width of the address bus in bits.
HEX_FILE parameter	Read a hex value text file as the initial state of the RAM.
RAM_TYPE parameter	Used to set the ram_style atribute.

Ports

rd_clk	Read clock positive edge
rd_rstn	Read reset active low
rd_en	Read enable active high
rd_data	Read data output
rd_addr	Read data address select
wr_clk	Write clock positive edge
wr_rstn	Write reset active low
wr_en	Write enable active high
wr_ben	Write byte enable, each bit represents one byte of write data.
wr_data	Write data input
wr_addr	Write data address select