tb_dc_block_ram.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench for Generic Dual Port RAM

License MIT

dc_block_ram

```
module tb_dc_block_ram #(
parameter
RAM_DEPTH
 =
256,
parameter
BYTE_WIDTH
 =
4,
parameter
ADDR_WIDTH
 =
32,
parameter
```

```
HEX_FILE
  =
"",
parameter
RAM_TYPE
  =
"block"
)()
```

Test bench for Generic Dual Port RAM

Parameters

RAM_DEPTH Number of words using the size of BYTE_WIDTH.
parameter

BYTE_WIDTH Width of the data bus in bytes.
parameter

ADDR_WIDTH Width of the address bus in bits.
parameter

HEX_FILE Read a hex value text file as the initial state of the RAM.
parameter

RAM_TYPE Used to set the ram_style atribute.
parameter

INSTANTIATED MODULES

clk_stim

```
clk_stimulus #(
                                                                                .
CLOCKS(1),
                                                                                .
CLOCK_BASE(1000000),
                                                                                .
RESETS(1),
                                                                                .
RESET_BASE(2000)
) clk_stim ( .clkv(tb_dut_clk), .rstnv(tb_dut_rstn), .rstv() )
```

Generate a 50/50 duty cycle set of clocks and reset.

inst_dc_block_ram

```
dc_block_ram #(
                                                                                .
RAM_DEPTH(RAM_DEPTH),
                                                                                .
BYTE_WIDTH(BYTE_WIDTH),
                                                                                .
ADDR_WIDTH(ADDR_WIDTH),
                                                                                .
HEX_FILE(HEX_FILE),
                                                                                .
RAM_TYPE(RAM_TYPE)
) inst_dc_block_ram ( .rd_clk(tb_dut_clk), .rd_rstn(tb_dut_rstn), .rd_en(tb_
```

Module instance of dc_block_ram