

# DC\_BLOCK\_RAM



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# 1 Usage

## 1.1 Introduction

Dual clock block RAM for any FPGA target. Includes a byte enable for selecting bytes to write from the bus.

## 1.2 Dependencies

The following are the dependencies of the cores.

- fusesoc 2.X
- iverilog (simulation)
- cocotb (simulation)

### 1.2.1 fusesoc\_info Dependencies

- dep
  - AFRL:utility:helper:1.0.0
- dep\_tb
  - AFRL:simulation:clock\_stimulator
  - AFRL:utility:sim\_helper

## 1.3 In a Project

Connect the device using the read write signals see 5 for details

# 2 Architecture

This core is made up of a single module.

- **ft245\_sync\_to\_axis** Interface AXIS to F245 device (see core for documentation).

This core has 2 always blocks that are sensitive to the positive clock edge.

- **Produce Data** Takes write input data and stores it in RAM at a specified address. BE will filter out bytes if the corresponding bits not set to active high.
- **Consume Data** Read data from RAM at a specified address and output over read interface.

Please see 5 for information on read/write interface ports.

## 3 Building

The DC block RAM is written in Verilog 2001. It should synthesize in any modern FPGA software. The core comes as a fusesoc packaged core and can be included in any other core. Be sure to make sure you have met the dependencies listed in the previous section. Linting is performed by verible using the lint target.

### 3.1 fusesoc

Fusesoc is a system for building FPGA software without relying on the internal project management of the tool. Avoiding vendor lock in to Vivado or Quartus. These cores, when included in a project, can be easily integrated and targets created based upon the end developer needs. The core by itself is not a part of a system and should be integrated into a fusesoc based system. Simulations are setup to use fusesoc and are a part of its targets.

### 3.2 Source Files

#### 3.2.1 fusesoc\_info File List

- src
  - src/dc\_block\_ram.v
- tb
  - 'tb/tb\_dc\_block\_ram.v': 'file\_type': 'verilogSource'

### 3.3 Targets

#### 3.3.1 fusesoc\_info Targets

- default
  - Info: Default for IP intergration.
- lint
  - Info: Lint with Verible
- sim
  - Info: Default for IP intergration.

### 3.4 Directory Guide

Below highlights important folders from the root of the directory.

1. **docs** Contains all documentation related to this project.
  - **manual** Contains user manual and github page that are generated from the latex sources.
2. **src** Contains source files for the core
3. **tb** Contains test bench files for iverilog and cocotb

## **4 Simulation**

There are a few different simulations that can be run for this core.

### **4.1 iverilog**

iverilog is used for simple test benches for quick verification, visually, of the core.

### **4.2 cocotb**

This feature is not implemented for this core.

## 5 Module Documentation

- **dc\_block\_ram** Generic dual clock block RAM

The next sections document the module.

# dc\_block\_ram.v

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## AUTHORS

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JAY CONVERTINO

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## DATES

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2024/03/07

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## INFORMATION

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### Brief

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Generic Dual Port RAM

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## dc\_block\_ram

---

```
module dc_block_ram #(
  parameter
  RAM_DEPTH
  =
  1,
  parameter
  BYTE_WIDTH
  =
  1,
  parameter
  ADDR_WIDTH
  =
  1,
  parameter
```



```

    HEX_FILE
    =
    ""
    parameter
    RAM_TYPE
    =
    "block"
  ) ( input rd_clk, input rd_rstn, input rd_en, output [(BYTE_WIDTH*8)-1:0]

```

Generic Dual Port RAM

## Parameters

<b>RAM_DEPTH</b> <i>parameter</i>	Number of words using the size of BYTE_WIDTH.
<b>BYTE_WIDTH</b> <i>parameter</i>	Width of the data bus in bytes.
<b>ADDR_WIDTH</b> <i>parameter</i>	Width of the address bus in bits.
<b>HEX_FILE</b> <i>parameter</i>	Read a hex value text file as the initial state of the RAM.
<b>RAM_TYPE</b> <i>parameter</i>	Used to set the ram_style attribute.

## Ports

<b>rd_clk</b>	Read clock positive edge
<b>rd_rstn</b>	Read reset active low
<b>rd_en</b>	Read enable active high
<b>rd_data</b>	Read data output
<b>rd_addr</b>	Read data address select
<b>wr_clk</b>	Write clock positive edge
<b>wr_rstn</b>	Write reset active low
<b>wr_en</b>	Write enable active high
<b>wr_ben</b>	Write byte enable, each bit represents one byte of write data.
<b>wr_data</b>	Write data input
<b>wr_addr</b>	Write data address select

# tb\_dc\_block\_ram.v

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## AUTHORS

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JAY CONVERTINO

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## DATES

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2025/01/17

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## INFORMATION

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### Brief

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Test bench for Generic Dual Port RAM

### License MIT

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## dc\_block\_ram

---

```
module tb_dc_block_ram #(
  parameter
  RAM_DEPTH
  =
  256,
  parameter
  BYTE_WIDTH
  =
  4,
  parameter
  ADDR_WIDTH
  =
  32,
  parameter
```

```

    HEX_FILE
    =
    ""
    parameter
    RAM_TYPE
    =
    "block"
    )()

```

Test bench for Generic Dual Port RAM

## Parameters

<b>RAM_DEPTH</b> parameter	Number of words using the size of BYTE_WIDTH.
<b>BYTE_WIDTH</b> parameter	Width of the data bus in bytes.
<b>ADDR_WIDTH</b> parameter	Width of the address bus in bits.
<b>HEX_FILE</b> parameter	Read a hex value text file as the initial state of the RAM.
<b>RAM_TYPE</b> parameter	Used to set the ram_style attribute.

## INSTANTIATED MODULES

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### clk\_stim

---

```

clk_stimulus #(
    CLOCKS(1),
    CLOCK_BASE(1000000),
    RESETS(1),
    RESET_BASE(2000)
) clk_stim ( .clkv(tb_dut_clk), .rstnv(tb_dut_rstn), .rstv() )

```

Generate a 50/50 duty cycle set of clocks and reset.

### inst\_dc\_block\_ram

---

```

dc_block_ram #(
    RAM_DEPTH(RAM_DEPTH),
    BYTE_WIDTH(BYTE_WIDTH),
    ADDR_WIDTH(ADDR_WIDTH),
    HEX_FILE(HEX_FILE),
    RAM_TYPE(RAM_TYPE)
) inst_dc_block_ram ( .rd_clk(tb_dut_clk), .rd_rstn(tb_dut_rstn), .rd_en(tb_

```

Module instance of dc\_block\_ram