

# fifo\_pipe.v

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## AUTHORS

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JAY CONVERTINO

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## DATES

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## INFORMATION

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### Brief

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Pipe fifo signals to help with timing issues, if they arise.

### License MIT

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## fifo\_pipe

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```
module fifo_pipe #(
  parameter
  RD_SYNC_DEPTH
  =
  0,
  parameter
  WR_SYNC_DEPTH
  =
  0,
  parameter
  DC_SYNC_DEPTH
  =
  0,
  parameter
```

```

    BYTE_WIDTH
    =
    1,
    parameter
    DATA_ZERO
    =
    0,
    parameter
    COUNT_WIDTH
    =
    1
) ( input rd_clk, input rd_rstn, input rd_en, input rd_valid, input [(BYTE_V

```

Pipe fifo signals to help with timing issues, if they arise.

## Parameters

<b>BYTE_WIDTH</b> parameter	How many bytes wide the data in/out will be.
<b>COUNT_WIDTH</b> parameter	Data count output width in bits. Should be the same power of two as fifo depth(256 for fifo depth... this should be 8).
<b>RD_SYNC_DEPTH</b> parameter	Add in pipelining to read path. Defaults to 0.
<b>WR_SYNC_DEPTH</b> parameter	Add in pipelining to write path. Defaults to 0.
<b>DC_SYNC_DEPTH</b> parameter	Add in pipelining to data count path. Defaults to 0.
<b>DATA_ZERO</b> parameter	Zero out data output when enabled.

## Ports

<b>rd_clk</b>	Clock for read data
<b>rd_rstn</b>	Negative edge reset for read.
<b>rd_en</b>	Active high enable input of read interface.
<b>rd_valid</b>	Active high output input that the data is valid.
<b>rd_data</b>	Output data input
<b>rd_empty</b>	Registered Active high output when read is empty.
<b>r_rd_en</b>	Registered Active high enable of read interface.
<b>r_rd_valid</b>	Registered Active high output that the data is valid.
<b>r_rd_data</b>	Registered Output data
<b>r_rd_empty</b>	Active high output when read is empty.
<b>wr_clk</b>	Clock for write data
<b>wr_rstn</b>	Negative edge reset for write
<b>wr_en</b>	Active high enable of write interface, feed into register.
<b>wr_ack</b>	Active high when enabled, that data write has been done, feed into register.
<b>wr_data</b>	Input data, feed into register.
<b>wr_full</b>	Active high output that the FIFO is full, feed into register.
<b>r_wr_en</b>	Register Active high enable of write interface.
<b>r_wr_ack</b>	Register Active high when enabled, that data write has been done.
<b>r_wr_data</b>	Register Input data
<b>r_wr_full</b>	Register Active high output that the FIFO is full.
<b>data_count_clk</b>	Clock for data count

<b>data_count_rstn</b>	Negative edge reset for data count.
<b>data_count</b>	Output that indicates the amount of data in the FIFO.