# fifo_pipe.v

## AUTHORS

### JAY CONVERTINO

## DATES

### 2021/06/29

## INFORMATION

### Brief

Pipe fifo signals to help with timing issues, if they arise.

### License MIT



### fifo_pipe

```
module fifo_pipe #(
parameter
RD_SYNC_DEPTH
  =
0,
parameter
WR_SYNC_DEPTH
  =
0,
parameter
DC_SYNC_DEPTH
  =
0,
parameter
```

```
BYTE_WIDTH
 =
1,
parameter
DATA_ZERO
 =
0,
parameter
COUNT_WIDTH
 =
1
) ( input rd_clk, input rd_rstn, input rd_en, input rd_valid, input [(BYTE_W
```

Pipe fifo signals to help with timing issues, if they arise.

## Parameters

| | |
|---|---|
| **BYTE_WIDTH**<br>parameter | How many bytes wide the data in/out will be. |
| **COUNT_WIDTH**<br>parameter | Data count output width in bits. Should be the same power of two as fifo depth(256 for fifo depth... this should be 8). |
| **RD_SYNC_DEPTH**<br>parameter | Add in pipelining to read path. Defaults to 0. |
| **WR_SYNC_DEPTH**<br>parameter | Add in pipelining to write path. Defaults to 0. |
| **DC_SYNC_DEPTH**<br>parameter | Add in pipelining to data count path. Defaults to 0. |
| **DATA_ZERO**<br>parameter | Zero out data output when enabled. |

## Ports

| | |
|---|---|
| **rd_clk** | Clock for read data |
| **rd_rstn** | Negative edge reset for read. |
| **rd_en** | Active high enable input of read interface. |
| **rd_valid** | Active high output input that the data is valid. |
| **rd_data** | Output data input |
| **rd_empty** | Registered Active high output when read is empty. |
| **r_rd_en** | Registered Active high enable of read interface. |
| **r_rd_valid** | Registered Active high output that the data is valid. |
| **r_rd_data** | Registered Output data |
| **r_rd_empty** | Active high output when read is empty. |
| **wr_clk** | Clock for write data |
| **wr_rstn** | Negative edge reset for write |
| **wr_en** | Active high enable of write interface, feed into register. |
| **wr_ack** | Active high when enabled, that data write has been done, feed into register. |
| **wr_data** | Input data, feed into register. |
| **wr_full** | Active high output that the FIFO is full, feed into register. |
| **r_wr_en** | Register Active high enable of write interface. |
| **r_wr_ack** | Register Active high when enabled, that data write has been done. |
| **r_wr_data** | Register Input data |
| **r_wr_full** | Register Active high output that the FIFO is full. |
| **data_count_clk** | Clock for data count |

| | |
|---|---|
| **data_count_rstn** | Negative edge reset for data count. |
| **data_count** | Output that indicates the amount of data in the FIFO. |