fifo_ctrl.v

AUTHORS

JAY CONVERTINO

DATES

2021/06/29

INFORMATION

Brief

Control block for fifo operations, emulates xilinx fifo.

License MIT

fifo_ctrl

```
module fifo_ctrl #(
parameter
FIFO_DEPTH
 =
256,
parameter
BYTE_WIDTH
 =
1,
parameter
ADDR_WIDTH
```

```
 =
1,
parameter
COUNT_WIDTH
 =
1,
parameter
GREY_CODE
 =
1,
parameter
COUNT_DELAY
 =
1,
parameter
COUNT_ENA
 =
1,
parameter
ACK_ENA
 =
0,
parameter
FWFT
 =
0
) ( input rd_clk, input rd_rstn, input rd_en, output [ADDR_WIDTH-1:0] rd_ad
```

Control block for fifo operations, emulates xilinx fifo.

Parameters

FIFO_DEPTH
parameter
Depth of the fifo, must be a power of two number(divisable aka 256 = 2^8). Any non-power of two will be rounded up to the next closest.

BYTE_WIDTH
parameter
How many bytes wide the data in/out will be.

ADDR_WIDTH
parameter
Width of the RAM address bus to write data to.

COUNT_WIDTH
parameter
Data count output width in bits. Should be the same power of two as fifo depth(256 for fifo depth... this should be 8).

GREY_CODE
parameter
RAM address uses grey code instead of linear addressing.

COUNT_DELAY
parameter
Delay count by one clock cycle of the data count clock. Set this to 0 to disable (only disable if read/write/data_count are on the same clock domain!).

COUNT_ENA
parameter
Enable the count output.

ACK_ENA
parameter
Enable ack on write.

FWFT
parameter
1 for first word fall through mode. 0 for normal.

Ports

rd_clk
Clock for read data

rd_rstn
Negative edge reset for read.

rd_en
Active high enable of read interface.

rd_addr
Address to read data from in RAM.

rd_valid	Active high output that the data is valid.
rd_mem_en	Active high enable to read from RAM.
rd_empty	Active high output when read is empty.
wr_clk	Clock for write data
wr_rstn	Negative edge reset for write
wr_en	Active high enable of write interface.
wr_addr	Address to write data to in RAM.
wr_ack	Active high when enabled, that data write has been done.
wr_mem_en	Active high enable to write to RAM.
wr_full	Active high output that the FIFO is full.
data_count_clk	Clock for data count
data_count_rstn	Negative edge reset for data count.
data_count	Output that indicates the amount of data in the FIFO.