

# tb\_fifo.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Test bench for fifo using fifo stim and clock stim.

### License MIT

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## tb\_fifo

---

```
module tb_fifo #(
  parameter
    IN_FILE_NAME
    =
    in.bin,
  parameter
    OUT_FILE_NAME
    =
    out.bin,
  parameter
    FIFO_DEPTH
    =
    64,
  parameter
```

```
RAND_FULL
=
0
)()
```

Test bench for fifo. This will run a file through the system and write its output. These can then be compared to check for errors. If the files are identical, no errors. A FST file will be written.

Parameters

<b>IN_FILE_NAME</b> <i>parameter</i>	File name for input.
<b>OUT_FILE_NAME</b> <i>parameter</i>	File name for output.
<b>FIFO_DEPTH</b> <i>parameter</i>	Number of transactions to buffer.
<b>RAND_READY</b>	0 = no random ready. 1 = randomize ready.

INSTANTIATED MODULES

clk\_stim

```
clk_stimulus #(
CLOCKS(2),
CLOCK_BASE(1000000),
CLOCK_INC(1000),
RESETS(2),
RESET_BASE(2000),
RESET_INC(100)
) clk_stim ( .clkv({tb_dut_clk, tb_stim_clk}), .rstnv({tb_dut_rstn, tb_stim_rstn})
```

Generate a 50/50 duty cycle set of clocks and reset.

write\_fifo\_stimulus

```
write_fifo_stimulus #(
BYTE_WIDTH(BYTE_WIDTH),
FILE(IN_FILE_NAME)
) write_fifo_stim ( .rd_clk(tb_stim_clk), .rd_rstn(tb_stim_rstn), .rd_en(~tb_stim_rstn)
```

Device under test WRITE stimulus module.

dut

```
fifo #(

```

```

FIFO_DEPTH(FIFO_DEPTH),
BYTE_WIDTH(BYTE_WIDTH),
COUNT_WIDTH(8),
FWFT(0),
RD_SYNC_DEPTH(0),
WR_SYNC_DEPTH(0),
DC_SYNC_DEPTH(0),
COUNT_DELAY(1),
COUNT_ENA(1),
DATA_ZERO(0),
ACK_ENA(0),
RAM_TYPE("block")
) dut ( .wr_clk(tb_stim_clk), .wr_rstn(tb_stim_rstn), .wr_en(tb_stim_valid),

```

Device under test, fifo

## read\_fifo\_stimulus

```

read_fifo_stimulus #(
BYTE_WIDTH(BYTE_WIDTH),
RAND_FULL(RAND_FULL),
FILE(OUT_FILE_NAME)
) read_fifo_stim ( .wr_clk(tb_dut_clk), .wr_rstn(tb_dut_rstn), .wr_en(tb_dut

```

Device under test READ stimulus module.