

# FIFO\_STIMULATOR



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# 1 Usage

## 1.1 Introduction

This core contains two modules. A writer, and reader that should be placed on the output, and input of the device under test. This will stream data through till it has read all data.

## 1.2 Dependencies

The following are the dependencies of the cores.

- fusesoc 2.X
- iverilog (simulation)
- cocotb (simulation)

### 1.2.1 fusesoc\_info Dependencies

- dep
  - AFRL:utility:helper:1.0.0
- dep\_tb
  - AFRL:simulation:clock\_stimulator
  - AFRL:utility:sim\_helper
- dep\_vpi
  - AFRL:vpi:binary\_file\_io:1.0.0

# 2 Architecture

The project contains two modules `write_fifo_stimulus` and `read_fifo_stimulus`. The `read_fifo_stimulus` is used to take input data from the `wr_fifo` interface (input) and write it to a file. Essentially it goes `DUT_RD_FIFO` to `read_fifo_stimulus(WR_FIFO)`. `write_fifo_stimulus` is used to read a file and push that data to the `rd_fifo` interface (output). Essentially it goes `write_fifo_stimulus(WR_FIFO)` to `DUT_RD_FIFO`.

This core uses a custom library for reading and writing files called `vpi_binary_file_io`. This library provides multithreaded file reads using a ring buffer between processes. The core will also puncture data according to its bit type. X/Z values are tossed if they are contained in a byte.

- **tm\_stim\_fifo** Contains two modules write\_fifo\_stimulus and read\_fifo\_stimulus.

Please see 5 for more information per target.

## 3 Building

The all FIFO stimulator modules are written in Verilog 2001. They should synthesize in any modern FPGA software. The core comes as a fusesoc packaged core and can be included in any other core. Be sure to make sure you have meet the dependencies listed in the previous section.

### 3.1 fusesoc

Fusesoc is a system for building FPGA software without relying on the internal project management of the tool. Avoiding vendor lock in to Vivado or Quartus. These cores, when included in a project, can be easily integrated and targets created based upon the end developer needs. The core by itself is not a part of a system and should be integrated into a fusesoc based system. Simulations are setup to use fusesoc and are a part of its targets.

### 3.2 Source Files

#### 3.2.1 fusesoc\_info File List

- src
  - 'src/tm\_stim\_fifo.v': 'file\_type': 'verilogSource'
- tb
  - 'tb/tb\_fifo.v': 'file\_type': 'verilogSource'

### 3.3 Targets

#### 3.3.1 fusesoc\_info Targets

- default
  - Info: Default for simulation filesset.
- sim
  - Info: Default for icarus simulation.
- sim\_rand\_data

Info: Random data input.

- `sim_rand_full_rand_data`

Info: Random data, random ready input.

- `sim_8bit_count_data`

Info: Counter data input.

- `sim_rand_full_8bit_count_data`

Info: Counter data, random ready input.

### 3.4 Directory Guide

Below highlights important folders from the root of the directory.

1. **docs** Contains all documentation related to this project.
  - **manual** Contains user manual and github page that are generated from the latex sources.
2. **src** Contains source files for `fifo_stimulator`.
3. **tb** Contains test bench files.

## **4 Simulation**

There is no simulation at the moment. Maybe a future addition?

## 5 Module Documentation

There project has multiple modules. The targets are the top system wrappers.

- **tm\_stim\_fifo**
- **tb\_fifo**

The next sections document the module in great detail.

# tm\_stim\_fifo.v

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## AUTHORS

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JAY CONVERTINO

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## DATES

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2023/01/30

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## INFORMATION

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### Brief

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Generic FIFO test bench modules (stimulus).

### License MIT

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## write\_fifo\_stimulus

---

```
module write_fifo_stimulus #(
    parameter
    BYTE_WIDTH
    =
    1,
    parameter
    BYTE_SWAP
    =
    0,
    parameter
    FWFT
```



```

    =
    0,
    parameter
    FILE
    =
    "test.bin"
) ( input rd_clk, input rd_rstn, input rd_en, output reg rd_valid, output

```

Simulator core to read file data, and output it to write fifo dut.

## Parameters

<b>BYTE_WIDTH</b> parameter	data width in bytes for data bus
<b>BYTE_SWAP</b> parameter	swap bytes fed to the DUT
<b>FWFT</b> parameter	Turn on or off first word fall through mode.
<b>FILE</b> parameter	input file name

## Ports

<b>rd_clk</b>	Read clock
<b>rd_rstn</b>	Read reset negative
<b>rd_en</b>	enable read
<b>rd_valid</b>	read data valid
<b>rd_data</b>	read data
<b>rd_empty</b>	read has no data
<b>eof</b>	end of input file has been reached.

## read\_fifo\_stimulus

```

module read_fifo_stimulus #(
    parameter
    BYTE_WIDTH
    =
    1,
    parameter
    ACK_ENA
    =
    0,
    parameter
    RAND_FULL
    =
    0,
    parameter
    FILE
    =
    "out.bin"
) ( input wr_clk, input wr_rstn, input wr_en, output reg wr_ack, input [(B\

```

Simulator core to write file data, from input over write fifo dut. This module will keep a constant ready to the dut.

## Parameters

<b>BYTE_WIDTH</b> parameter	data width in bytes for data bus
<b>ACK_ENA</b> parameter	enable ack if set to 1 (does nothing at the moment, ack is not used)
<b>RAND_FULL</b> parameter	randomize the full output signal
<b>FILE</b> parameter	output file name

## Ports

<b>wr_clk</b>	Write clock
<b>wr_rstn</b>	Write reset negative
<b>wr_en</b>	enable write
<b>wr_ack</b>	write data has been written
<b>wr_data</b>	write data
<b>wr_full</b>	can't write data, destination is full.
<b>eof</b>	Exit if end of file is reached.

## tb\_fifo.v

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### AUTHORS

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JAY CONVERTINO

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### DATES

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2023/01/30

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### INFORMATION

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#### Brief

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Generic FIFO test bench top.

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## tb\_axis

---

Generic AXIS test bench top with verification.

#### Parameters

<b>IN_FILE_NAME</b>	Name of the input file to read from.
<b>OUT_FILE_NAME</b>	Name of the output file to write.
<b>RAND_FULL</b>	Randomize the full signal from the writer (read_fifo_stimulus) core.

## INSTANTIATED MODULES

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### clk\_stim

---

```
clk_stimulus #(
    CLOCKS(1),
    CLOCK_BASE(1000000),
    CLOCK_INC(1000),
    RESETS(1),
    RESET_BASE(2000),
    RESET_INC(100)
) clk_stim ( .clkv(tb_stim_clk), .rstnv(tb_stim_rstn), .rstv() )
```

Generate a clock for the modules.

### write\_fifo\_stim

---

```
write_fifo_stimulus #(
    BYTE_WIDTH(BUS_WIDTH),
    FILE(IN_FILE_NAME)
) write_fifo_stim ( .rd_clk(tb_stim_clk), .rd_rstn(tb_stim_rstn), .rd_en(~tb_stim_rstn) )
```

Read a file and output to a wr\_fifo interface from the read.

### read\_fifo\_stim

---

```
read_fifo_stimulus #(
    BYTE_WIDTH(BUS_WIDTH),
    RAND_FULL(RAND_FULL),
    FILE(OUT_FILE_NAME)
) read_fifo_stim ( .wr_clk(tb_stim_clk), .wr_rstn(tb_stim_rstn), .wr_en(tb_stim_rstn) )
```

Write a file from the input from a rd\_fifo interface to the write.