

# tb\_fifo.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Generic FIFO test bench top.

### License MIT

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## tb\_axis

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Generic AXIS test bench top with verification.

### Parameters

<b>IN_FILE_NAME</b>	Name of the input file to read from.
<b>OUT_FILE_NAME</b>	Name of the output file to write.
<b>RAND_FULL</b>	Randomize the full signal from the writer (read_fifo_stimulus) core.

## INSTANTIATED MODULES

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### clk\_stim

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```
clk_stimulus #(
    CLOCKS(1),
    CLOCK_BASE(1000000),
    CLOCK_INC(1000),
    RESETS(1),
    RESET_BASE(2000),
    RESET_INC(100)
) clk_stim ( .clkv(tb_stim_clk), .rstnv(tb_stim_rstn), .rstv() )
```

Generate a clock for the modules.

### write\_fifo\_stim

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```
write_fifo_stimulus #(
    BYTE_WIDTH(BUS_WIDTH),
    FILE(IN_FILE_NAME)
) write_fifo_stim ( .rd_clk(tb_stim_clk), .rd_rstn(tb_stim_rstn), .rd_en(~tb_stim_rstn) )
```

Read a file and output to a wr\_fifo interface from the read.

### read\_fifo\_stim

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```
read_fifo_stimulus #(
    BYTE_WIDTH(BUS_WIDTH),
    RAND_FULL(RAND_FULL),
    FILE(OUT_FILE_NAME)
) read_fifo_stim ( .wr_clk(tb_stim_clk), .wr_rstn(tb_stim_rstn), .wr_en(tb_stim_rstn) )
```

Write a file from the input from a rd\_fifo interface to the write.