

tm_stim_fifo.v

AUTHORS

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DATES

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INFORMATION

Brief

Generic FIFO test bench modules (stimulus).

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write_fifo_stimulus

```
module write_fifo_stimulus #(
  parameter
  BYTE_WIDTH
  =
  1,
  parameter
  BYTE_SWAP
  =
  0,
  parameter
  FWFT
```

```

    =
    0,
    parameter
    FILE
    =
    "test.bin"
  ) ( input rd_clk, input rd_rstn, input rd_en, output reg rd_valid, output

```

Simulator core to read file data, and output it to write fifo dut.

Parameters

BYTE_WIDTH parameter	data width in bytes for data bus
BYTE_SWAP parameter	swap bytes fed to the DUT
FWFT parameter	Turn on or off first word fall through mode.
FILE parameter	input file name

Ports

rd_clk	Read clock
rd_rstn	Read reset negative
rd_en	enable read
rd_valid	read data valid
rd_data	read data
rd_empty	read has no data
eof	end of input file has been reached.

read_fifo_stimulus

```

module read_fifo_stimulus #(
  parameter
  BYTE_WIDTH
  =
  1,
  parameter
  ACK_ENA
  =
  0,
  parameter
  RAND_FULL
  =
  0,
  parameter
  FILE
  =
  "out.bin"
) ( input wr_clk, input wr_rstn, input wr_en, output reg wr_ack, input [(B\

```

Simulator core to write file data, from input over write fifo dut. This module will keep a constant ready to the dut.

Parameters

BYTE_WIDTH parameter	data width in bytes for data bus
ACK_ENA parameter	enable ack if set to 1 (does nothing at the moment, ack is not used)
RAND_FULL parameter	randomize the full output signal
FILE parameter	output file name

Ports

wr_clk	Write clock
wr_rstn	Write reset negative
wr_en	enable write
wr_ack	write data has been written
wr_data	write data
wr_full	can't write data, destination is full.
eof	Exit if end of file is reached.