# tb fifo.v

### **AUTHORS**

## **JAY CONVERTINO**

### **DATES**

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## **INFORMATION**

### **Brief**

Generic FIFO test bench top.

## **License MIT**

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#### tb axis

Generic AXIS test bench top with verification.

#### **Parameters**

IN\_FILE\_NAMEOUT\_FILE\_NAMEName of the output file to write.

**RAND\_FULL** Randomize the full signal from the writer (read\_fifo\_stimulus) core.

## **INSTANTIANTED MODULES**

# clk\_stim

Generate a clock for the modules.

# write\_fifo\_stim

```
write_fifo_stimulus #(

BYTE_WIDTH(BUS_WIDTH),

FILE(IN_FILE_NAME)
) write_fifo_stim ( .rd_clk(tb_stim_clk), .rd_rstn(tb_stim_rstn), .rd_en(~tt
```

Read a file and output to a wr\_fifo interface from the read.

# read\_fifo\_stim

Write a file from the input from a rd\_fifo interface to the write.