# system\_wrapper.v

#### **AUTHORS**

# **JAY CONVERTINO**

## **DATES**

#### 2023/12/17

# **INFORMATION**

## **Brief**

System wrapper for pl and ps for arria10soc board.

## **License MIT**

Copyright 2023 Jay Convertino

Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions:

The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software.

THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

# system\_wrapper

```
module system_wrapper #(
parameter
FPGA_TECHNOLOGY
=
103,
parameter
FPGA_FAMILY
=
1,
parameter
SPEED_GRADE
```

```
parameter
DEV_PACKAGE

a

parameter
DELAY_REFCLK_FREQUENCY

parameter
ADC_INIT_DELAY

parameter
ADC_INIT_DELAY

index

a

parameter
DAC_INIT_DELAY

index

index

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hr

input sys_clk, input sys_resetn, input sys_resetn,
```

System wrapper for pl and ps for arria10soc board.

#### **Parameters**

**FPGA TECHNOLOGY** Type of FPGA, such as Ultrascale, Arria 10. 103 is for Arria

meter

**FPGA\_FAMILY** Sub type of fpga, such as GX, SX, etc. 1 is for SX

parameter

**SPEED\_GRADE** Number that corresponds to the ships recommended

parameter speed. 2 is for 2.

**DEV\_PACKAGE** Specify a number that is equal to the manufactures

parameter package. 3 is for FBGA.

**DELAY\_REFCLK\_FREQUENCY** Reference clock frequency used for ad\_data\_in instances

parameter

ADC\_INIT\_DELAY Initial Delay for the ADC

parameter

**DAC\_INIT\_DELAY** Initial Delay for the DAC

oarameter

#### **Ports**

sys\_clkInput clock for all clockssys\_resetnInput reset for all resets

hps\_ddr\_ref\_clk DDR port hps\_ddr\_clk\_p DDR port hps\_ddr\_clk\_n DDR port hps\_ddr\_a DDR port hps\_ddr\_ba DDR port hps\_ddr\_bg DDR port hps\_ddr\_cke DDR port hps\_ddr\_cs\_n DDR port hps\_ddr\_odt DDR port hps\_ddr\_reset\_n DDR port hps\_ddr\_act\_n DDR port

hps\_ddr\_parDDR porthps\_ddr\_alert\_nDDR porthps\_ddr\_dqs\_pDDR porthps\_ddr\_dqDDR porthps\_ddr\_ddinDDR porthps\_ddr\_dbi\_nDDR porthps\_ddr\_rzqDDR port

hps\_eth\_rxclk **Ethernet Device** hps\_eth\_rxctl **Ethernet Device** hps\_eth\_rxd **Ethernet Device** hps\_eth\_txclk **Ethernet Device** hps\_eth\_txctl **Ethernet Device** hps\_eth\_txd **Ethernet Device** Ethernet Device hps\_eth\_mdc hps\_eth\_mdio Ethernet Device hps\_sdio\_clk SD card interface hps\_sdio\_cmd SD card interface hps\_sdio\_d SD card interface hps\_usb\_clk USB interface hps\_usb\_dir **USB** interface hps\_usb\_nxt USB interface hps usb stp USB interface hps\_usb\_d USB interface hps\_uart\_rx **UART** interface hps\_uart\_tx **UART** interface hps\_i2c\_sda i2c interface hps\_i2c\_scl i2c interface hps\_gpio **GPIO** interface gpio\_bd\_i fmcomms2-3 gpio

gpio\_bd\_o

rx\_clk\_in fmcomms2-3 receive clock in rx\_frame\_in\_p fmcomms2-3 receive frame rx\_frame\_in\_n fmcomms2-3 receive frame rx data in p fmcomms2-3 receive lvds data rx\_data\_in\_n fmcomms2-3 receive lvds data tx\_clk\_out\_p fmcomms2-3 transmit clock tx\_clk\_out\_n fmcomms2-3 transmit clock fmcomms2-3 transmit frame tx\_frame\_out\_p tx\_frame\_out\_n fmcomms2-3 transmit frame tx data out p fmcomms2-3 transmit lvds data tx data out n fmcomms2-3 transmit lvds data

fmcomms2-3 gpio

**enable** fmcomms2-3 enable

fmcomms2-3 txnrx select txnrx gpio\_resetb fmcomms2-3 gpio reset gpio\_sync fmcomms2-3 gpio sync gpio\_en\_agc fmcomms2-3 gpio enable agc fmcomms2-3 control gpio\_ctl fmcomms2-3 status gpio\_status spi\_csn fmcomms2-3 spi select spi\_clk fmcomms2-3 spi clk spi mosi fmcomms2-3 spi output spi\_miso fmcomms2-3 spi input

## **INSTANTIANTED MODULES**

# inst system pl wrapper

```
system_pl_wrapper #(

FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),

FPGA_FAMILY(FPGA_FAMILY),

SPEED_GRADE(SPEED_GRADE),

DEV_PACKAGE(DEV_PACKAGE),

ADC_INIT_DELAY(ADC_INIT_DELAY),

DAC_INIT_DELAY(DAC_INIT_DELAY),

DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)

) inst_system_pl_wrapper ( .axi_aclk(s_axi_clk), .axi_aresetn(s_axi_aresetn))
```

Module instance of system\_pl\_wrapper for the fmcomms2-3 device.

# inst\_system\_ps\_wrapper

```
system_ps_wrapper inst_system_ps_wrapper (
    s_axi_clk_clk(s_axi_clk),
    s_axi_aresetn_reset_n(s_axi_aresetn),
    m_axi_awaddr(w_axi_awaddr),
    m_axi_awprot(w_axi_awprot),
    m_axi_awvalid(w_axi_awvalid),
    m_axi_awready(w_axi_awready),
    m_axi_wdata(w_axi_wdata),
    m_axi_wstrb(w_axi_wstrb),
```

```
m_axi_wvalid(w_axi_wvalid),
m_axi_wready(w_axi_wready),
m_axi_bresp(w_axi_bresp),
m_axi_bvalid(w_axi_bvalid),
m_axi_bready(w_axi_bready),
m_axi_araddr(w_axi_araddr),
m_axi_arprot(w_axi_arprot),
m_axi_arvalid(w_axi_arvalid),
m_axi_arready(w_axi_arready),
m_axi_rdata(w_axi_rdata),
m_axi_rresp(w_axi_rresp),
m_axi_rvalid(w_axi_rvalid),
m_axi_rready(w_axi_rready),
sys_delay_clk_clk(s_delay_clk),
sys_clk_clk(sys_clk),
sys_gpio_bd_in_port(gpio_i[31:0]),
sys_gpio_bd_out_port(gpio_o[31:0]),
sys_gpio_in_export(gpio_i[63:32]),
sys_gpio_out_export(gpio_o[63:32]),
sys_hps_rstn_reset_n
sys_resetn),
sys_rstn_reset_n
sys_resetn_s),
sys_hps_io_hps_io_phery_emac0_TX_CLK
hps_eth_txclk),
sys\_hps\_io\_hps\_io\_phery\_emac0\_TXD0
hps_eth_txd[0]),
sys_hps_io_hps_io_phery_emac0_TXD1
hps_eth_txd[1]),
sys\_hps\_io\_hps\_io\_phery\_emac0\_TXD2
hps_eth_txd[2]),
sys_hps_io_hps_io_phery_emac0_TXD3
hps_eth_txd[3]),
```

```
sys_hps_io_hps_io_phery_emac0_RX_CTL
                                                                          (
hps_eth_rxctl),
sys_hps_io_hps_io_phery_emac0_TX_CTL
                                                                          (
hps_eth_txctl),
sys_hps_io_hps_io_phery_emac0_RX_CLK
                                                                          (
hps_eth_rxclk),
sys_hps_io_hps_io_phery_emac0_RXD0
                                                                          (
hps_eth_rxd[0]),
sys_hps_io_hps_io_phery_emac0_RXD1
                                                                          (
hps_eth_rxd[1]),
sys_hps_io_hps_io_phery_emac0_RXD2
                                                                          (
hps_eth_rxd[2]),
sys_hps_io_hps_io_phery_emac0_RXD3
                                                                          (
hps_eth_rxd[3]),
sys_hps_io_hps_io_phery_emac0_MDIO
hps_eth_mdio),
sys_hps_io_hps_io_phery_emac0_MDC
hps_eth_mdc),
sys_hps_io_hps_io_phery_sdmmc_CMD
hps_sdio_cmd),
sys\_hps\_io\_hps\_io\_phery\_sdmmc\_D0
                                                                          (
hps_sdio_d[0]),
sys_hps_io_hps_io_phery_sdmmc_D1
                                                                          (
hps_sdio_d[1]),
sys_hps_io_hps_io_phery_sdmmc_D2
                                                                          (
hps_sdio_d[2]),
sys_hps_io_hps_io_phery_sdmmc_D3
                                                                          (
hps_sdio_d[3]),
sys_hps_io_hps_io_phery_sdmmc_D4
                                                                          (
hps_sdio_d[4]),
sys_hps_io_hps_io_phery_sdmmc_D5
                                                                          (
hps_sdio_d[5]),
sys\_hps\_io\_hps\_io\_phery\_sdmmc\_D6
```

```
(
hps_sdio_d[6]),
sys_hps_io_hps_io_phery_sdmmc_D7
                                                                          (
hps_sdio_d[7]),
sys_hps_io_hps_io_phery_sdmmc_CCLK
                                                                          (
hps_sdio_clk),
sys\_hps\_io\_hps\_io\_phery\_usb0\_DATA0
hps_usb_d[0]),
sys_hps_io_hps_io_phery_usb0_DATA1
                                                                          (
hps_usb_d[1]),
sys_hps_io_hps_io_phery_usb0_DATA2
                                                                          (
hps_usb_d[2]),
sys_hps_io_hps_io_phery_usb0_DATA3
                                                                          (
hps_usb_d[3]),
sys_hps_io_hps_io_phery_usb0_DATA4
                                                                          (
hps_usb_d[4]),
sys_hps_io_hps_io_phery_usb0_DATA5
                                                                          (
hps_usb_d[5]),
sys_hps_io_hps_io_phery_usb0_DATA6
                                                                          (
hps_usb_d[6]),
sys_hps_io_hps_io_phery_usb0_DATA7
                                                                          (
hps_usb_d[7]),
sys_hps_io_hps_io_phery_usb0_CLK
                                                                          (
hps_usb_clk),
sys_hps_io_hps_io_phery_usb0_STP
                                                                          (
hps_usb_stp),
sys_hps_io_hps_io_phery_usb0_DIR
hps_usb_dir),
sys\_hps\_io\_hps\_io\_phery\_usb0\_NXT
hps_usb_nxt),
sys_hps_io_hps_io_phery_uart1_RX
                                                                          (
hps_uart_rx),
sys_hps_io_hps_io_phery_uart1_TX
                                                                          (
hps_uart_tx),
```

```
sys_hps_io_hps_io_phery_i2c1_SDA
                                                                         (
hps_i2c_sda),
sys_hps_io_hps_io_phery_i2c1_SCL
                                                                         (
hps_i2c_scl),
sys_hps_io_hps_io_gpio_gpio1_io5
                                                                         (
hps_gpio[0]),
sys_hps_io_hps_io_gpio_gpio1_io14
                                                                         (
hps_gpio[1]),
sys_hps_io_hps_io_gpio_gpio1_io16
                                                                         (
hps_gpio[2]),
sys_hps_io_hps_io_gpio_gpio1_io17
                                                                         (
hps_gpio[3]),
sys_hps_out_rstn_reset_n
                                                                         (
sys_hps_resetn),
sys_hps_fpga_irq1_irq
                                                                        ({
32{1'b0}}),
sys_hps_dma_data_awid(0),
sys_hps_dma_data_awaddr(adc_hp0_axi_awaddr),
sys_hps_dma_data_awlen(adc_hp0_axi_awlen),
sys_hps_dma_data_awsize(adc_hp0_axi_awsize),
sys_hps_dma_data_awburst(adc_hp0_axi_awburst),
sys_hps_dma_data_awlock(0),
sys_hps_dma_data_awcache(adc_hp0_axi_awcache),
sys_hps_dma_data_awprot(adc_hp0_axi_awprot),
sys_hps_dma_data_awvalid(adc_hp0_axi_awvalid),
sys_hps_dma_data_awready(adc_hp0_axi_awready),
sys_hps_dma_data_awuser(0),
sys_hps_dma_data_wid(0),
sys_hps_dma_data_wdata(adc_hp0_axi_wdata),
sys_hps_dma_data_wstrb(adc_hp0_axi_wstrb),
sys_hps_dma_data_wlast(adc_hp0_axi_wlast),
sys_hps_dma_data_wvalid(adc_hp0_axi_wvalid),
sys_hps_dma_data_wready(adc_hp0_axi_wready),
```

```
sys_hps_dma_data_bid(),
sys_hps_dma_data_bresp(adc_hp0_axi_bresp),
sys_hps_dma_data_bvalid(adc_hp0_axi_bvalid),
sys_hps_dma_data_bready(adc_hp0_axi_bready),
sys_hps_dma_data_arid(0),
sys_hps_dma_data_araddr(dac_hp1_axi_araddr),
sys_hps_dma_data_arlen(dac_hp1_axi_arlen),
sys_hps_dma_data_arsize(dac_hp1_axi_arsize),
sys_hps_dma_data_arburst(dac_hp1_axi_arburst),
sys_hps_dma_data_arlock(0),
sys_hps_dma_data_arcache(dac_hp1_axi_arcache),
sys_hps_dma_data_arprot(dac_hp1_axi_arprot),
sys_hps_dma_data_arvalid(dac_hp1_axi_arvalid),
sys_hps_dma_data_arready(dac_hp1_axi_arready),
sys_hps_dma_data_aruser(0),
sys_hps_dma_data_rid(),
sys_hps_dma_data_rdata(dac_hp1_axi_rdata),
sys_hps_dma_data_rresp(dac_hp1_axi_rresp),
sys_hps_dma_data_rlast(dac_hp1_axi_rlast),
sys_hps_dma_data_rvalid(dac_hp1_axi_rvalid),
sys_hps_dma_data_rready(dac_hp1_axi_rready),
sys_hps_ddr_mem_ck(hps_ddr_clk_p),
sys_hps_ddr_mem_ck_n(hps_ddr_clk_n),
sys_hps_ddr_mem_a(hps_ddr_a),
sys_hps_ddr_mem_act_n(hps_ddr_act_n),
sys_hps_ddr_mem_ba(hps_ddr_ba),
sys_hps_ddr_mem_bg(hps_ddr_bg),
sys_hps_ddr_mem_cke(hps_ddr_cke),
sys_hps_ddr_mem_cs_n(hps_ddr_cs_n),
sys\_hps\_ddr\_mem\_odt(hps\_ddr\_odt),
sys_hps_ddr_mem_reset_n(hps_ddr_reset_n),
sys_hps_ddr_mem_par(hps_ddr_par),
sys_hps_ddr_mem_alert_n(hps_ddr_alert_n),
```

```
sys_hps_ddr_mem_dqs(hps_ddr_dqs_p),
sys_hps_ddr_mem_dqs_n(hps_ddr_dqs_n),
sys_hps_ddr_mem_dq(hps_ddr_dq),
sys_hps_ddr_mem_dbi_n(hps_ddr_dbi_n),
sys_hps_ddr_oct_oct_rzqin(hps_ddr_rzq),
sys_hps_ddr_ref_clk_clk(hps_ddr_ref_clk),
sys_hps_ddr_rstn_reset_n(sys_resetn),
sys_spi_MISO(spi_miso),
sys_spi_MOSI(spi_mosi),
sys_spi_SCLK(spi_clk),
sys_spi_SS_n(spi_csn),
irq_irq({s_dac_dma_irq, s_adc_dma_irq, {2{1'b0}}})
```

Module instance of inst\_system\_ps\_wrapper for the built in CPU.