

# system\_pl\_wrapper.v

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## AUTHORS

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JAY CONVERTINO

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## DATES

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## INFORMATION

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### Brief

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System wrapper for pl only for zed board.

### License MIT

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## system\_pl\_wrapper

---

```
module system_pl_wrapper #(
    parameter
    FPGA_TECHNOLOGY
    =
    0,
    parameter
    FPGA_FAMILY
    =
    0,
    parameter
    SPEED_GRADE
```

```

    =
    0,
    parameter
    DEV_PACKAGE
    =
    0,
    parameter
    ADC_INIT_DELAY
    =
    23,
    parameter
    DAC_INIT_DELAY
    =
    0,
    parameter
    DELAY_REFCLK_FREQUENCY
    =
    200
) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_

```

System wrapper for pl only for zed board.

## Parameters

<b>FPGA_TECHNOLOGY</b> parameter	Type of FPGA, such as Ultrascale, Arria 10. 1 is for 7 series.
<b>FPGA_FAMILY</b> parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
<b>SPEED_GRADE</b> parameter	Number that corresponds to the ships recommeneded speed. 20 is for -2.
<b>DEV_PACKAGE</b> parameter	Specify a number that is equal to the manufactures package. 3 is for ff.
<b>DELAY_REFCLK_FREQUENCY</b> parameter	Reference clock frequency used for ad_data_in instances
<b>ADC_INIT_DELAY</b> parameter	Initial Delay for the ADC
<b>DAC_INIT_DELAY</b> parameter	Initial Delay for the DAC

## Ports

<b>axi_aclk</b>	AXI Lite control bus
<b>axi_aresetn</b>	AXI Lite control bus
<b>s_axi_awvalid</b>	AXI Lite control bus
<b>s_axi_awaddr</b>	AXI Lite control bus
<b>s_axi_awready</b>	AXI Lite control bus
<b>s_axi_awprot</b>	AXI Lite control bus
<b>s_axi_wvalid</b>	AXI Lite control bus
<b>s_axi_wdata</b>	AXI Lite control bus
<b>s_axi_wstrb</b>	AXI Lite control bus
<b>s_axi_wready</b>	AXI Lite control bus
<b>s_axi_bvalid</b>	AXI Lite control bus
<b>s_axi_bresp</b>	AXI Lite control bus
<b>s_axi_bready</b>	AXI Lite control bus

<b>s_axi_arvalid</b>	AXI Lite control bus
<b>s_axi_araddr</b>	AXI Lite control bus
<b>s_axi_arready</b>	AXI Lite control bus
<b>s_axi_arprot</b>	AXI Lite control bus
<b>s_axi_rvalid</b>	AXI Lite control bus
<b>s_axi_rready</b>	AXI Lite control bus
<b>s_axi_rresp</b>	AXI Lite control bus
<b>s_axi_rdata</b>	AXI Lite control bus
<b>adc_dma_irq</b>	fmcomms2-3 ADC irq
<b>dac_dma_irq</b>	fmcomms2-3 DAC irq
<b>delay_clk</b>	fmcomms2-3 delay clock
<b>rx_clk_in_p</b>	fmcomms2-3 receive clock in
<b>rx_clk_in_n</b>	fmcomms2-3 receive clock in
<b>rx_frame_in_p</b>	fmcomms2-3 receive frame
<b>rx_frame_in_n</b>	fmcomms2-3 receive frame
<b>rx_data_in_p</b>	fmcomms2-3 receive lvds data
<b>rx_data_in_n</b>	fmcomms2-3 receive lvds data
<b>tx_clk_out_p</b>	fmcomms2-3 transmit clock
<b>tx_clk_out_n</b>	fmcomms2-3 transmit clock
<b>tx_frame_out_p</b>	fmcomms2-3 transmit frame
<b>tx_frame_out_n</b>	fmcomms2-3 transmit frame
<b>tx_data_out_p</b>	fmcomms2-3 transmit lvds data
<b>tx_data_out_n</b>	fmcomms2-3 transmit lvds data
<b>enable</b>	fmcomms2-3 enable
<b>txnrx</b>	fmcomms2-3 txnrx select
<b>up_enable</b>	fmcomms2-3 enable input
<b>up_txnrx</b>	fmcomms2-3 txnrx select input
<b>tdd_sync_t</b>	fmcomms2-3 TDD sync i/o
<b>tdd_sync_i</b>	fmcomms2-3 TDD sync i/o
<b>tdd_sync_o</b>	fmcomms2-3 TDD sync i/o
<b>adc_m_dest_axi_awaddr</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awlen</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awsz</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awburst</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awprot</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awcache</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awvalid</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awready</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_wdata</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_wstrb</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_wready</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_wvalid</b>	fmcomms2-3 ADC DMA

<b>adc_m_dest_axi_wlast</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_bvalid</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_bresp</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_bready</b>	fmcomms2-3 ADC DMA
<b>dac_m_src_axi_arready</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arvalid</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_araddr</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arlen</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arsize</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arburst</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arprot</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arcache</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_rdata</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_rready</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_rvalid</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_rresp</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_rlast</b>	fmcomms2-3 DAC DMA
<b>iic_sda_fmc</b>	i2c for fmc
<b>iic_scl_fmc</b>	i2c for fmc
<b>iic2intc_irpt</b>	i2c for fmc

## INSTANTIATED MODULES

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### iic\_sda\_iobuf

---

```
ad_iobuf #(
    DATA_WIDTH(1)
) iic_sda_iobuf ( .dio_t (sda_t), .dio_i (sda_o), .dio_o (sda_i), .dio_p (sda_i))
```

Tristate i2c sda

### iic\_scl\_iobuf

---

```
ad_iobuf #(
    DATA_WIDTH(1)
) iic_scl_iobuf ( .dio_t (scl_t), .dio_i (scl_o), .dio_o (scl_i), .dio_p (scl_i))
```

Tristate i2c scl

### inst\_ad9361\_pl\_wrapper

---

```
ad9361_pl_wrapper #()
```

```

FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
FPGA_FAMILY(FPGA_FAMILY),
SPEED_GRADE(SPEED_GRADE),
DEV_PACKAGE(DEV_PACKAGE),
ADC_INIT_DELAY(ADC_INIT_DELAY),
DAC_INIT_DELAY(DAC_INIT_DELAY),
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_ad9361_pl_wrapper ( .axi_aclk(axi_aclk), .axi_aresetn(axi_aresetn),

```

Module instance of ad9361\_pl\_wrapper for the fmcomms2-3 device.

## inst\_axi\_crossbar\_pl

```

axi_crossbar_pl inst_axi_crossbar_pl (
aclk(axi_aclk),
aresetn(axi_aresetn),
s_axi_awaddr(s_axi_awaddr),
s_axi_awprot(s_axi_awprot),
s_axi_awvalid(s_axi_awvalid),
s_axi_awready(s_axi_awready),
s_axi_wdata(s_axi_wdata),
s_axi_wstrb(s_axi_wstrb),
s_axi_wvalid(s_axi_wvalid),
s_axi_wready(s_axi_wready),
s_axi_bresp(s_axi_bresp),
s_axi_bvalid(s_axi_bvalid),
s_axi_bready(s_axi_bready),
s_axi_araddr(s_axi_araddr),
s_axi_arprot(s_axi_arprot),
s_axi_arvalid(s_axi_arvalid),
s_axi_arready(s_axi_arready),
s_axi_rdata(s_axi_rdata),
s_axi_rresp(s_axi_rresp),
s_axi_rvalid(s_axi_rvalid),
s_axi_rready(s_axi_rready),

```

```

m_axi_awaddr({iic_fmc_axi_awaddr, connect_axi_awaddr}),
m_axi_awprot({iic_fmc_axi_awprot, connect_axi_awprot}),
m_axi_awvalid({iic_fmc_axi_awvalid, connect_axi_awvalid}),
m_axi_awready({iic_fmc_axi_awready, connect_axi_awready}),
m_axi_wdata({iic_fmc_axi_wdata, connect_axi_wdata}),
m_axi_wstrb({iic_fmc_axi_wstrb, connect_axi_wstrb}),
m_axi_wvalid({iic_fmc_axi_wvalid, connect_axi_wvalid}),
m_axi_wready({iic_fmc_axi_wready, connect_axi_wready}),
m_axi_bresp({iic_fmc_axi_bresp, connect_axi_bresp}),
m_axi_bvalid({iic_fmc_axi_bvalid, connect_axi_bvalid}),
m_axi_bready({iic_fmc_axi_bready, connect_axi_bready}),
m_axi_araddr({iic_fmc_axi_araddr, connect_axi_araddr}),
m_axi_arprot({iic_fmc_axi_arprot, connect_axi_arprot}),
m_axi_arvalid({iic_fmc_axi_arvalid, connect_axi_arvalid}),
m_axi_arready({iic_fmc_axi_arready, connect_axi_arready}),
m_axi_rdata({iic_fmc_axi_rdata, connect_axi_rdata}),
m_axi_rresp({iic_fmc_axi_rresp, connect_axi_rresp}),
m_axi_rvalid({iic_fmc_axi_rvalid, connect_axi_rvalid}),
m_axi_rready({iic_fmc_axi_rready, connect_axi_rready})
)

```

Module instance of axi\_crossbar\_pl for the fmcomms2-3 device.

## inst\_axi\_iic\_fmc

```

axi_iic_fmc inst_axi_iic_fmc (
s_axi_aclk(axi_aclk),
s_axi_aresetn(axi_aresetn),
iic2intc_irpt(iic2intc_irpt),
s_axi_awaddr(iic_fmc_axi_awaddr[8:0]),
s_axi_awvalid(iic_fmc_axi_awvalid),
s_axi_awready(iic_fmc_axi_awready),
s_axi_wdata(iic_fmc_axi_wdata),
s_axi_wstrb(iic_fmc_axi_wstrb),
s_axi_wvalid(iic_fmc_axi_wvalid),

```

```

s_axi_wready(iic_fmc_axi_wready),
s_axi_bresp(iic_fmc_axi_bresp),
s_axi_bvalid(iic_fmc_axi_bvalid),
s_axi_bready(iic_fmc_axi_bready),
s_axi_araddr(iic_fmc_axi_araddr[8:0]),
s_axi_arvalid(iic_fmc_axi_arvalid),
s_axi_arready(iic_fmc_axi_arready),
s_axi_rdata(iic_fmc_axi_rdata),
s_axi_rresp(iic_fmc_axi_rresp),
s_axi_rvalid(iic_fmc_axi_rvalid),
s_axi_rready(iic_fmc_axi_rready),
sda_i(sda_i),
sda_o(sda_o),
sda_t(sda_t),
scl_i(scl_i),
scl_o(scl_o),
scl_t(scl_t),
gpo()
)

```

Module instance of axi\_iic\_fmc for the fmcomms2-3 device.