FMCOMMS2-3

AFRL

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Contents

1 Usage

1.1 Introduction

The fmcomms2-3 project builds a FPGA base system for the fmcomms2 and fmcomms3 Analog Devices development boards. Project targets are listed in 3.3. The base IP for the Analog Devices parts are from the Analog Devices HDL repo. They have been converted into fusesoc cores and some modifications have been made. Modifications include making the ADC/DAC routes both use AXIS out of the DMAs. The Intel FPGA targets now uses ad_data/ad_clock cores, clock select, and DC filter to reach functionally on par with Xilinx targets.

1.2 Dependencies

The following are the dependencies of the cores.

- fusesoc 2.X
- iverilog (simulation)
- cocotb (simulation)

1.2.1 fusesoc_info Depenecies

- zed
  - AFRL:utility:digilent_zed_board_base:1.0.0
  - AFRL:utility:vivado_board_support_packages
  - AD:common:ad_iobuf:1.0.0
- zed_bootgen
  - AFRL:utility:digilent_zed_boot_gen:1.0.0
- zc706
  - AFRL:utility:xilinx_zc706_board_base:1.0.0
  - AFRL:utility:vivado_board_support_packages
  - AD:common:ad_iobuf:1.0.0
- zc706_bootgen
  - AFRL:utility:xilinx_zc706_boot_gen:1.0.0
- zc702
  - AFRL:utility:xilinx_zc702_board_base:1.0.0

  - AFRL:utility:vivado_board_support_packages
  - AD:common:ad_iobuf:1.0.0

- zc702_bootgen
  - AFRL:utility:xilinx_zc702_boot_gen:1.0.0
- zcu102
  - AFRL:utility:xilinx_zcu102_board_base:1.0.0
  - AFRL:utility:vivado_board_support_packages
- zcu102_bootgen
  - AFRL:utility:xilinx_zcu102_boot_gen:1.0.0
- hanpilot
  - AFRL:utility:terasic_hanpilot_board_base:1.0.0
- hanpilot_bootgen
  - AFRL:utility:terasic_hanpilot_boot_gen:1.0.0
- a10soc
  - AFRL:utility:intel_a10soc_board_base:1.0.0
- a10soc_bootgen
  - AFRL:utility:intel_a10soc_boot_gen:1.0.0
- dep
  - AD:RF_Transceiver:axi_ad9361:1.0.0
  - AD:utility:tdd_sync:1.0.0
  - AD:memory_controller:axi_dmac:1.0.0
  - AD:data_flow:util_cpack_axis:1.0.0
  - AD:data_flow:util_upack:2.0.0
  - AD:buffer:util_rfifo:1.0.0
  - AD:buffer:util_wfifo:1.0.0
  - AD:common:util_clkdiv:1.0.0
  - AD:common:ad_rst:1.0.0
  - AFRL:utility:tcl_helper_check:1.0.0
  - zipcpu:axi_lite:crossbar:1.0.0

2 Architecture

The project contains four wrappers

- **system_wrapper** Contains the top level project module and contains system_pl_wrapper and system_ps_wrapper.
- **system_pl_wrapper** Contains the AD9361 wrapper and any support IP's in the program logic.
- **ad9361_pl_wrapper** Contains all program logic IP's dealing with the AD9361.
- **system_ps_wrapper** Contains the processor system IP wrappers.

Please see 5 for more information per target.

3 Building

The all fmcomms2-3 core is written in Verilog 2001. They should synthesize in any modern FPGA software. The core comes as a fusesoc packaged core and can be included in any other core. Be sure to make sure you have meet the dependencies listed in the previous section.

3.1 fusesoc

Fusesoc is a system for building FPGA software without relying on the internal project management of the tool. Avoiding vendor lock in to Vivado or Quartus. These cores, when included in a project, can be easily integrated and targets created based upon the end developer needs. The core by itself is not a part of a system and should be integrated into a fusesoc based system. Simulations are setup to use fusesoc and are a part of its targets.

3.2 Source Files

3.2.1 fusesoc_info File List

- src_ad9361_pl
  - 'common/ad9361_pl_wrapper.v': 'file_type': 'verilogSource'
- zed
  - 'zed/system_constr.xdc': 'file_type': 'xdc'

  - ’zed/system_wrapper.v’: ’file_type’: ’verilogSource’
  - ’zed/system_pl_wrapper.v’: ’file_type’: ’verilogSource’
  - ’zed/system_pl_gen.tcl’: ’file_type’: ’tclSource’
  - ’zed/system_gen.tcl’: ’file_type’: ’tclSource’

- zc706
  - ’zc706/system_constr.xdc’: ’file_type’: ’xdc’
  - ’zc706/system_wrapper.v’: ’file_type’: ’verilogSource’
  - ’zc706/system_pl_wrapper.v’: ’file_type’: ’verilogSource’
  - ’zc706/system_pl_gen.tcl’: ’file_type’: ’tclSource’
  - ’zc706/system_gen.tcl’: ’file_type’: ’tclSource’
- zc702
  - ’zc702/system_constr.xdc’: ’file_type’: ’xdc’
  - ’zc702/system_wrapper.v’: ’file_type’: ’verilogSource’
  - ’zc702/system_pl_wrapper.v’: ’file_type’: ’verilogSource’
  - ’zc702/system_pl_gen.tcl’: ’file_type’: ’tclSource’
  - ’zc702/system_gen.tcl’: ’file_type’: ’tclSource’
- zcu102
  - ’zcu102/system_constr.xdc’: ’file_type’: ’xdc’
  - ’zcu102/system_wrapper.v’: ’file_type’: ’verilogSource’
  - ’zcu102/system_pl_wrapper.v’: ’file_type’: ’verilogSource’
  - ’zcu102/system_pl_gen.tcl’: ’file_type’: ’tclSource’
  - ’zcu102/system_gen.tcl’: ’file_type’: ’tclSource’
- hanpilot
  - ’hanpilot/system_constr.sdc’: ’file_type’: ’SDC’
  - ’hanpilot/system_wrapper.v’: ’file_type’: ’verilogSource’
  - ’hanpilot/system_pl_wrapper.v’: ’file_type’: ’verilogSource’
  - ’hanpilot/system_pl_gen.tcl’: ’file_type’: ’tclSource’
  - ’hanpilot/system_gen.tcl’: ’file_type’: ’tclSource’
- a10soc
  - ’a10soc/system_constr.sdc’: ’file_type’: ’SDC’
  - ’a10soc/system_wrapper.v’: ’file_type’: ’verilogSource’
  - ’a10soc/system_pl_wrapper.v’: ’file_type’: ’verilogSource’
  - ’a10soc/system_pl_gen.tcl’: ’file_type’: ’tclSource’
  - ’a10soc/system_gen.tcl’: ’file_type’: ’tclSource’

3.3 Targets

3.3.1 fusesoc_info Targets

- default

  Info: Default target, do not use.

- zed

  Info: zedboard target.

- zed_bootgen

  Info: zed build with boot.bin output in BOOTFS folder.

- zc706

  Info: zc706 target.

- zc706_bootgen

  Info: zc706 build with boot.bin output in BOOTFS folder.

- zc702

  Info: zc702 target.

- zc702_bootgen

  Info: zc702 build with boot.bin output in BOOTFS folder.

- zcu102

  Info: zcu102 target.

- zcu102_bootgen

  Info: zcu102 build with boot.bin output in BOOTFS folder.

- hanpilot

  Info: hanpilot target.

- hanpilot_bootgen

  Info: hanpilot build with BOOTFS file generation.

- a10soc

  Info: a10soc target.

- a10soc_bootgen

  Info: arria10 build with BOOTFS file generation.

3.4 Directory Guide

Below highlights important folders from the root of the directory.

1. **docs** Contains all documentation related to this project.
    - **manual** Contains user manual and github page that are generated from the latex sources.
2. **a10soc** Contains source files for Arria 10 soc
3. **common** Contains source file wrapper for ad9361 core
4. **hanpilot** Contains source files for Arria based hanpilot
5. **zc702** Contains source files for Xilinx zc702
6. **zc706** Contains source files for Xilinx zc706
7. **zcu102** Contains source files for Xilinx zcu102
8. **zed** Contains source files for Digilent Zedboard

4 Simulation

There is no simulation at the moment. This is dues to the AD9361 and ARM subsystems. Maybe a future addition with Vexriscv?

5 Module Documentation

There project has multiple modules. The targets are the top system wrappers.

- **ad9361 system pl**
- **hanpilot system pl**
- **hanpilot system**
- **zc702 system pl**
- **zc702 system**
- **zc706 system pl**
- **zc706 system**
- **zcu102 system pl**
- **zcu102 system**
- **zed system pl**
- **zed system**
- **a10soc system pl**
- **a10soc system**

The next sections document the module in great detail.

ad9361_pl_wrapper.v

AUTHORS

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DATES

2023/11/02

INFORMATION

Brief

AD9361 core and support core wrapper.

License MIT

ad9361_pl_wrapper

```
module ad9361_pl_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
0,
parameter
FPGA_FAMILY
 =
0,
parameter
SPEED_GRADE
```

```
 =
0,
parameter
DEV_PACKAGE
 =
0,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0,
parameter
DELAY_REFCLK_FREQUENCY
 =
200,
parameter
DMA_AXI_PROTOCOL_TO_PS
 =
1,
parameter
AXI_DMAC_ADC_ADDR
 =
32'h7C400000,
parameter
AXI_DMAC_DAC_ADDR
 =
32'h7C420000,
parameter
AXI_AD9361_ADDR
 =
32'h79020000
) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_a
```

AD9361 core and support core wrapper.

Parameters

FPGA_TECHNOLOGY
parameter
Type of FPGA, such as Ultrascale, Arria 10. 1 is for 7 series.

FPGA_FAMILY
parameter
Sub type of fpga, such as GX, SX, etc. 4 is for zynq.

SPEED_GRADE
parameter
Number that corresponds to the ships recommeneded speed. 20 is for -2.

DEV_PACKAGE
parameter
Specify a number that is equal to the manufactures package. 3 is for ff.

DELAY_REFCLK_FREQUENCY
parameter
Reference clock frequency used for ad_data_in instances

ADC_INIT_DELAY
parameter
Initial Delay for the ADC

DAC_INIT_DELAY
parameter
Initial Delay for the DAC

Ports

axi_aclk AXI Lite control bus

axi_aresetn AXI Lite control bus

s_axi_awvalid AXI Lite control bus

s_axi_awaddr	AXI Lite control bus
s_axi_awready	AXI Lite control bus
s_axi_awprot	AXI Lite control bus
s_axi_wvalid	AXI Lite control bus
s_axi_wdata	AXI Lite control bus
s_axi_wstrb	AXI Lite control bus
s_axi_wready	AXI Lite control bus
s_axi_bvalid	AXI Lite control bus
s_axi_bresp	AXI Lite control bus
s_axi_bready	AXI Lite control bus
s_axi_arvalid	AXI Lite control bus
s_axi_araddr	AXI Lite control bus
s_axi_arready	AXI Lite control bus
s_axi_arprot	AXI Lite control bus
s_axi_rvalid	AXI Lite control bus
s_axi_rready	AXI Lite control bus
s_axi_rresp	AXI Lite control bus
s_axi_rdata	AXI Lite control bus
adc_dma_irq	fmcomms2-3 ADC irq
dac_dma_irq	fmcomms2-3 DAC irq
delay_clk	fmcomms2-3 delay clock
rx_clk_in_p	fmcomms2-3 receive clock in
rx_clk_in_n	fmcomms2-3 receive clock in
rx_frame_in_p	fmcomms2-3 receive frame
rx_frame_in_n	fmcomms2-3 receive frame
rx_data_in_p	fmcomms2-3 receive lvds data
rx_data_in_n	fmcomms2-3 receive lvds data
tx_clk_out_p	fmcomms2-3 transmit clock
tx_clk_out_n	fmcomms2-3 transmit clock
tx_frame_out_p	fmcomms2-3 transmit frame
tx_frame_out_n	fmcomms2-3 transmit frame
tx_data_out_p	fmcomms2-3 transmit lvds data
tx_data_out_n	fmcomms2-3 transmit lvds data
enable	fmcomms2-3 enable
txnrx	fmcomms2-3 txnrx select
up_enable	fmcomms2-3 enable input
up_txnrx	fmcomms2-3 txnrx select input
tdd_sync_t	fmcomms2-3 TDD sync i/o
tdd_sync_i	fmcomms2-3 TDD sync i/o
tdd_sync_o	fmcomms2-3 TDD sync i/o
adc_m_dest_axi_awaddr	fmcomms2-3 ADC DMA

adc_m_dest_axi_awlen	fmcomms2-3 ADC DMA
adc_m_dest_axi_awsize	fmcomms2-3 ADC DMA
adc_m_dest_axi_awburst	fmcomms2-3 ADC DMA
adc_m_dest_axi_awprot	fmcomms2-3 ADC DMA
adc_m_dest_axi_awcache	fmcomms2-3 ADC DMA
adc_m_dest_axi_awvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_awready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wdata	fmcomms2-3 ADC DMA
adc_m_dest_axi_wstrb	fmcomms2-3 ADC DMA
adc_m_dest_axi_wready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_wlast	fmcomms2-3 ADC DMA
adc_m_dest_axi_bvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_bresp	fmcomms2-3 ADC DMA
adc_m_dest_axi_bready	fmcomms2-3 ADC DMA
dac_m_src_axi_arready	fmcomms2-3 DAC DMA
dac_m_src_axi_arvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_araddr	fmcomms2-3 DAC DMA
dac_m_src_axi_arlen	fmcomms2-3 DAC DMA
dac_m_src_axi_arsize	fmcomms2-3 DAC DMA
dac_m_src_axi_arburst	fmcomms2-3 DAC DMA
dac_m_src_axi_arprot	fmcomms2-3 DAC DMA
dac_m_src_axi_arcache	fmcomms2-3 DAC DMA
dac_m_src_axi_rdata	fmcomms2-3 DAC DMA
dac_m_src_axi_rready	fmcomms2-3 DAC DMA
dac_m_src_axi_rvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_rresp	fmcomms2-3 DAC DMA
dac_m_src_axi_rlast	fmcomms2-3 DAC DMA

INSTANTIANTED MODULES

inst_axi_ad9361

```
axi_ad9361 #(

ID(0),

MODE_1R1T(0),

FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),

FPGA_FAMILY(FPGA_FAMILY),

SPEED_GRADE(SPEED_GRADE),
DEV_PACKAGE(DEV_PACKAGE),

TDD_DISABLE(1),

PPS_RECEIVER_ENABLE(0),

CMOS_OR_LVDS_N(0),

ADC_INIT_DELAY(ADC_INIT_DELAY),

ADC_DATAPATH_DISABLE(0),

ADC_USERPORTS_DISABLE(0),

ADC_DATAFORMAT_DISABLE(0),

ADC_DCFILTER_DISABLE(0),

ADC_IQCORRECTION_DISABLE(0),

DAC_INIT_DELAY(DAC_INIT_DELAY),

DAC_CLK_EDGE_SEL(0),

DAC_IODELAY_ENABLE(0),

DAC_DATAPATH_DISABLE(0),

DAC_DDS_DISABLE(0),

DAC_DDS_TYPE(1),

DAC_DDS_CORDIC_DW(14),

DAC_DDS_CORDIC_PHASE_DW(13),

DAC_USERPORTS_DISABLE(0),

DAC_IQCORRECTION_DISABLE(0),

IO_DELAY_GROUP("dev_if_delay_group"),

MIMO_ENABLE(0),

USE_SSI_CLK(1),

DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY),

RX_NODPA(0)
) inst_axi_ad9361 ( .rx_clk_in_p(rx_clk_in_p), .rx_clk_in_n(rx_clk_in_n), .r
```

Analog Devices ad9361 interface core

inst_adc_axi_dmac

```
axi_dmac #(

ID(0),

DMA_DATA_WIDTH_SRC(64),

DMA_DATA_WIDTH_DEST(64),
DMA_LENGTH_WIDTH(24),
DMA_2D_TRANSFER(0),
ASYNC_CLK_REQ_SRC(1),
ASYNC_CLK_SRC_DEST(1),
ASYNC_CLK_DEST_REQ(0),
AXI_SLICE_DEST(0),
AXI_SLICE_SRC(0),
SYNC_TRANSFER_START(1),
CYCLIC(0),
DMA_AXI_PROTOCOL_DEST(DMA_AXI_PROTOCOL_TO_PS),
DMA_AXI_PROTOCOL_SRC(1),
DMA_TYPE_DEST(0),
DMA_TYPE_SRC(1),
DMA_AXI_ADDR_WIDTH(32),
MAX_BYTES_PER_BURST(128),
FIFO_SIZE(8),
AXI_ID_WIDTH_SRC(6),
AXI_ID_WIDTH_DEST(6),
DMA_AXIS_ID_W(8),
DMA_AXIS_DEST_W(4),
DISABLE_DEBUG_REGISTERS(0),
ENABLE_DIAGNOSTICS_IF(0),
ALLOW_ASYM_MEM(1)
) inst_adc_axi_dmac ( .s_axi_aclk(axi_aclk), .s_axi_aresetn(axi_aresetn), .s
```

Analog Devices DMA for AD9361 ADC

inst_dac_axi_dmac

```
axi_dmac #(
ID(0),
DMA_DATA_WIDTH_SRC(64),
DMA_DATA_WIDTH_DEST(64),
DMA_LENGTH_WIDTH(24),
DMA_2D_TRANSFER(0),
 ASYNC_CLK_REQ_SRC(0),
                                                                             .
 ASYNC_CLK_SRC_DEST(1),
                                                                             .
 ASYNC_CLK_DEST_REQ(1),
                                                                             .
 AXI_SLICE_DEST(0),
                                                                             .
 AXI_SLICE_SRC(0),
                                                                             .
 SYNC_TRANSFER_START(0),
                                                                             .
 CYCLIC(1),
                                                                             .
 DMA_AXI_PROTOCOL_DEST(1),
                                                                             .
 DMA_AXI_PROTOCOL_SRC(DMA_AXI_PROTOCOL_TO_PS),
                                                                             .
 DMA_TYPE_DEST(1),
                                                                             .
 DMA_TYPE_SRC(0),
                                                                             .
 DMA_AXI_ADDR_WIDTH(32),
                                                                             .
 MAX_BYTES_PER_BURST(128),
                                                                             .
 FIFO_SIZE(8),
                                                                             .
 AXI_ID_WIDTH_SRC(6),
                                                                             .
 AXI_ID_WIDTH_DEST(6),
                                                                             .
 DMA_AXIS_ID_W(8),
                                                                             .
 DMA_AXIS_DEST_W(4),
                                                                             .
 DISABLE_DEBUG_REGISTERS(0),
                                                                             .
 ENABLE_DIAGNOSTICS_IF(0),
                                                                             .
 ALLOW_ASYM_MEM(1)
) inst_dac_axi_dmac ( .s_axi_aclk(axi_aclk), .s_axi_aresetn(axi_aresetn), .s
```

Analog Devices DMA for AD9361 DAC

inst_adc_cpack

```
 util_cpack2_axis #(
                                                                             .
 NUM_OF_CHANNELS(4),
                                                                             .
 SAMPLES_PER_CHANNEL(1),
                                                                             .
 SAMPLE_DATA_WIDTH(16)
) inst_adc_cpack ( .clk(d_clk), .reset(p_reset), .enable_0(fifo_adc_enable_
```

Analog Devices Utility to take ad9361 data and pack it to a AXIS bus for the ADC

inst_dac_cpack

Analog Devices Utility to take ad9361 data and unpack from the AXIS bus to the DAC

inst_dac_fifo

```
util_rfifo #(
                                                                        .
NUM_OF_CHANNELS(4),
                                                                        .
DIN_DATA_WIDTH(16),
                                                                        .
DOUT_DATA_WIDTH(16),
                                                                        .
DIN_ADDRESS_WIDTH(4)
) inst_dac_fifo ( .din_rstn(p_aresetn), .din_clk(d_clk), .din_enable_0(fif
```

Analog Devices FIFO for AD9361 DAC BUS

inst_adc_fifo

```
util_wfifo #(
                                                                        .
NUM_OF_CHANNELS(4),
                                                                        .
DIN_DATA_WIDTH(16),
                                                                        .
DOUT_DATA_WIDTH(16),
                                                                        .
DIN_ADDRESS_WIDTH(4)
) inst_adc_fifo ( .din_rst(ad_reset_o), .din_clk(l_clk), .din_enable_0(adc_
```

Analog Devices FIFO for AD9361 ADC BUS

inst_clkdiv

```
util_clkdiv #(
                                                                        .
SIM_DEVICE(SIM_DEVICE)
) inst_clkdiv ( .clk(l_clk), .clk_sel(adc_r1_mode & dac_r1_mode), .clk_out
```

Analog Devices Clock Divider with select

isnt_util_tdd_sync

```
util_tdd_sync #(
                                                                        .
TDD_SYNC_PERIOD(100000000)
) isnt_util_tdd_sync ( .clk(axi_aclk), .rstn(axi_aresetn), .sync_mode(tdd_
```

Analog Devices tdd sync utility

inst_ad_reset

```
 ad_rst inst_ad_reset (
                                                                          .
 rst_async(~axi_aresetn),
                                                                          .
 clk(d_clk),
                                                                          .
 rstn(p_aresetn),
                                                                          .
 rst(p_reset)
)
```

Analog Devices reset sync

inst_axilxbar

```
 axilxbar #(
                                                                          .
 C_AXI_DATA_WIDTH(32),
                                                                          .
 C_AXI_ADDR_WIDTH(32),
                                                                          .
 NM(1),
                                                                          .
 NS(3),
                                                                          .
 SLAVE_ADDR({{AXI_DMAC_ADC_ADDR},{AXI_DMAC_DAC_ADDR},{AXI_AD9361_ADDR}}),
                                                                          .
 SLAVE_MASK({{32'hFFFFF000},{32'hFFFFF000},{32'hFFFF0000}})
) inst_axilxbar ( .S_AXI_ACLK(axi_aclk), .S_AXI_ARESETN(axi_aresetn), .S_AXI
```

AXI Lite crossbar for ADC DMA, DAC DMA, and AD9361 control registers.

system_pl_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl only for hanpilot board.

License MIT

system_pl_wrapper

```
module system_pl_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
0,
parameter
FPGA_FAMILY
 =
0,
parameter
SPEED_GRADE
```

```
 =
0,
parameter
DEV_PACKAGE
 =
0,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0,
parameter
DELAY_REFCLK_FREQUENCY
 =
200
) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_
```

System wrapper for pl only for hanpilot board.

Parameters

FPGA_TECHNOLOGY
parameter
Type of FPGA, such as Ultrascale, Arria 10. 103 is for Arria 10.

FPGA_FAMILY
parameter
Sub type of fpga, such as GX, SX, etc. 1 is for SX

SPEED_GRADE
parameter
Number that corresponds to the ships recommeneded speed. 2 is for 2.

DEV_PACKAGE
parameter
Specify a number that is equal to the manufactures package. 3 is for FBGA.

ADC_INIT_DELAY
parameter
Initial Delay for the ADC

DAC_INIT_DELAY
parameter
Initial Delay for the DAC

DELAY_REFCLK_FREQUENCY
parameter
Reference clock frequency used for ad_data_in instances

Ports

axi_aclk	AXI Lite control bus
axi_aresetn	AXI Lite control bus
s_axi_awvalid	AXI Lite control bus
s_axi_awaddr	AXI Lite control bus
s_axi_awready	AXI Lite control bus
s_axi_awprot	AXI Lite control bus
s_axi_wvalid	AXI Lite control bus
s_axi_wdata	AXI Lite control bus
s_axi_wstrb	AXI Lite control bus
s_axi_wready	AXI Lite control bus
s_axi_bvalid	AXI Lite control bus
s_axi_bresp	AXI Lite control bus
s_axi_bready	AXI Lite control bus

s_axi_arvalid	AXI Lite control bus
s_axi_araddr	AXI Lite control bus
s_axi_arready	AXI Lite control bus
s_axi_arprot	AXI Lite control bus
s_axi_rvalid	AXI Lite control bus
s_axi_rready	AXI Lite control bus
s_axi_rresp	AXI Lite control bus
s_axi_rdata	AXI Lite control bus
adc_dma_irq	fmcomms2-3 ADC irq
dac_dma_irq	fmcomms2-3 DAC irq
delay_clk	fmcomms2-3 delay clock
rx_clk_in_p	fmcomms2-3 receive clock in
rx_clk_in_n	fmcomms2-3 receive clock in
rx_frame_in_p	fmcomms2-3 receive frame
rx_frame_in_n	fmcomms2-3 receive frame
rx_data_in_p	fmcomms2-3 receive lvds data
rx_data_in_n	fmcomms2-3 receive lvds data
tx_clk_out_p	fmcomms2-3 transmit clock
tx_clk_out_n	fmcomms2-3 transmit clock
tx_frame_out_p	fmcomms2-3 transmit frame
tx_frame_out_n	fmcomms2-3 transmit frame
tx_data_out_p	fmcomms2-3 transmit lvds data
tx_data_out_n	fmcomms2-3 transmit lvds data
enable	fmcomms2-3 enable
txnrx	fmcomms2-3 txnrx select
up_enable	fmcomms2-3 enable input
up_txnrx	fmcomms2-3 txnrx select input
tdd_sync_t	fmcomms2-3 TDD sync i/o
tdd_sync_i	fmcomms2-3 TDD sync i/o
tdd_sync_o	fmcomms2-3 TDD sync i/o
adc_m_dest_axi_awaddr	fmcomms2-3 ADC DMA
adc_m_dest_axi_awlen	fmcomms2-3 ADC DMA
adc_m_dest_axi_awsize	fmcomms2-3 ADC DMA
adc_m_dest_axi_awburst	fmcomms2-3 ADC DMA
adc_m_dest_axi_awprot	fmcomms2-3 ADC DMA
adc_m_dest_axi_awcache	fmcomms2-3 ADC DMA
adc_m_dest_axi_awvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_awready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wdata	fmcomms2-3 ADC DMA
adc_m_dest_axi_wstrb	fmcomms2-3 ADC DMA
adc_m_dest_axi_wready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wvalid	fmcomms2-3 ADC DMA

adc_m_dest_axi_wlast	fmcomms2-3 ADC DMA
adc_m_dest_axi_bvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_bresp	fmcomms2-3 ADC DMA
adc_m_dest_axi_bready	fmcomms2-3 ADC DMA
dac_m_src_axi_arready	fmcomms2-3 DAC DMA
dac_m_src_axi_arvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_araddr	fmcomms2-3 DAC DMA
dac_m_src_axi_arlen	fmcomms2-3 DAC DMA
dac_m_src_axi_arsize	fmcomms2-3 DAC DMA
dac_m_src_axi_arburst	fmcomms2-3 DAC DMA
dac_m_src_axi_arprot	fmcomms2-3 DAC DMA
dac_m_src_axi_arcache	fmcomms2-3 DAC DMA
dac_m_src_axi_rdata	fmcomms2-3 DAC DMA
dac_m_src_axi_rready	fmcomms2-3 DAC DMA
dac_m_src_axi_rvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_rresp	fmcomms2-3 DAC DMA
dac_m_src_axi_rlast	fmcomms2-3 DAC DMA

INSTANTIANTED MODULES

inst_ad9361_pl_wrapper

```
 ad9361_pl_wrapper #(
                                                                          .
 FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                          .
 FPGA_FAMILY(FPGA_FAMILY),
                                                                          .
 SPEED_GRADE(SPEED_GRADE),
                                                                          .
 DEV_PACKAGE(DEV_PACKAGE),
                                                                          .
 ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                          .
 DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                          .
 DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY),
                                                                          .
 AXI_DMAC_ADC_ADDR(32'h00010000),
                                                                          .
 AXI_DMAC_DAC_ADDR(32'h00014000),
                                                                          .
 AXI_AD9361_ADDR(32'h00000000)
) inst_ad9361_pl_wrapper ( .axi_aclk(axi_aclk), .axi_aresetn(axi_aresetn),
```

Module instance of ad9361_pl_wrapper for the fmcomms2-3 device.

system_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl and ps for hanpilot board.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
103,
parameter
FPGA_FAMILY
 =
1,
parameter
SPEED_GRADE
```

```
 =
2,
parameter
DEV_PACKAGE
 =
3,
parameter
DELAY_REFCLK_FREQUENCY
 =
200,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0
) ( input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hp
```

System wrapper for pl and ps for hanpilot board.

Parameters

FPGA_TECHNOLOGY
parameter
Type of FPGA, such as Ultrascale, Arria 10. 103 is for Arria 10.

FPGA_FAMILY
parameter
Sub type of fpga, such as GX, SX, etc. 1 is for SX

SPEED_GRADE
parameter
Number that corresponds to the ships recommeneded speed. 2 is for 2.

DEV_PACKAGE
parameter
Specify a number that is equal to the manufactures package. 3 is for FBGA.

DELAY_REFCLK_FREQUENCY
parameter
Reference clock frequency used for ad_data_in instances

ADC_INIT_DELAY
parameter
Initial Delay for the ADC

DAC_INIT_DELAY
parameter
Initial Delay for the DAC

Ports

sys_clk	Input clock for all clocks
sys_resetn	Input reset for all resets
hps_ddr_ref_clk	DDR port
hps_ddr_clk_p	DDR port
hps_ddr_clk_n	DDR port
hps_ddr_a	DDR port
hps_ddr_ba	DDR port
hps_ddr_bg	DDR port
hps_ddr_cke	DDR port
hps_ddr_cs_n	DDR port
hps_ddr_odt	DDR port
hps_ddr_reset_n	DDR port
hps_ddr_act_n	DDR port

hps_ddr_par	DDR port
hps_ddr_alert_n	DDR port
hps_ddr_dqs_p	DDR port
hps_ddr_dqs_n	DDR port
hps_ddr_dq	DDR port
hps_ddr_dbi_n	DDR port
hps_ddr_rzq	DDR port
hps_eth_rxclk	Ethernet Device
hps_eth_rxctl	Ethernet Device
hps_eth_rxd	Ethernet Device
hps_eth_txclk	Ethernet Device
hps_eth_txctl	Ethernet Device
hps_eth_txd	Ethernet Device
hps_eth_mdc	Ethernet Device
hps_eth_mdio	Ethernet Device
hps_sdio_clk	SD card interface
hps_sdio_cmd	SD card interface
hps_sdio_d	SD card interface
hps_usb_clk	USB interface
hps_usb_dir	USB interface
hps_usb_nxt	USB interface
hps_usb_stp	USB interface
hps_usb_d	USB interface
hps_uart_rx	UART interface
hps_uart_tx	UART interface
hps_i2c_sda	i2c interface
hps_i2c_scl	i2c interface
hps_gpio	GPIO interface
hps_led	LED output, heartbeat
hps_key	Used for reset
gpio_bd_i	fmcomms2-3 gpio
gpio_bd_o	fmcomms2-3 gpio
fmc_i2c_sda	fmcomms2-3 i2c
fmc_i2c_scl	fmcomms2-3 i2c
rx_clk_in	fmcomms2-3 receive clock in
rx_frame_in_p	fmcomms2-3 receive frame
rx_frame_in_n	fmcomms2-3 receive frame
rx_data_in_p	fmcomms2-3 receive lvds data
rx_data_in_n	fmcomms2-3 receive lvds data
tx_clk_out_p	fmcomms2-3 transmit clock
tx_clk_out_n	fmcomms2-3 transmit clock
tx_frame_out_p	fmcomms2-3 transmit frame

tx_frame_out_n	fmcomms2-3 transmit frame
tx_data_out_p	fmcomms2-3 transmit lvds data
tx_data_out_n	fmcomms2-3 transmit lvds data
enable	fmcomms2-3 enable
txnrx	fmcomms2-3 txnrx select
gpio_resetb	fmcomms2-3 gpio reset
gpio_sync	fmcomms2-3 gpio sync
gpio_en_agc	fmcomms2-3 gpio enable agc
gpio_ctl	fmcomms2-3 control
gpio_status	fmcomms2-3 status
spi_csn	fmcomms2-3 spi select
spi_clk	fmcomms2-3 spi clk
spi_mosi	fmcomms2-3 spi output
spi_miso	fmcomms2-3 spi input

INSTANTIANTED MODULES

inst_system_pl_wrapper

```
system_pl_wrapper #(
                                                                        .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                        .
FPGA_FAMILY(FPGA_FAMILY),
                                                                        .
SPEED_GRADE(SPEED_GRADE),
                                                                        .
DEV_PACKAGE(DEV_PACKAGE),
                                                                        .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                        .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                        .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_system_pl_wrapper ( .axi_aclk(s_axi_clk), .axi_aresetn(s_axi_aresetn
```

Module instance of system_pl_wrapper for the fmcomms2-3 device.

inst_system_ps_wrapper

```
system_ps_wrapper inst_system_ps_wrapper (
                                                                        .
s_axi_clk_clk(s_axi_clk),
                                                                        .
s_axi_aresetn_reset_n(s_axi_aresetn),
                                                                        .
m_axi_awaddr(w_axi_awaddr),
                                                                        .
m_axi_awprot(w_axi_awprot),
                                                                        .
m_axi_awvalid(w_axi_awvalid),
m_axi_awready(w_axi_awready),
m_axi_wdata(w_axi_wdata),
m_axi_wstrb(w_axi_wstrb),
m_axi_wvalid(w_axi_wvalid),
m_axi_wready(w_axi_wready),
m_axi_bresp(w_axi_bresp),
m_axi_bvalid(w_axi_bvalid),
m_axi_bready(w_axi_bready),
m_axi_araddr(w_axi_araddr),
m_axi_arprot(w_axi_arprot),
m_axi_arvalid(w_axi_arvalid),
m_axi_arready(w_axi_arready),
m_axi_rdata(w_axi_rdata),
m_axi_rresp(w_axi_rresp),
m_axi_rvalid(w_axi_rvalid),
m_axi_rready(w_axi_rready),
sys_delay_clk_clk(s_delay_clk),
sys_clk_clk(sys_clk),
sys_gpio_bd_in_port(gpio_i[31:0]),
sys_gpio_bd_out_port(gpio_o[31:0]),
sys_gpio_in_export(gpio_i[63:32]),
sys_gpio_out_export(gpio_o[63:32]),
sys_hps_rstn_reset_n
sys_resetn),
sys_rstn_reset_n
sys_resetn_s),
sys_hps_io_hps_io_phery_emac0_TX_CLK
hps_eth_txclk),
sys_hps_io_hps_io_phery_emac0_TXD0
hps_eth_txd[0]),
sys_hps_io_hps_io_phery_emac0_TXD1
hps_eth_txd[1]),
sys_hps_io_hps_io_phery_emac0_TXD2
```

```
                                                                          (
hps_eth_txd[2]),
                                                                          .
sys_hps_io_hps_io_phery_emac0_TXD3
                                                                          (
hps_eth_txd[3]),
                                                                          .
sys_hps_io_hps_io_phery_emac0_RX_CTL
                                                                          (
hps_eth_rxctl),
                                                                          .
sys_hps_io_hps_io_phery_emac0_TX_CTL
                                                                          (
hps_eth_txctl),
                                                                          .
sys_hps_io_hps_io_phery_emac0_RX_CLK
                                                                          (
hps_eth_rxclk),
                                                                          .
sys_hps_io_hps_io_phery_emac0_RXD0
                                                                          (
hps_eth_rxd[0]),
                                                                          .
sys_hps_io_hps_io_phery_emac0_RXD1
                                                                          (
hps_eth_rxd[1]),
                                                                          .
sys_hps_io_hps_io_phery_emac0_RXD2
                                                                          (
hps_eth_rxd[2]),
                                                                          .
sys_hps_io_hps_io_phery_emac0_RXD3
                                                                          (
hps_eth_rxd[3]),
                                                                          .
sys_hps_io_hps_io_phery_emac0_MDIO
                                                                          (
hps_eth_mdio),
                                                                          .
sys_hps_io_hps_io_phery_emac0_MDC
                                                                          (
hps_eth_mdc),
                                                                          .
sys_hps_io_hps_io_phery_sdmmc_CMD
                                                                          (
hps_sdio_cmd),
                                                                          .
sys_hps_io_hps_io_phery_sdmmc_D0
                                                                          (
hps_sdio_d[0]),
                                                                          .
sys_hps_io_hps_io_phery_sdmmc_D1
                                                                          (
hps_sdio_d[1]),
                                                                          .
sys_hps_io_hps_io_phery_sdmmc_D2
                                                                          (
hps_sdio_d[2]),
                                                                          .
sys_hps_io_hps_io_phery_sdmmc_D3
                                                                          (
hps_sdio_d[3]),
                                                                          .
sys_hps_io_hps_io_phery_sdmmc_CCLK
                                                                          (
hps_sdio_clk),
                                                                        .
sys_hps_io_hps_io_phery_usb0_DATA0
                                                                        (
hps_usb_d[0]),
                                                                        .
sys_hps_io_hps_io_phery_usb0_DATA1
                                                                        (
hps_usb_d[1]),
                                                                        .
sys_hps_io_hps_io_phery_usb0_DATA2
                                                                        (
hps_usb_d[2]),
                                                                        .
sys_hps_io_hps_io_phery_usb0_DATA3
                                                                        (
hps_usb_d[3]),
                                                                        .
sys_hps_io_hps_io_phery_usb0_DATA4
                                                                        (
hps_usb_d[4]),
                                                                        .
sys_hps_io_hps_io_phery_usb0_DATA5
                                                                        (
hps_usb_d[5]),
                                                                        .
sys_hps_io_hps_io_phery_usb0_DATA6
                                                                        (
hps_usb_d[6]),
                                                                        .
sys_hps_io_hps_io_phery_usb0_DATA7
                                                                        (
hps_usb_d[7]),
                                                                        .
sys_hps_io_hps_io_phery_usb0_CLK
                                                                        (
hps_usb_clk),
                                                                        .
sys_hps_io_hps_io_phery_usb0_STP
                                                                        (
hps_usb_stp),
                                                                        .
sys_hps_io_hps_io_phery_usb0_DIR
                                                                        (
hps_usb_dir),
                                                                        .
sys_hps_io_hps_io_phery_usb0_NXT
                                                                        (
hps_usb_nxt),
                                                                        .
sys_hps_io_hps_io_phery_uart1_RX
                                                                        (
hps_uart_rx),
                                                                        .
sys_hps_io_hps_io_phery_uart1_TX
                                                                        (
hps_uart_tx),
                                                                        .
sys_hps_io_hps_io_phery_i2c0_SDA
                                                                        (
hps_i2c_sda),
                                                                        .
sys_hps_io_hps_io_phery_i2c0_SCL
                                                                        (
hps_i2c_scl),
                                                                        .
sys_hps_io_hps_io_gpio_gpio1_io1
```

```
                                                                        (
hps_led),
                                                                        .
sys_hps_io_hps_io_gpio_gpio1_io4
                                                                        (
hps_key),
                                                                        .
sys_hps_io_hps_io_gpio_gpio1_io15(mpu_int),
                                                                        .
sys_hps_io_hps_io_gpio_gpio2_io8
                                                                        (
hps_gpio[0]),
                                                                        .
sys_hps_io_hps_io_gpio_gpio2_io9
                                                                        (
hps_gpio[1]),
                                                                        .
sys_hps_io_hps_io_gpio_gpio2_io10
                                                                        (
hps_gpio[2]),
                                                                        .
sys_hps_io_hps_io_gpio_gpio2_io11
                                                                        (
hps_gpio[3]),
                                                                        .
sys_hps_out_rstn_reset_n
                                                                        (
sys_hps_resetn),
                                                                        .
sys_hps_fpga_irq1_irq
                                                                       ({
32{1'b0}}),
                                                                        .
sys_hps_dma_data_awid(0),
                                                                        .
sys_hps_dma_data_awaddr(adc_hp0_axi_awaddr),
                                                                        .
sys_hps_dma_data_awlen(adc_hp0_axi_awlen),
                                                                        .
sys_hps_dma_data_awsize(adc_hp0_axi_awsize),
                                                                        .
sys_hps_dma_data_awburst(adc_hp0_axi_awburst),
                                                                        .
sys_hps_dma_data_awlock(0),
                                                                        .
sys_hps_dma_data_awcache(adc_hp0_axi_awcache),
                                                                        .
sys_hps_dma_data_awprot(adc_hp0_axi_awprot),
                                                                        .
sys_hps_dma_data_awvalid(adc_hp0_axi_awvalid),
                                                                        .
sys_hps_dma_data_awready(adc_hp0_axi_awready),
                                                                        .
sys_hps_dma_data_awuser(0),
                                                                        .
sys_hps_dma_data_wid(0),
                                                                        .
sys_hps_dma_data_wdata(adc_hp0_axi_wdata),
                                                                        .
sys_hps_dma_data_wstrb(adc_hp0_axi_wstrb),
                                                                        .
sys_hps_dma_data_wlast(adc_hp0_axi_wlast),
                                                                        .
sys_hps_dma_data_wvalid(adc_hp0_axi_wvalid),
                                                                        .
sys_hps_dma_data_wready(adc_hp0_axi_wready),
sys_hps_dma_data_bid(),
sys_hps_dma_data_bresp(adc_hp0_axi_bresp),
sys_hps_dma_data_bvalid(adc_hp0_axi_bvalid),
sys_hps_dma_data_bready(adc_hp0_axi_bready),
sys_hps_dma_data_arid(0),
sys_hps_dma_data_araddr(dac_hp1_axi_araddr),
sys_hps_dma_data_arlen(dac_hp1_axi_arlen),
sys_hps_dma_data_arsize(dac_hp1_axi_arsize),
sys_hps_dma_data_arburst(dac_hp1_axi_arburst),
sys_hps_dma_data_arlock(0),
sys_hps_dma_data_arcache(dac_hp1_axi_arcache),
sys_hps_dma_data_arprot(dac_hp1_axi_arprot),
sys_hps_dma_data_arvalid(dac_hp1_axi_arvalid),
sys_hps_dma_data_arready(dac_hp1_axi_arready),
sys_hps_dma_data_aruser(0),
sys_hps_dma_data_rid(),
sys_hps_dma_data_rdata(dac_hp1_axi_rdata),
sys_hps_dma_data_rresp(dac_hp1_axi_rresp),
sys_hps_dma_data_rlast(dac_hp1_axi_rlast),
sys_hps_dma_data_rvalid(dac_hp1_axi_rvalid),
sys_hps_dma_data_rready(dac_hp1_axi_rready),
sys_hps_ddr_mem_ck(hps_ddr_clk_p),
sys_hps_ddr_mem_ck_n(hps_ddr_clk_n),
sys_hps_ddr_mem_a(hps_ddr_a),
sys_hps_ddr_mem_act_n(hps_ddr_act_n),
sys_hps_ddr_mem_ba(hps_ddr_ba),
sys_hps_ddr_mem_bg(hps_ddr_bg),
sys_hps_ddr_mem_cke(hps_ddr_cke),
sys_hps_ddr_mem_cs_n(hps_ddr_cs_n),
sys_hps_ddr_mem_odt(hps_ddr_odt),
sys_hps_ddr_mem_reset_n(hps_ddr_reset_n),
sys_hps_ddr_mem_par(hps_ddr_par),
sys_hps_ddr_mem_alert_n(hps_ddr_alert_n),
.sys_hps_ddr_mem_dqs(hps_ddr_dqs_p),
.sys_hps_ddr_mem_dqs_n(hps_ddr_dqs_n),
.sys_hps_ddr_mem_dq(hps_ddr_dq),
.sys_hps_ddr_mem_dbi_n(hps_ddr_dbi_n),
.sys_hps_ddr_oct_oct_rzqin(hps_ddr_rzq),
.sys_hps_ddr_ref_clk_clk(hps_ddr_ref_clk),
.sys_hps_ddr_rstn_reset_n(sys_resetn),
.sys_spi_MISO(spi_miso),
.sys_spi_MOSI(spi_mosi),
.sys_spi_SCLK(spi_clk),
.sys_spi_SS_n(spi_csn),
.sys_i2c_sda_in(fpga_i2c_sda_in),
.sys_i2c_scl_in(fpga_i2c_scl_in),
.sys_i2c_sda_oe(fpga_i2c_sda_oe),
.sys_i2c_scl_oe(fpga_i2c_scl_oe),
.fmc_i2c_sda_in(fmc_i2c_sda_in),
.fmc_i2c_scl_in(fmc_i2c_scl_in),
.fmc_i2c_sda_oe(fmc_i2c_sda_oe),
.fmc_i2c_scl_oe(fmc_i2c_scl_oe),
.irq_irq({s_dac_dma_irq, s_adc_dma_irq, {2{1'b0}}})
)
```

Module instance of inst_system_ps_wrapper for the built in CPU.

system_pl_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl only for zc702 board.

License MIT

system_pl_wrapper

```
module system_pl_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
0,
parameter
FPGA_FAMILY
 =
0,
parameter
SPEED_GRADE
```

```
 =
0,
parameter
DEV_PACKAGE
 =
0,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0,
parameter
DELAY_REFCLK_FREQUENCY
 =
200
) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_
```

System wrapper for pl only for zc702 board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 1 is for 7 series.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 10 is for -1.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 14 is for cl.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

axi_aclk	AXI Lite control bus
axi_aresetn	AXI Lite control bus
s_axi_awvalid	AXI Lite control bus
s_axi_awaddr	AXI Lite control bus
s_axi_awready	AXI Lite control bus
s_axi_awprot	AXI Lite control bus
s_axi_wvalid	AXI Lite control bus
s_axi_wdata	AXI Lite control bus
s_axi_wstrb	AXI Lite control bus
s_axi_wready	AXI Lite control bus
s_axi_bvalid	AXI Lite control bus
s_axi_bresp	AXI Lite control bus
s_axi_bready	AXI Lite control bus

s_axi_arvalid	AXI Lite control bus
s_axi_araddr	AXI Lite control bus
s_axi_arready	AXI Lite control bus
s_axi_arprot	AXI Lite control bus
s_axi_rvalid	AXI Lite control bus
s_axi_rready	AXI Lite control bus
s_axi_rresp	AXI Lite control bus
s_axi_rdata	AXI Lite control bus
adc_dma_irq	fmcomms2-3 ADC irq
dac_dma_irq	fmcomms2-3 DAC irq
delay_clk	fmcomms2-3 delay clock
rx_clk_in_p	fmcomms2-3 receive clock in
rx_clk_in_n	fmcomms2-3 receive clock in
rx_frame_in_p	fmcomms2-3 receive frame
rx_frame_in_n	fmcomms2-3 receive frame
rx_data_in_p	fmcomms2-3 receive lvds data
rx_data_in_n	fmcomms2-3 receive lvds data
tx_clk_out_p	fmcomms2-3 transmit clock
tx_clk_out_n	fmcomms2-3 transmit clock
tx_frame_out_p	fmcomms2-3 transmit frame
tx_frame_out_n	fmcomms2-3 transmit frame
tx_data_out_p	fmcomms2-3 transmit lvds data
tx_data_out_n	fmcomms2-3 transmit lvds data
enable	fmcomms2-3 enable
txnrx	fmcomms2-3 txnrx select
up_enable	fmcomms2-3 enable input
up_txnrx	fmcomms2-3 txnrx select input
tdd_sync_t	fmcomms2-3 TDD sync i/o
tdd_sync_i	fmcomms2-3 TDD sync i/o
tdd_sync_o	fmcomms2-3 TDD sync i/o
adc_m_dest_axi_awaddr	fmcomms2-3 ADC DMA
adc_m_dest_axi_awlen	fmcomms2-3 ADC DMA
adc_m_dest_axi_awsize	fmcomms2-3 ADC DMA
adc_m_dest_axi_awburst	fmcomms2-3 ADC DMA
adc_m_dest_axi_awprot	fmcomms2-3 ADC DMA
adc_m_dest_axi_awcache	fmcomms2-3 ADC DMA
adc_m_dest_axi_awvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_awready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wdata	fmcomms2-3 ADC DMA
adc_m_dest_axi_wstrb	fmcomms2-3 ADC DMA
adc_m_dest_axi_wready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wvalid	fmcomms2-3 ADC DMA

adc_m_dest_axi_wlast	fmcomms2-3 ADC DMA
adc_m_dest_axi_bvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_bresp	fmcomms2-3 ADC DMA
adc_m_dest_axi_bready	fmcomms2-3 ADC DMA
dac_m_src_axi_arready	fmcomms2-3 DAC DMA
dac_m_src_axi_arvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_araddr	fmcomms2-3 DAC DMA
dac_m_src_axi_arlen	fmcomms2-3 DAC DMA
dac_m_src_axi_arsize	fmcomms2-3 DAC DMA
dac_m_src_axi_arburst	fmcomms2-3 DAC DMA
dac_m_src_axi_arprot	fmcomms2-3 DAC DMA
dac_m_src_axi_arcache	fmcomms2-3 DAC DMA
dac_m_src_axi_rdata	fmcomms2-3 DAC DMA
dac_m_src_axi_rready	fmcomms2-3 DAC DMA
dac_m_src_axi_rvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_rresp	fmcomms2-3 DAC DMA
dac_m_src_axi_rlast	fmcomms2-3 DAC DMA
iic_sda_fmc	i2c for fmc
iic_scl_fmc	i2c for fmc
iic2intc_irpt	i2c for fmc

INSTANTIANTED MODULES

iic_sda_iobuf

```
ad_iobuf #(
                                                                        .
DATA_WIDTH(1)
) iic_sda_iobuf ( .dio_t (sda_t), .dio_i (sda_o), .dio_o (sda_i), .dio_p (i
```

Tristate i2c sda

iic_scl_iobuf

```
ad_iobuf #(
                                                                        .
DATA_WIDTH(1)
) iic_scl_iobuf ( .dio_t (scl_t), .dio_i (scl_o), .dio_o (scl_i), .dio_p (i
```

Tristate i2c scl

inst_ad9361_pl_wrapper

```
ad9361_pl_wrapper #(
                                                                        .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                        .
FPGA_FAMILY(FPGA_FAMILY),
                                                                        .
SPEED_GRADE(SPEED_GRADE),
                                                                        .
DEV_PACKAGE(DEV_PACKAGE),
                                                                        .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                        .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                        .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_ad9361_pl_wrapper ( .axi_aclk(axi_aclk), .axi_aresetn(axi_aresetn),
```

Module instance of ad9361_pl_wrapper for the fmcomms2-3 device.

inst_axi_crossbar_pl

```
axi_crossbar_pl inst_axi_crossbar_pl (
                                                                        .
aclk(axi_aclk),
                                                                        .
aresetn(axi_aresetn),
                                                                        .
s_axi_awaddr(s_axi_awaddr),
                                                                        .
s_axi_awprot(s_axi_awprot),
                                                                        .
s_axi_awvalid(s_axi_awvalid),
                                                                        .
s_axi_awready(s_axi_awready),
                                                                        .
s_axi_wdata(s_axi_wdata),
                                                                        .
s_axi_wstrb(s_axi_wstrb),
                                                                        .
s_axi_wvalid(s_axi_wvalid),
                                                                        .
s_axi_wready(s_axi_wready),
                                                                        .
s_axi_bresp(s_axi_bresp),
                                                                        .
s_axi_bvalid(s_axi_bvalid),
                                                                        .
s_axi_bready(s_axi_bready),
                                                                        .
s_axi_araddr(s_axi_araddr),
                                                                        .
s_axi_arprot(s_axi_arprot),
                                                                        .
s_axi_arvalid(s_axi_arvalid),
                                                                        .
s_axi_arready(s_axi_arready),
                                                                        .
s_axi_rdata(s_axi_rdata),
                                                                        .
s_axi_rresp(s_axi_rresp),
                                                                        .
s_axi_rvalid(s_axi_rvalid),
                                                                        .
s_axi_rready(s_axi_rready),
                                                                         .
 m_axi_awaddr({iic_fmc_axi_awaddr, connect_axi_awaddr}),
                                                                         .
 m_axi_awprot({iic_fmc_axi_awprot, connect_axi_awprot}),
                                                                         .
 m_axi_awvalid({iic_fmc_axi_awvalid, connect_axi_awvalid}),
                                                                         .
 m_axi_awready({iic_fmc_axi_awready, connect_axi_awready}),
                                                                         .
 m_axi_wdata({iic_fmc_axi_wdata, connect_axi_wdata}),
                                                                         .
 m_axi_wstrb({iic_fmc_axi_wstrb, connect_axi_wstrb}),
                                                                         .
 m_axi_wvalid({iic_fmc_axi_wvalid, connect_axi_wvalid}),
                                                                         .
 m_axi_wready({iic_fmc_axi_wready, connect_axi_wready}),
                                                                         .
 m_axi_bresp({iic_fmc_axi_bresp, connect_axi_bresp}),
                                                                         .
 m_axi_bvalid({iic_fmc_axi_bvalid, connect_axi_bvalid}),
                                                                         .
 m_axi_bready({iic_fmc_axi_bready, connect_axi_bready}),
                                                                         .
 m_axi_araddr({iic_fmc_axi_araddr, connect_axi_araddr}),
                                                                         .
 m_axi_arprot({iic_fmc_axi_arprot, connect_axi_arprot}),
                                                                         .
 m_axi_arvalid({iic_fmc_axi_arvalid, connect_axi_arvalid}),
                                                                         .
 m_axi_arready({iic_fmc_axi_arready, connect_axi_arready}),
                                                                         .
 m_axi_rdata({iic_fmc_axi_rdata, connect_axi_rdata}),
                                                                         .
 m_axi_rresp({iic_fmc_axi_rresp, connect_axi_rresp}),
                                                                         .
 m_axi_rvalid({iic_fmc_axi_rvalid, connect_axi_rvalid}),
                                                                         .
 m_axi_rready({iic_fmc_axi_rready, connect_axi_rready})
)
```

Module instance of axi_crossbar_pl for the fmcomms2-3 device.

inst_axi_iic_fmc

```
 axi_iic_fmc inst_axi_iic_fmc (
                                                                         .
 s_axi_aclk(axi_aclk),
                                                                         .
 s_axi_aresetn(axi_aresetn),
                                                                         .
 iic2intc_irpt(iic2intc_irpt),
                                                                         .
 s_axi_awaddr(iic_fmc_axi_awaddr[8:0]),
                                                                         .
 s_axi_awvalid(iic_fmc_axi_awvalid),
                                                                         .
 s_axi_awready(iic_fmc_axi_awready),
                                                                         .
 s_axi_wdata(iic_fmc_axi_wdata),
                                                                         .
 s_axi_wstrb(iic_fmc_axi_wstrb),
                                                                         .
 s_axi_wvalid(iic_fmc_axi_wvalid),
                                                                                   .
 s_axi_wready(iic_fmc_axi_wready),
                                                                                   .
 s_axi_bresp(iic_fmc_axi_bresp),
                                                                                   .
 s_axi_bvalid(iic_fmc_axi_bvalid),
                                                                                   .
 s_axi_bready(iic_fmc_axi_bready),
                                                                                   .
 s_axi_araddr(iic_fmc_axi_araddr[8:0]),
                                                                                   .
 s_axi_arvalid(iic_fmc_axi_arvalid),
                                                                                   .
 s_axi_arready(iic_fmc_axi_arready),
                                                                                   .
 s_axi_rdata(iic_fmc_axi_rdata),
                                                                                   .
 s_axi_rresp(iic_fmc_axi_rresp),
                                                                                   .
 s_axi_rvalid(iic_fmc_axi_rvalid),
                                                                                   .
 s_axi_rready(iic_fmc_axi_rready),
                                                                                   .
 sda_i(sda_i),
                                                                                   .
 sda_o(sda_o),
                                                                                   .
 sda_t(sda_t),
                                                                                   .
 scl_i(scl_i),
                                                                                   .
 scl_o(scl_o),
                                                                                   .
 scl_t(scl_t),
                                                                                   .
 gpo()
)
```

Module instance of axi_iic_fmc for the fmcomms2-3 device.

system_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl and ps for zc702 board.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
1,
parameter
FPGA_FAMILY
 =
4,
parameter
SPEED_GRADE
```

```
 =
10,
parameter
DEV_PACKAGE
 =
14,
parameter
DELAY_REFCLK_FREQUENCY
 =
200,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0
) ( inout [14:0] ddr_addr, inout [ 2:0] ddr_ba, inout ddr_cas_n, inout ddr_
```

System wrapper for pl and ps for zc702 board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 1 is for 7 series.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 10 is for -1.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 14 is for cl.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

ddr_addr	DDR interface
ddr_ba	DDR interface
ddr_cas_n	DDR interface
ddr_ck_n	DDR interface
ddr_ck_p	DDR interface
ddr_cke	DDR interface
ddr_cs_n	DDR interface
ddr_dm	DDR interface
ddr_dq	DDR interface
ddr_dqs_n	DDR interface
ddr_dqs_p	DDR interface
ddr_odt	DDR interface
ddr_ras_n	DDR interface

ddr_reset_n	DDR interface
ddr_we_n	DDR interface
fixed_io_ddr_vrn	DDR interface
fixed_io_ddr_vrp	DDR interface
fixed_io_mio	ps mio
fixed_io_ps_clk	ps clk
fixed_io_ps_porb	ps por
fixed_io_ps_srstb	ps rst
iic_scl_fmc	fmcomms2-3 i2c
iic_sda_fmc	fmcomms2-3 i2c
gpio_bd	gpio
rx_clk_in_p	fmcomms2-3 rx clk
rx_clk_in_n	fmcomms2-3 rx clk
rx_frame_in_p	fmcomms2-3 rx frame
rx_frame_in_n	fmcomms2-3 rx frame
rx_data_in_p	fmcomms2-3 rx data
rx_data_in_n	fmcomms2-3 rx data
tx_clk_out_p	fmcomms2-3 tx clk
tx_clk_out_n	fmcomms2-3 tx clk
tx_frame_out_p	fmcomms2-3 tx frame
tx_frame_out_n	fmcomms2-3 tx frame
tx_data_out_p	fmcomms2-3 tx data
tx_data_out_n	fmcomms2-3 tx data
txnrx	fmcomms2-3 txnrx
enable	fmcomms2-3 enable
gpio_muxout_tx	fmcomms2-3 gpio
gpio_muxout_rx	fmcomms2-3 gpio
gpio_resetb	fmcomms2-3 gpio
gpio_sync	fmcomms2-3 gpio
gpio_en_agc	fmcomms2-3 gpio
gpio_ctl	fmcomms2-3 gpio
gpio_status	fmcomms2-3 gpio
spi_csn	spi chip select
spi_clk	spi clk
spi_mosi	spi master out
spi_miso	spi master in
spi_udc_csn_tx	spi udc chip select tx
spi_udc_csn_rx	spi udc chip select rx
spi_udc_sclk	spi udc clock
spi_udc_data	spi udc data

INSTANTIANTED MODULES

inst_system_pl_wrapper

```
system_pl_wrapper #(
                                                                         .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                         .
FPGA_FAMILY(FPGA_FAMILY),
                                                                         .
SPEED_GRADE(SPEED_GRADE),
                                                                         .
DEV_PACKAGE(DEV_PACKAGE),
                                                                         .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                         .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                         .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_system_pl_wrapper ( .axi_aclk(s_axi_clk), .axi_aresetn(s_axi_aresetn
```

Module instance of system_pl_wrapper for the fmcomms2-3 device.

inst_system_ps_wrapper

```
system_ps_wrapper inst_system_ps_wrapper (
                                                                         .
GPIO_I(gpio_i),
                                                                         .
GPIO_O(gpio_o),
                                                                         .
GPIO_T(gpio_t),
                                                                         .
SPI0_SCLK_I(1'b0),
                                                                         .
SPI0_SCLK_O(spi_clk),
                                                                         .
SPI0_MOSI_I(1'b0),
                                                                         .
SPI0_MOSI_O(spi_mosi),
                                                                         .
SPI0_MISO_I(spi_miso),
                                                                         .
SPI0_SS_I(1'b1),
                                                                         .
SPI0_SS_O(spi_csn),
                                                                         .
SPI1_SCLK_I(1'b0),
                                                                         .
SPI1_SCLK_O(spi_udc_sclk),
                                                                         .
SPI1_MOSI_I(spi_udc_data),
                                                                         .
SPI1_MOSI_O(spi_udc_data),
                                                                         .
SPI1_MISO_I(1'b0),
                                                                         .
SPI1_SS_I(1'b1),
                                                                         .
SPI1_SS_O(spi_udc_csn_tx),
SPI1_SS1_O(spi_udc_csn_rx),
SPI1_SS2_O(),
M_AXI_araddr(w_axi_araddr),
M_AXI_arprot(w_axi_arprot),
M_AXI_arready(w_axi_arready),
M_AXI_arvalid(w_axi_arvalid),
M_AXI_awaddr(w_axi_awaddr),
M_AXI_awprot(w_axi_awprot),
M_AXI_awready(w_axi_awready),
M_AXI_awvalid(w_axi_awvalid),
M_AXI_bready(w_axi_bready),
M_AXI_bresp(w_axi_bresp),
M_AXI_bvalid(w_axi_bvalid),
M_AXI_rdata(w_axi_rdata),
M_AXI_rready(w_axi_rready),
M_AXI_rresp(w_axi_rresp),
M_AXI_rvalid(w_axi_rvalid),
M_AXI_wdata(w_axi_wdata),
M_AXI_wready(w_axi_wready),
M_AXI_wstrb(w_axi_wstrb),
M_AXI_wvalid(w_axi_wvalid),
S_AXI_HP0_arready(),
S_AXI_HP0_awready(adc_hp0_axi_awready),
S_AXI_HP0_bvalid(adc_hp0_axi_bvalid),
S_AXI_HP0_rlast(),
S_AXI_HP0_rvalid(),
S_AXI_HP0_wready(adc_hp0_axi_wready),
S_AXI_HP0_bresp(adc_hp0_axi_bresp),
S_AXI_HP0_rresp(),
S_AXI_HP0_bid(),
S_AXI_HP0_rid(),
S_AXI_HP0_rdata(),
S_AXI_HP0_ACLK(s_axi_clk),
S_AXI_HP0_arvalid(1'b0),
S_AXI_HP0_awvalid(adc_hp0_axi_awvalid),
S_AXI_HP0_bready(adc_hp0_axi_bready),
S_AXI_HP0_rready(1'b0),
S_AXI_HP0_wlast(adc_hp0_axi_wlast),
S_AXI_HP0_wvalid(adc_hp0_axi_wvalid),
S_AXI_HP0_arburst(2'b01),
S_AXI_HP0_arlock(0),
S_AXI_HP0_arsize(3'b011),
S_AXI_HP0_awburst(adc_hp0_axi_awburst),
S_AXI_HP0_awlock(0),
S_AXI_HP0_awsize(adc_hp0_axi_awsize),
S_AXI_HP0_arprot(0),
S_AXI_HP0_awprot(adc_hp0_axi_awprot),
S_AXI_HP0_araddr(0),
S_AXI_HP0_awaddr(adc_hp0_axi_awaddr),
S_AXI_HP0_arcache(4'b0011),
S_AXI_HP0_arlen(0),
S_AXI_HP0_arqos(0),
S_AXI_HP0_awcache(adc_hp0_axi_awcache),
S_AXI_HP0_awlen(adc_hp0_axi_awlen),
S_AXI_HP0_awqos(0),
S_AXI_HP0_arid(0),
S_AXI_HP0_awid(0),
S_AXI_HP0_wid(0),
S_AXI_HP0_wdata(adc_hp0_axi_wdata),
S_AXI_HP0_wstrb(adc_hp0_axi_wstrb),
S_AXI_HP1_arready(dac_hp1_axi_arready),
S_AXI_HP1_awready(),
S_AXI_HP1_bvalid(),
S_AXI_HP1_rlast(dac_hp1_axi_rlast),
S_AXI_HP1_rvalid(dac_hp1_axi_rvalid),
S_AXI_HP1_wready(),
S_AXI_HP1_bresp(),
S_AXI_HP1_rresp(dac_hp1_axi_rresp),
S_AXI_HP1_bid(),
S_AXI_HP1_rid(),
S_AXI_HP1_rdata(dac_hp1_axi_rdata),
S_AXI_HP1_ACLK(s_axi_clk),
S_AXI_HP1_arvalid(dac_hp1_axi_arvalid),
S_AXI_HP1_awvalid(1'b0),
S_AXI_HP1_bready(1'b0),
S_AXI_HP1_rready(dac_hp1_axi_rready),
S_AXI_HP1_wlast(1'b0),
S_AXI_HP1_wvalid(1'b0),
S_AXI_HP1_arburst(dac_hp1_axi_arburst),
S_AXI_HP1_arlock(0),
S_AXI_HP1_arsize(dac_hp1_axi_arsize),
S_AXI_HP1_awburst(2'b01),
S_AXI_HP1_awlock(0),
S_AXI_HP1_awsize(3'b011),
S_AXI_HP1_arprot(dac_hp1_axi_arprot),
S_AXI_HP1_awprot(0),
S_AXI_HP1_araddr(dac_hp1_axi_araddr),
S_AXI_HP1_awaddr(0),
S_AXI_HP1_arcache(dac_hp1_axi_arcache),
S_AXI_HP1_arlen(dac_hp1_axi_arlen),
S_AXI_HP1_arqos(0),
S_AXI_HP1_awcache(4'b0011),
S_AXI_HP1_awlen(0),
S_AXI_HP1_awqos(0),
S_AXI_HP1_arid(0),
S_AXI_HP1_awid(0),
S_AXI_HP1_wid(0),
S_AXI_HP1_wdata(0),
S_AXI_HP1_wstrb(~0),
 IRQ_F2P({{2{1'b0}}, s_adc_dma_irq, s_dac_dma_irq, s_iic2intc_irpt, {11{1'b0
 FCLK_CLK0(s_axi_clk),
 FCLK_CLK1(s_delay_clk),
 FIXED_IO_mio(fixed_io_mio),
 DDR_cas_n(ddr_cas_n),
 DDR_cke(ddr_cke),
 DDR_ck_n(ddr_ck_n),
 DDR_ck_p(ddr_ck_p),
 DDR_cs_n(ddr_cs_n),
 DDR_reset_n(ddr_reset_n),
 DDR_odt(ddr_odt),
 DDR_ras_n(ddr_ras_n),
 DDR_we_n(ddr_we_n),
 DDR_ba(ddr_ba),
 DDR_addr(ddr_addr),
 FIXED_IO_ddr_vrn(fixed_io_ddr_vrn),
 FIXED_IO_ddr_vrp(fixed_io_ddr_vrp),
 DDR_dm(ddr_dm),
 DDR_dq(ddr_dq),
 DDR_dqs_n(ddr_dqs_n),
 DDR_dqs_p(ddr_dqs_p),
 FIXED_IO_ps_srstb(fixed_io_ps_srstb),
 FIXED_IO_ps_clk(fixed_io_ps_clk),
 FIXED_IO_ps_porb(fixed_io_ps_porb),
 peripheral_aresetn(s_axi_aresetn)
)
```

Module instance of inst_system_ps_wrapper for the built in CPU.

system_pl_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

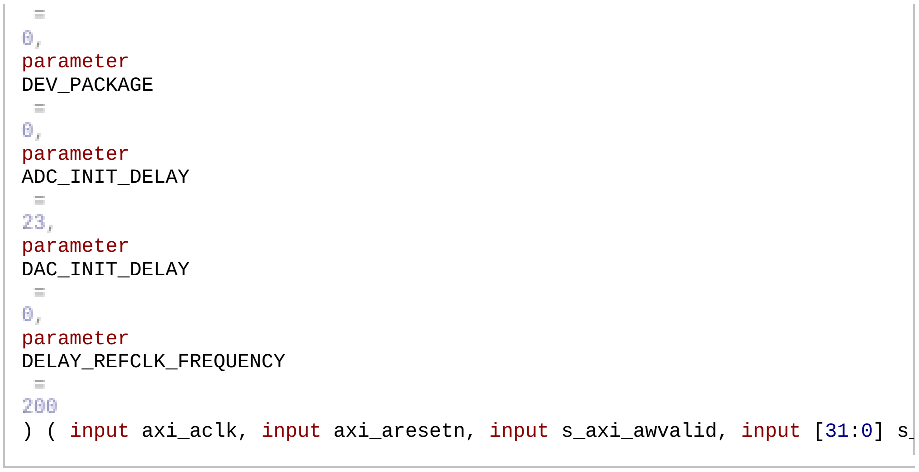
Brief

System wrapper for pl only for zc706 board.

License MIT

system_pl_wrapper

```
module system_pl_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
0,
parameter
FPGA_FAMILY
 =
0,
parameter
SPEED_GRADE
```



```
 =
0,
parameter
DEV_PACKAGE
 =
0,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0,
parameter
DELAY_REFCLK_FREQUENCY
 =
200
) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_
```

System wrapper for pl only for zc706 board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 1 is for 7 series.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 20 is for -2.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 3 is for ff.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

axi_aclk	AXI Lite control bus
axi_aresetn	AXI Lite control bus
s_axi_awvalid	AXI Lite control bus
s_axi_awaddr	AXI Lite control bus
s_axi_awready	AXI Lite control bus
s_axi_awprot	AXI Lite control bus
s_axi_wvalid	AXI Lite control bus
s_axi_wdata	AXI Lite control bus
s_axi_wstrb	AXI Lite control bus
s_axi_wready	AXI Lite control bus
s_axi_bvalid	AXI Lite control bus
s_axi_bresp	AXI Lite control bus
s_axi_bready	AXI Lite control bus

s_axi_arvalid	AXI Lite control bus
s_axi_araddr	AXI Lite control bus
s_axi_arready	AXI Lite control bus
s_axi_arprot	AXI Lite control bus
s_axi_rvalid	AXI Lite control bus
s_axi_rready	AXI Lite control bus
s_axi_rresp	AXI Lite control bus
s_axi_rdata	AXI Lite control bus
adc_dma_irq	fmcomms2-3 ADC irq
dac_dma_irq	fmcomms2-3 DAC irq
delay_clk	fmcomms2-3 delay clock
rx_clk_in_p	fmcomms2-3 receive clock in
rx_clk_in_n	fmcomms2-3 receive clock in
rx_frame_in_p	fmcomms2-3 receive frame
rx_frame_in_n	fmcomms2-3 receive frame
rx_data_in_p	fmcomms2-3 receive lvds data
rx_data_in_n	fmcomms2-3 receive lvds data
tx_clk_out_p	fmcomms2-3 transmit clock
tx_clk_out_n	fmcomms2-3 transmit clock
tx_frame_out_p	fmcomms2-3 transmit frame
tx_frame_out_n	fmcomms2-3 transmit frame
tx_data_out_p	fmcomms2-3 transmit lvds data
tx_data_out_n	fmcomms2-3 transmit lvds data
enable	fmcomms2-3 enable
txnrx	fmcomms2-3 txnrx select
up_enable	fmcomms2-3 enable input
up_txnrx	fmcomms2-3 txnrx select input
tdd_sync_t	fmcomms2-3 TDD sync i/o
tdd_sync_i	fmcomms2-3 TDD sync i/o
tdd_sync_o	fmcomms2-3 TDD sync i/o
adc_m_dest_axi_awaddr	fmcomms2-3 ADC DMA
adc_m_dest_axi_awlen	fmcomms2-3 ADC DMA
adc_m_dest_axi_awsize	fmcomms2-3 ADC DMA
adc_m_dest_axi_awburst	fmcomms2-3 ADC DMA
adc_m_dest_axi_awprot	fmcomms2-3 ADC DMA
adc_m_dest_axi_awcache	fmcomms2-3 ADC DMA
adc_m_dest_axi_awvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_awready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wdata	fmcomms2-3 ADC DMA
adc_m_dest_axi_wstrb	fmcomms2-3 ADC DMA
adc_m_dest_axi_wready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wvalid	fmcomms2-3 ADC DMA

adc_m_dest_axi_wlast	fmcomms2-3 ADC DMA
adc_m_dest_axi_bvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_bresp	fmcomms2-3 ADC DMA
adc_m_dest_axi_bready	fmcomms2-3 ADC DMA
dac_m_src_axi_arready	fmcomms2-3 DAC DMA
dac_m_src_axi_arvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_araddr	fmcomms2-3 DAC DMA
dac_m_src_axi_arlen	fmcomms2-3 DAC DMA
dac_m_src_axi_arsize	fmcomms2-3 DAC DMA
dac_m_src_axi_arburst	fmcomms2-3 DAC DMA
dac_m_src_axi_arprot	fmcomms2-3 DAC DMA
dac_m_src_axi_arcache	fmcomms2-3 DAC DMA
dac_m_src_axi_rdata	fmcomms2-3 DAC DMA
dac_m_src_axi_rready	fmcomms2-3 DAC DMA
dac_m_src_axi_rvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_rresp	fmcomms2-3 DAC DMA
dac_m_src_axi_rlast	fmcomms2-3 DAC DMA
iic_sda_fmc	i2c for fmc
iic_scl_fmc	i2c for fmc
iic2intc_irpt	i2c for fmc

INSTANTIANTED MODULES

iic_sda_iobuf

```
ad_iobuf #(
                                                                               .
DATA_WIDTH(1)
) iic_sda_iobuf ( .dio_t (sda_t), .dio_i (sda_o), .dio_o (sda_i), .dio_p (
```

Tristate i2c sda

iic_scl_iobuf

```
ad_iobuf #(
                                                                               .
DATA_WIDTH(1)
) iic_scl_iobuf ( .dio_t (scl_t), .dio_i (scl_o), .dio_o (scl_i), .dio_p (
```

Tristate i2c scl

inst_ad9361_pl_wrapper

```
ad9361_pl_wrapper #(
                                                                        .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                        .
FPGA_FAMILY(FPGA_FAMILY),
                                                                        .
SPEED_GRADE(SPEED_GRADE),
                                                                        .
DEV_PACKAGE(DEV_PACKAGE),
                                                                        .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                        .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                        .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_ad9361_pl_wrapper ( .axi_aclk(axi_aclk), .axi_aresetn(axi_aresetn),
```

Module instance of ad9361_pl_wrapper for the fmcomms2-3 device.

inst_axi_crossbar_pl

```
axi_crossbar_pl inst_axi_crossbar_pl (
                                                                        .
aclk(axi_aclk),
                                                                        .
aresetn(axi_aresetn),
                                                                        .
s_axi_awaddr(s_axi_awaddr),
                                                                        .
s_axi_awprot(s_axi_awprot),
                                                                        .
s_axi_awvalid(s_axi_awvalid),
                                                                        .
s_axi_awready(s_axi_awready),
                                                                        .
s_axi_wdata(s_axi_wdata),
                                                                        .
s_axi_wstrb(s_axi_wstrb),
                                                                        .
s_axi_wvalid(s_axi_wvalid),
                                                                        .
s_axi_wready(s_axi_wready),
                                                                        .
s_axi_bresp(s_axi_bresp),
                                                                        .
s_axi_bvalid(s_axi_bvalid),
                                                                        .
s_axi_bready(s_axi_bready),
                                                                        .
s_axi_araddr(s_axi_araddr),
                                                                        .
s_axi_arprot(s_axi_arprot),
                                                                        .
s_axi_arvalid(s_axi_arvalid),
                                                                        .
s_axi_arready(s_axi_arready),
                                                                        .
s_axi_rdata(s_axi_rdata),
                                                                        .
s_axi_rresp(s_axi_rresp),
                                                                        .
s_axi_rvalid(s_axi_rvalid),
                                                                        .
s_axi_rready(s_axi_rready),
                                                                          .
 m_axi_awaddr({iic_fmc_axi_awaddr, connect_axi_awaddr}),
                                                                          .
 m_axi_awprot({iic_fmc_axi_awprot, connect_axi_awprot}),
                                                                          .
 m_axi_awvalid({iic_fmc_axi_awvalid, connect_axi_awvalid}),
                                                                          .
 m_axi_awready({iic_fmc_axi_awready, connect_axi_awready}),
                                                                          .
 m_axi_wdata({iic_fmc_axi_wdata, connect_axi_wdata}),
                                                                          .
 m_axi_wstrb({iic_fmc_axi_wstrb, connect_axi_wstrb}),
                                                                          .
 m_axi_wvalid({iic_fmc_axi_wvalid, connect_axi_wvalid}),
                                                                          .
 m_axi_wready({iic_fmc_axi_wready, connect_axi_wready}),
                                                                          .
 m_axi_bresp({iic_fmc_axi_bresp, connect_axi_bresp}),
                                                                          .
 m_axi_bvalid({iic_fmc_axi_bvalid, connect_axi_bvalid}),
                                                                          .
 m_axi_bready({iic_fmc_axi_bready, connect_axi_bready}),
                                                                          .
 m_axi_araddr({iic_fmc_axi_araddr, connect_axi_araddr}),
                                                                          .
 m_axi_arprot({iic_fmc_axi_arprot, connect_axi_arprot}),
                                                                          .
 m_axi_arvalid({iic_fmc_axi_arvalid, connect_axi_arvalid}),
                                                                          .
 m_axi_arready({iic_fmc_axi_arready, connect_axi_arready}),
                                                                          .
 m_axi_rdata({iic_fmc_axi_rdata, connect_axi_rdata}),
                                                                          .
 m_axi_rresp({iic_fmc_axi_rresp, connect_axi_rresp}),
                                                                          .
 m_axi_rvalid({iic_fmc_axi_rvalid, connect_axi_rvalid}),
                                                                          .
 m_axi_rready({iic_fmc_axi_rready, connect_axi_rready})
)
```

Module instance of axi_crossbar_pl for the fmcomms2-3 device.

inst_axi_iic_fmc

```
 axi_iic_fmc inst_axi_iic_fmc (
                                                                          .
 s_axi_aclk(axi_aclk),
                                                                          .
 s_axi_aresetn(axi_aresetn),
                                                                          .
 iic2intc_irpt(iic2intc_irpt),
                                                                          .
 s_axi_awaddr(iic_fmc_axi_awaddr[8:0]),
                                                                          .
 s_axi_awvalid(iic_fmc_axi_awvalid),
                                                                          .
 s_axi_awready(iic_fmc_axi_awready),
                                                                          .
 s_axi_wdata(iic_fmc_axi_wdata),
                                                                          .
 s_axi_wstrb(iic_fmc_axi_wstrb),
                                                                          .
 s_axi_wvalid(iic_fmc_axi_wvalid),
                                                                         .
 s_axi_wready(iic_fmc_axi_wready),
                                                                         .
 s_axi_bresp(iic_fmc_axi_bresp),
                                                                         .
 s_axi_bvalid(iic_fmc_axi_bvalid),
                                                                         .
 s_axi_bready(iic_fmc_axi_bready),
                                                                         .
 s_axi_araddr(iic_fmc_axi_araddr[8:0]),
                                                                         .
 s_axi_arvalid(iic_fmc_axi_arvalid),
                                                                         .
 s_axi_arready(iic_fmc_axi_arready),
                                                                         .
 s_axi_rdata(iic_fmc_axi_rdata),
                                                                         .
 s_axi_rresp(iic_fmc_axi_rresp),
                                                                         .
 s_axi_rvalid(iic_fmc_axi_rvalid),
                                                                         .
 s_axi_rready(iic_fmc_axi_rready),
                                                                         .
 sda_i(sda_i),
                                                                         .
 sda_o(sda_o),
                                                                         .
 sda_t(sda_t),
                                                                         .
 scl_i(scl_i),
                                                                         .
 scl_o(scl_o),
                                                                         .
 scl_t(scl_t),
                                                                         .
 gpo()
)
```

Module instance of axi_iic_fmc for the fmcomms2-3 device.

system_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl and ps for zc706 board.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
1,
parameter
FPGA_FAMILY
 =
4,
parameter
SPEED_GRADE
```

```
 =
20,
parameter
DEV_PACKAGE
 =
3,
parameter
DELAY_REFCLK_FREQUENCY
 =
200,
parameter
ADC_INIT_DELAY
 =
20,
parameter
DAC_INIT_DELAY
 =
0
) ( inout [14:0] ddr_addr, inout [ 2:0] ddr_ba, inout ddr_cas_n, inout ddr_
```

System wrapper for pl and ps for zc706 board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 1 is for 7 series.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 20 is for -2.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 3 is for ff.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

ddr_addr	DDR interface
ddr_ba	DDR interface
ddr_cas_n	DDR interface
ddr_ck_n	DDR interface
ddr_ck_p	DDR interface
ddr_cke	DDR interface
ddr_cs_n	DDR interface
ddr_dm	DDR interface
ddr_dq	DDR interface
ddr_dqs_n	DDR interface
ddr_dqs_p	DDR interface
ddr_odt	DDR interface
ddr_ras_n	DDR interface

ddr_reset_n	DDR interface
ddr_we_n	DDR interface
fixed_io_ddr_vrn	DDR interface
fixed_io_ddr_vrp	DDR interface
fixed_io_mio	ps mio
fixed_io_ps_clk	ps clk
fixed_io_ps_porb	ps por
fixed_io_ps_srstb	ps rst
iic_scl_fmc	fmcomms2-3 i2c
iic_sda_fmc	fmcomms2-3 i2c
gpio_bd	gpio
rx_clk_in_p	fmcomms2-3 rx clk
rx_clk_in_n	fmcomms2-3 rx clk
rx_frame_in_p	fmcomms2-3 rx frame
rx_frame_in_n	fmcomms2-3 rx frame
rx_data_in_p	fmcomms2-3 rx data
rx_data_in_n	fmcomms2-3 rx data
tx_clk_out_p	fmcomms2-3 tx clk
tx_clk_out_n	fmcomms2-3 tx clk
tx_frame_out_p	fmcomms2-3 tx frame
tx_frame_out_n	fmcomms2-3 tx frame
tx_data_out_p	fmcomms2-3 tx data
tx_data_out_n	fmcomms2-3 tx data
txnrx	fmcomms2-3 txnrx
enable	fmcomms2-3 enable
gpio_muxout_tx	fmcomms2-3 gpio
gpio_muxout_rx	fmcomms2-3 gpio
gpio_resetb	fmcomms2-3 gpio
gpio_sync	fmcomms2-3 gpio
gpio_en_agc	fmcomms2-3 gpio
gpio_ctl	fmcomms2-3 gpio
gpio_status	fmcomms2-3 gpio
spi_csn	spi chip select
spi_clk	spi clk
spi_mosi	spi master out
spi_miso	spi master in
spi_udc_csn_tx	spi udc chip select tx
spi_udc_csn_rx	spi udc chip select rx
spi_udc_sclk	spi udc clock
spi_udc_data	spi udc data

INSTANTIANTED MODULES

inst_system_pl_wrapper

```
system_pl_wrapper #(
                                                                        .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                        .
FPGA_FAMILY(FPGA_FAMILY),
                                                                        .
SPEED_GRADE(SPEED_GRADE),
                                                                        .
DEV_PACKAGE(DEV_PACKAGE),
                                                                        .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                        .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                        .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_system_pl_wrapper ( .axi_aclk(s_axi_clk), .axi_aresetn(s_axi_areset
```

Module instance of system_pl_wrapper for the fmcomms2-3 device.

inst_system_ps_wrapper

```
system_ps_wrapper inst_system_ps_wrapper (
                                                                        .
GPIO_I(gpio_i),
                                                                        .
GPIO_O(gpio_o),
                                                                        .
GPIO_T(gpio_t),
                                                                        .
SPI0_SCLK_I(1'b0),
                                                                        .
SPI0_SCLK_O(spi_clk),
                                                                        .
SPI0_MOSI_I(1'b0),
                                                                        .
SPI0_MOSI_O(spi_mosi),
                                                                        .
SPI0_MISO_I(spi_miso),
                                                                        .
SPI0_SS_I(1'b1),
                                                                        .
SPI0_SS_O(spi_csn),
                                                                        .
SPI1_SCLK_I(1'b0),
                                                                        .
SPI1_SCLK_O(spi_udc_sclk),
                                                                        .
SPI1_MOSI_I(spi_udc_data),
                                                                        .
SPI1_MOSI_O(spi_udc_data),
                                                                        .
SPI1_MISO_I(1'b0),
                                                                        .
SPI1_SS_I(1'b1),
                                                                        .
SPI1_SS_O(spi_udc_csn_tx),
SPI1_SS1_O(spi_udc_csn_rx),
SPI1_SS2_O(),
M_AXI_araddr(w_axi_araddr),
M_AXI_arprot(w_axi_arprot),
M_AXI_arready(w_axi_arready),
M_AXI_arvalid(w_axi_arvalid),
M_AXI_awaddr(w_axi_awaddr),
M_AXI_awprot(w_axi_awprot),
M_AXI_awready(w_axi_awready),
M_AXI_awvalid(w_axi_awvalid),
M_AXI_bready(w_axi_bready),
M_AXI_bresp(w_axi_bresp),
M_AXI_bvalid(w_axi_bvalid),
M_AXI_rdata(w_axi_rdata),
M_AXI_rready(w_axi_rready),
M_AXI_rresp(w_axi_rresp),
M_AXI_rvalid(w_axi_rvalid),
M_AXI_wdata(w_axi_wdata),
M_AXI_wready(w_axi_wready),
M_AXI_wstrb(w_axi_wstrb),
M_AXI_wvalid(w_axi_wvalid),
S_AXI_HP0_arready(),
S_AXI_HP0_awready(adc_hp0_axi_awready),
S_AXI_HP0_bvalid(adc_hp0_axi_bvalid),
S_AXI_HP0_rlast(),
S_AXI_HP0_rvalid(),
S_AXI_HP0_wready(adc_hp0_axi_wready),
S_AXI_HP0_bresp(adc_hp0_axi_bresp),
S_AXI_HP0_rresp(),
S_AXI_HP0_bid(),
S_AXI_HP0_rid(),
S_AXI_HP0_rdata(),
S_AXI_HP0_ACLK(s_axi_clk),
S_AXI_HP0_arvalid(1'b0),
S_AXI_HP0_awvalid(adc_hp0_axi_awvalid),
S_AXI_HP0_bready(adc_hp0_axi_bready),
S_AXI_HP0_rready(1'b0),
S_AXI_HP0_wlast(adc_hp0_axi_wlast),
S_AXI_HP0_wvalid(adc_hp0_axi_wvalid),
S_AXI_HP0_arburst(2'b01),
S_AXI_HP0_arlock(0),
S_AXI_HP0_arsize(3'b011),
S_AXI_HP0_awburst(adc_hp0_axi_awburst),
S_AXI_HP0_awlock(0),
S_AXI_HP0_awsize(adc_hp0_axi_awsize),
S_AXI_HP0_arprot(0),
S_AXI_HP0_awprot(adc_hp0_axi_awprot),
S_AXI_HP0_araddr(0),
S_AXI_HP0_awaddr(adc_hp0_axi_awaddr),
S_AXI_HP0_arcache(4'b0011),
S_AXI_HP0_arlen(0),
S_AXI_HP0_arqos(0),
S_AXI_HP0_awcache(adc_hp0_axi_awcache),
S_AXI_HP0_awlen(adc_hp0_axi_awlen),
S_AXI_HP0_awqos(0),
S_AXI_HP0_arid(0),
S_AXI_HP0_awid(0),
S_AXI_HP0_wid(0),
S_AXI_HP0_wdata(adc_hp0_axi_wdata),
S_AXI_HP0_wstrb(adc_hp0_axi_wstrb),
S_AXI_HP1_arready(dac_hp1_axi_arready),
S_AXI_HP1_awready(),
S_AXI_HP1_bvalid(),
S_AXI_HP1_rlast(dac_hp1_axi_rlast),
S_AXI_HP1_rvalid(dac_hp1_axi_rvalid),
S_AXI_HP1_wready(),
S_AXI_HP1_bresp(),
S_AXI_HP1_rresp(dac_hp1_axi_rresp),
S_AXI_HP1_bid(),
S_AXI_HP1_rid(),
S_AXI_HP1_rdata(dac_hp1_axi_rdata),
S_AXI_HP1_ACLK(s_axi_clk),
S_AXI_HP1_arvalid(dac_hp1_axi_arvalid),
S_AXI_HP1_awvalid(1'b0),
S_AXI_HP1_bready(1'b0),
S_AXI_HP1_rready(dac_hp1_axi_rready),
S_AXI_HP1_wlast(1'b0),
S_AXI_HP1_wvalid(1'b0),
S_AXI_HP1_arburst(dac_hp1_axi_arburst),
S_AXI_HP1_arlock(0),
S_AXI_HP1_arsize(dac_hp1_axi_arsize),
S_AXI_HP1_awburst(2'b01),
S_AXI_HP1_awlock(0),
S_AXI_HP1_awsize(3'b011),
S_AXI_HP1_arprot(dac_hp1_axi_arprot),
S_AXI_HP1_awprot(0),
S_AXI_HP1_araddr(dac_hp1_axi_araddr),
S_AXI_HP1_awaddr(0),
S_AXI_HP1_arcache(dac_hp1_axi_arcache),
S_AXI_HP1_arlen(dac_hp1_axi_arlen),
S_AXI_HP1_arqos(0),
S_AXI_HP1_awcache(4'b0011),
S_AXI_HP1_awlen(0),
S_AXI_HP1_awqos(0),
S_AXI_HP1_arid(0),
S_AXI_HP1_awid(0),
S_AXI_HP1_wid(0),
S_AXI_HP1_wdata(0),
S_AXI_HP1_wstrb(~0),
 IRQ_F2P({{2{1'b0}}, s_adc_dma_irq, s_dac_dma_irq, s_iic2intc_irpt, {11{1'b0
 FCLK_CLK0(s_axi_clk),
 FCLK_CLK1(s_delay_clk),
 FIXED_IO_mio(fixed_io_mio),
 DDR_cas_n(ddr_cas_n),
 DDR_cke(ddr_cke),
 DDR_ck_n(ddr_ck_n),
 DDR_ck_p(ddr_ck_p),
 DDR_cs_n(ddr_cs_n),
 DDR_reset_n(ddr_reset_n),
 DDR_odt(ddr_odt),
 DDR_ras_n(ddr_ras_n),
 DDR_we_n(ddr_we_n),
 DDR_ba(ddr_ba),
 DDR_addr(ddr_addr),
 FIXED_IO_ddr_vrn(fixed_io_ddr_vrn),
 FIXED_IO_ddr_vrp(fixed_io_ddr_vrp),
 DDR_dm(ddr_dm),
 DDR_dq(ddr_dq),
 DDR_dqs_n(ddr_dqs_n),
 DDR_dqs_p(ddr_dqs_p),
 FIXED_IO_ps_srstb(fixed_io_ps_srstb),
 FIXED_IO_ps_clk(fixed_io_ps_clk),
 FIXED_IO_ps_porb(fixed_io_ps_porb),
 peripheral_aresetn(s_axi_aresetn)
)
```

Module instance of inst_system_ps_wrapper for the built in CPU.

system_pl_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl only for zcu102 board.

License MIT

system_pl_wrapper

```
module system_pl_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
0,
parameter
FPGA_FAMILY
 =
0,
parameter
SPEED_GRADE
```

```
 =
0,
parameter
DEV_PACKAGE
 =
0,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0,
parameter
DELAY_REFCLK_FREQUENCY
 =
200
) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_
```

System wrapper for pl only for zcu102 board.

Parameters

FPGA_TECHNOLOGY
parameter
Type of FPGA, such as Ultrascale, Arria 10. 3 is for ultrascale+.

FPGA_FAMILY
parameter
Sub type of fpga, such as GX, SX, etc. 4 is for zynq.

SPEED_GRADE
parameter
Number that corresponds to the ships recommeneded speed. 20 is for -2.

DEV_PACKAGE
parameter
Specify a number that is equal to the manufactures package. 3 is for ff.

DELAY_REFCLK_FREQUENCY
parameter
Reference clock frequency used for ad_data_in instances

ADC_INIT_DELAY
parameter
Initial Delay for the ADC

DAC_INIT_DELAY
parameter
Initial Delay for the DAC

Ports

axi_aclk	AXI Lite control bus
axi_aresetn	AXI Lite control bus
s_axi_awvalid	AXI Lite control bus
s_axi_awaddr	AXI Lite control bus
s_axi_awready	AXI Lite control bus
s_axi_awprot	AXI Lite control bus
s_axi_wvalid	AXI Lite control bus
s_axi_wdata	AXI Lite control bus
s_axi_wstrb	AXI Lite control bus
s_axi_wready	AXI Lite control bus
s_axi_bvalid	AXI Lite control bus
s_axi_bresp	AXI Lite control bus
s_axi_bready	AXI Lite control bus

s_axi_arvalid	AXI Lite control bus
s_axi_araddr	AXI Lite control bus
s_axi_arready	AXI Lite control bus
s_axi_arprot	AXI Lite control bus
s_axi_rvalid	AXI Lite control bus
s_axi_rready	AXI Lite control bus
s_axi_rresp	AXI Lite control bus
s_axi_rdata	AXI Lite control bus
adc_dma_irq	fmcomms2-3 ADC irq
dac_dma_irq	fmcomms2-3 DAC irq
delay_clk	fmcomms2-3 delay clock
rx_clk_in_p	fmcomms2-3 receive clock in
rx_clk_in_n	fmcomms2-3 receive clock in
rx_frame_in_p	fmcomms2-3 receive frame
rx_frame_in_n	fmcomms2-3 receive frame
rx_data_in_p	fmcomms2-3 receive lvds data
rx_data_in_n	fmcomms2-3 receive lvds data
tx_clk_out_p	fmcomms2-3 transmit clock
tx_clk_out_n	fmcomms2-3 transmit clock
tx_frame_out_p	fmcomms2-3 transmit frame
tx_frame_out_n	fmcomms2-3 transmit frame
tx_data_out_p	fmcomms2-3 transmit lvds data
tx_data_out_n	fmcomms2-3 transmit lvds data
enable	fmcomms2-3 enable
txnrx	fmcomms2-3 txnrx select
up_enable	fmcomms2-3 enable input
up_txnrx	fmcomms2-3 txnrx select input
tdd_sync_t	fmcomms2-3 TDD sync i/o
tdd_sync_i	fmcomms2-3 TDD sync i/o
tdd_sync_o	fmcomms2-3 TDD sync i/o
adc_m_dest_axi_awaddr	fmcomms2-3 ADC DMA
adc_m_dest_axi_awlen	fmcomms2-3 ADC DMA
adc_m_dest_axi_awsize	fmcomms2-3 ADC DMA
adc_m_dest_axi_awburst	fmcomms2-3 ADC DMA
adc_m_dest_axi_awprot	fmcomms2-3 ADC DMA
adc_m_dest_axi_awcache	fmcomms2-3 ADC DMA
adc_m_dest_axi_awvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_awready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wdata	fmcomms2-3 ADC DMA
adc_m_dest_axi_wstrb	fmcomms2-3 ADC DMA
adc_m_dest_axi_wready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wvalid	fmcomms2-3 ADC DMA

adc_m_dest_axi_wlast	fmcomms2-3 ADC DMA
adc_m_dest_axi_bvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_bresp	fmcomms2-3 ADC DMA
adc_m_dest_axi_bready	fmcomms2-3 ADC DMA
dac_m_src_axi_arready	fmcomms2-3 DAC DMA
dac_m_src_axi_arvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_araddr	fmcomms2-3 DAC DMA
dac_m_src_axi_arlen	fmcomms2-3 DAC DMA
dac_m_src_axi_arsize	fmcomms2-3 DAC DMA
dac_m_src_axi_arburst	fmcomms2-3 DAC DMA
dac_m_src_axi_arprot	fmcomms2-3 DAC DMA
dac_m_src_axi_arcache	fmcomms2-3 DAC DMA
dac_m_src_axi_rdata	fmcomms2-3 DAC DMA
dac_m_src_axi_rready	fmcomms2-3 DAC DMA
dac_m_src_axi_rvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_rresp	fmcomms2-3 DAC DMA
dac_m_src_axi_rlast	fmcomms2-3 DAC DMA

INSTANTIANTED MODULES

inst_ad9361_pl_wrapper

```
 ad9361_pl_wrapper #(

 FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),

 FPGA_FAMILY(FPGA_FAMILY),

 SPEED_GRADE(SPEED_GRADE),

 DEV_PACKAGE(DEV_PACKAGE),

 ADC_INIT_DELAY(ADC_INIT_DELAY),

 DAC_INIT_DELAY(DAC_INIT_DELAY),

 DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY),

 DMA_AXI_PROTOCOL_TO_PS(0),

 AXI_DMAC_ADC_ADDR(32'h9C400000),

 AXI_DMAC_DAC_ADDR(32'h9C420000),

 AXI_AD9361_ADDR(32'h99020000)
) inst_ad9361_pl_wrapper ( .axi_aclk(axi_aclk), .axi_aresetn(axi_aresetn),
```

Module instance of ad9361_pl_wrapper for the fmcomms2-3 device.

system_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl and ps for zcu102 board.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
3,
parameter
FPGA_FAMILY
 =
4,
parameter
SPEED_GRADE
```

```
 =
20,
parameter
DEV_PACKAGE
 =
3,
parameter
DELAY_REFCLK_FREQUENCY
 =
500,
parameter
ADC_INIT_DELAY
 =
11,
parameter
DAC_INIT_DELAY
 =
0
) ( input [12:0] gpio_bd_i, output [ 7:0] gpio_bd_o, input rx_clk_in_p, inpu
```

System wrapper for pl and ps for zcu102 board.

Parameters

FPGA_TECHNOLOGY parameter
Type of FPGA, such as Ultrascale, Arria 10. 3 is for ultrascale+.

FPGA_FAMILY parameter
Sub type of fpga, such as GX, SX, etc. 4 is for zynq.

SPEED_GRADE parameter
Number that corresponds to the ships recommeneded speed. 20 is for -2.

DEV_PACKAGE parameter
Specify a number that is equal to the manufactures package. 3 is for ff.

DELAY_REFCLK_FREQUENCY parameter
Reference clock frequency used for ad_data_in instances

ADC_INIT_DELAY parameter
Initial Delay for the ADC

DAC_INIT_DELAY parameter
Initial Delay for the DAC

Ports

gpio_bd_i	gpio
gpio_bd_o	gpio
rx_clk_in_p	fmcomms2-3 rx clk
rx_clk_in_n	fmcomms2-3 rx clk
rx_frame_in_p	fmcomms2-3 rx frame
rx_frame_in_n	fmcomms2-3 rx frame
rx_data_in_p	fmcomms2-3 rx data
rx_data_in_n	fmcomms2-3 rx data
tx_clk_out_p	fmcomms2-3 tx clk
tx_clk_out_n	fmcomms2-3 tx clk
tx_frame_out_p	fmcomms2-3 tx frame
tx_frame_out_n	fmcomms2-3 tx frame

tx_data_out_p	fmcomms2-3 tx data
tx_data_out_n	fmcomms2-3 tx data
txnrx	fmcomms2-3 txnrx
enable	fmcomms2-3 enable
gpio_resetb	fmcomms2-3 gpio
gpio_sync	fmcomms2-3 gpio
gpio_en_agc	fmcomms2-3 gpio
gpio_ctl	fmcomms2-3 gpio
gpio_status	fmcomms2-3 gpio
spi_csn	spi chip select
spi_clk	spi clk
spi_mosi	spi master out
spi_miso	spi master in

INSTANTIANTED MODULES

inst_system_pl_wrapper

```
system_pl_wrapper #(
                                                                          .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                          .
FPGA_FAMILY(FPGA_FAMILY),
                                                                          .
SPEED_GRADE(SPEED_GRADE),
                                                                          .
DEV_PACKAGE(DEV_PACKAGE),
                                                                          .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                          .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                          .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_system_pl_wrapper ( .axi_aclk(s_axi_clk), .axi_aresetn(s_axi_aresetn
```

Module instance of system_pl_wrapper for the fmcomms2-3 device.

inst_system_ps_wrapper

```
system_ps_wrapper inst_system_ps_wrapper (
                                                                          .
M_AXI_araddr(w_axi_araddr),
                                                                          .
M_AXI_arprot(w_axi_arprot),
                                                                          .
M_AXI_arready(w_axi_arready),
                                                                          .
M_AXI_arvalid(w_axi_arvalid),
                                                                          .
M_AXI_awaddr(w_axi_awaddr),
                                                                          .
```

```
M_AXI_awprot(w_axi_awprot),
M_AXI_awready(w_axi_awready),
M_AXI_awvalid(w_axi_awvalid),
M_AXI_bready(w_axi_bready),
M_AXI_bresp(w_axi_bresp),
M_AXI_bvalid(w_axi_bvalid),
M_AXI_rdata(w_axi_rdata),
M_AXI_rready(w_axi_rready),
M_AXI_rresp(w_axi_rresp),
M_AXI_rvalid(w_axi_rvalid),
M_AXI_wdata(w_axi_wdata),
M_AXI_wready(w_axi_wready),
M_AXI_wstrb(w_axi_wstrb),
M_AXI_wvalid(w_axi_wvalid),
S_AXI_HP0_arready(),
S_AXI_HP0_awready(adc_hp0_axi_awready),
S_AXI_HP0_bvalid(adc_hp0_axi_bvalid),
S_AXI_HP0_rlast(),
S_AXI_HP0_rvalid(),
S_AXI_HP0_wready(adc_hp0_axi_wready),
S_AXI_HP0_bresp(adc_hp0_axi_bresp),
S_AXI_HP0_rresp(),
S_AXI_HP0_bid(),
S_AXI_HP0_rid(),
S_AXI_HP0_rdata(),
S_AXI_HP0_ACLK(s_axi_clk),
S_AXI_HP0_arvalid(1'b0),
S_AXI_HP0_awvalid(adc_hp0_axi_awvalid),
S_AXI_HP0_bready(adc_hp0_axi_bready),
S_AXI_HP0_rready(1'b0),
S_AXI_HP0_wlast(adc_hp0_axi_wlast),
S_AXI_HP0_wvalid(adc_hp0_axi_wvalid),
S_AXI_HP0_arburst(2'b01),
S_AXI_HP0_arlock(0),
S_AXI_HP0_arsize(3'b011),
S_AXI_HP0_awburst(adc_hp0_axi_awburst),
S_AXI_HP0_awlock(0),
S_AXI_HP0_awsize(adc_hp0_axi_awsize),
S_AXI_HP0_arprot(0),
S_AXI_HP0_awprot(adc_hp0_axi_awprot),
S_AXI_HP0_araddr(0),
S_AXI_HP0_awaddr(adc_hp0_axi_awaddr),
S_AXI_HP0_arcache(4'b0011),
S_AXI_HP0_arlen(0),
S_AXI_HP0_arqos(0),
S_AXI_HP0_awcache(adc_hp0_axi_awcache),
S_AXI_HP0_awlen(adc_hp0_axi_awlen),
S_AXI_HP0_awqos(0),
S_AXI_HP0_arid(0),
S_AXI_HP0_awid(0),
S_AXI_HP0_wdata(adc_hp0_axi_wdata),
S_AXI_HP0_wstrb(adc_hp0_axi_wstrb),
S_AXI_HP0_aruser(1'b0),
S_AXI_HP0_awuser(1'b0),
S_AXI_HP1_arready(dac_hp1_axi_arready),
S_AXI_HP1_awready(),
S_AXI_HP1_bvalid(),
S_AXI_HP1_rlast(dac_hp1_axi_rlast),
S_AXI_HP1_rvalid(dac_hp1_axi_rvalid),
S_AXI_HP1_wready(),
S_AXI_HP1_bresp(),
S_AXI_HP1_rresp(dac_hp1_axi_rresp),
S_AXI_HP1_bid(),
S_AXI_HP1_rid(),
S_AXI_HP1_rdata(dac_hp1_axi_rdata),
S_AXI_HP1_ACLK(s_axi_clk),
S_AXI_HP1_arvalid(dac_hp1_axi_arvalid),
S_AXI_HP1_awvalid(1'b0),
S_AXI_HP1_bready(1'b0),
S_AXI_HP1_rready(dac_hp1_axi_rready),
S_AXI_HP1_wlast(1'b0),
S_AXI_HP1_wvalid(1'b0),
S_AXI_HP1_arburst(dac_hp1_axi_arburst),
S_AXI_HP1_arlock(0),
S_AXI_HP1_arsize(dac_hp1_axi_arsize),
S_AXI_HP1_awburst(2'b01),
S_AXI_HP1_awlock(0),
S_AXI_HP1_awsize(3'b011),
S_AXI_HP1_arprot(dac_hp1_axi_arprot),
S_AXI_HP1_awprot(0),
S_AXI_HP1_araddr(dac_hp1_axi_araddr),
S_AXI_HP1_awaddr(0),
S_AXI_HP1_arcache(dac_hp1_axi_arcache),
S_AXI_HP1_arlen(dac_hp1_axi_arlen),
S_AXI_HP1_arqos(0),
S_AXI_HP1_awcache(4'b0011),
S_AXI_HP1_awlen(0),
S_AXI_HP1_awqos(0),
S_AXI_HP1_arid(0),
S_AXI_HP1_awid(0),
S_AXI_HP1_wdata(0),
S_AXI_HP1_wstrb(~0),
S_AXI_HP1_aruser(1'b0),
S_AXI_HP1_awuser(1'b0),
gpio_i(gpio_i),
gpio_o(gpio_o),
gpio_t(),
peripheral_aresetn(s_axi_aresetn),
pl_clk0(s_axi_clk),
 pl_clk1(),
                                                                          .
 pl_clk2(s_delay_clk),
                                                                          .
 pl_ps_irq1({{2{1'b0}}, s_adc_dma_irq, s_dac_dma_irq, {4{1'b0}}}),
                                                                          .
 spi0_m_i(spi_miso),
                                                                          .
 spi0_m_o(spi_mosi),
                                                                          .
 spi0_mo_t(),
                                                                          .
 spi0_s_i(1'b0),
                                                                          .
 spi0_s_o(),
                                                                          .
 spi0_sclk_i(1'b0),
                                                                          .
 spi0_sclk_o(spi_clk),
                                                                          .
 spi0_sclk_t(),
                                                                          .
 spi0_so_t(),
                                                                          .
 spi0_ss1_o_n(),
                                                                          .
 spi0_ss2_o_n(),
                                                                          .
 spi0_ss_i_n(1'b1),
                                                                          .
 spi0_ss_n_t(),
                                                                          .
 spi0_ss_o_n(spi_csn),
                                                                          .
 spi1_m_i(1'b0),
                                                                          .
 spi1_m_o(),
                                                                          .
 spi1_mo_t(),
                                                                          .
 spi1_s_i(1'b0),
                                                                          .
 spi1_s_o(),
                                                                          .
 spi1_sclk_i(1'b0),
                                                                          .
 spi1_sclk_o(),
                                                                          .
 spi1_sclk_t(),
                                                                          .
 spi1_so_t(),
                                                                          .
 spi1_ss1_o_n(),
                                                                          .
 spi1_ss2_o_n(),
                                                                          .
 spi1_ss_i_n(1'b1),
                                                                          .
 spi1_ss_n_t(),
                                                                          .
 spi1_ss_o_n()
)
```

Module instance of inst_system_ps_wrapper for the built in CPU.

system_pl_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl only for zed board.

License MIT

system_pl_wrapper

```
module system_pl_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
0,
parameter
FPGA_FAMILY
 =
0,
parameter
SPEED_GRADE
```

```
 =
0,
parameter
DEV_PACKAGE
 =
0,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0,
parameter
DELAY_REFCLK_FREQUENCY
 =
200
) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_
```

System wrapper for pl only for zed board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 1 is for 7 series.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 20 is for -2.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 3 is for ff.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

axi_aclk	AXI Lite control bus
axi_aresetn	AXI Lite control bus
s_axi_awvalid	AXI Lite control bus
s_axi_awaddr	AXI Lite control bus
s_axi_awready	AXI Lite control bus
s_axi_awprot	AXI Lite control bus
s_axi_wvalid	AXI Lite control bus
s_axi_wdata	AXI Lite control bus
s_axi_wstrb	AXI Lite control bus
s_axi_wready	AXI Lite control bus
s_axi_bvalid	AXI Lite control bus
s_axi_bresp	AXI Lite control bus
s_axi_bready	AXI Lite control bus

s_axi_arvalid	AXI Lite control bus
s_axi_araddr	AXI Lite control bus
s_axi_arready	AXI Lite control bus
s_axi_arprot	AXI Lite control bus
s_axi_rvalid	AXI Lite control bus
s_axi_rready	AXI Lite control bus
s_axi_rresp	AXI Lite control bus
s_axi_rdata	AXI Lite control bus
adc_dma_irq	fmcomms2-3 ADC irq
dac_dma_irq	fmcomms2-3 DAC irq
delay_clk	fmcomms2-3 delay clock
rx_clk_in_p	fmcomms2-3 receive clock in
rx_clk_in_n	fmcomms2-3 receive clock in
rx_frame_in_p	fmcomms2-3 receive frame
rx_frame_in_n	fmcomms2-3 receive frame
rx_data_in_p	fmcomms2-3 receive lvds data
rx_data_in_n	fmcomms2-3 receive lvds data
tx_clk_out_p	fmcomms2-3 transmit clock
tx_clk_out_n	fmcomms2-3 transmit clock
tx_frame_out_p	fmcomms2-3 transmit frame
tx_frame_out_n	fmcomms2-3 transmit frame
tx_data_out_p	fmcomms2-3 transmit lvds data
tx_data_out_n	fmcomms2-3 transmit lvds data
enable	fmcomms2-3 enable
txnrx	fmcomms2-3 txnrx select
up_enable	fmcomms2-3 enable input
up_txnrx	fmcomms2-3 txnrx select input
tdd_sync_t	fmcomms2-3 TDD sync i/o
tdd_sync_i	fmcomms2-3 TDD sync i/o
tdd_sync_o	fmcomms2-3 TDD sync i/o
adc_m_dest_axi_awaddr	fmcomms2-3 ADC DMA
adc_m_dest_axi_awlen	fmcomms2-3 ADC DMA
adc_m_dest_axi_awsize	fmcomms2-3 ADC DMA
adc_m_dest_axi_awburst	fmcomms2-3 ADC DMA
adc_m_dest_axi_awprot	fmcomms2-3 ADC DMA
adc_m_dest_axi_awcache	fmcomms2-3 ADC DMA
adc_m_dest_axi_awvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_awready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wdata	fmcomms2-3 ADC DMA
adc_m_dest_axi_wstrb	fmcomms2-3 ADC DMA
adc_m_dest_axi_wready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wvalid	fmcomms2-3 ADC DMA

adc_m_dest_axi_wlast	fmcomms2-3 ADC DMA
adc_m_dest_axi_bvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_bresp	fmcomms2-3 ADC DMA
adc_m_dest_axi_bready	fmcomms2-3 ADC DMA
dac_m_src_axi_arready	fmcomms2-3 DAC DMA
dac_m_src_axi_arvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_araddr	fmcomms2-3 DAC DMA
dac_m_src_axi_arlen	fmcomms2-3 DAC DMA
dac_m_src_axi_arsize	fmcomms2-3 DAC DMA
dac_m_src_axi_arburst	fmcomms2-3 DAC DMA
dac_m_src_axi_arprot	fmcomms2-3 DAC DMA
dac_m_src_axi_arcache	fmcomms2-3 DAC DMA
dac_m_src_axi_rdata	fmcomms2-3 DAC DMA
dac_m_src_axi_rready	fmcomms2-3 DAC DMA
dac_m_src_axi_rvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_rresp	fmcomms2-3 DAC DMA
dac_m_src_axi_rlast	fmcomms2-3 DAC DMA
iic_sda_fmc	i2c for fmc
iic_scl_fmc	i2c for fmc
iic2intc_irpt	i2c for fmc

INSTANTIANTED MODULES

iic_sda_iobuf

```
ad_iobuf #(
                                                                    .
DATA_WIDTH(1)
) iic_sda_iobuf ( .dio_t (sda_t), .dio_i (sda_o), .dio_o (sda_i), .dio_p (
```

Tristate i2c sda

iic_scl_iobuf

```
ad_iobuf #(
                                                                    .
DATA_WIDTH(1)
) iic_scl_iobuf ( .dio_t (scl_t), .dio_i (scl_o), .dio_o (scl_i), .dio_p (
```

Tristate i2c scl

inst_ad9361_pl_wrapper

```
ad9361_pl_wrapper #(
                                                                       .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                       .
FPGA_FAMILY(FPGA_FAMILY),
                                                                       .
SPEED_GRADE(SPEED_GRADE),
                                                                       .
DEV_PACKAGE(DEV_PACKAGE),
                                                                       .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                       .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                       .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_ad9361_pl_wrapper ( .axi_aclk(axi_aclk), .axi_aresetn(axi_aresetn),
```

Module instance of ad9361_pl_wrapper for the fmcomms2-3 device.

inst_axi_crossbar_pl

```
axi_crossbar_pl inst_axi_crossbar_pl (
                                                                       .
aclk(axi_aclk),
                                                                       .
aresetn(axi_aresetn),
                                                                       .
s_axi_awaddr(s_axi_awaddr),
                                                                       .
s_axi_awprot(s_axi_awprot),
                                                                       .
s_axi_awvalid(s_axi_awvalid),
                                                                       .
s_axi_awready(s_axi_awready),
                                                                       .
s_axi_wdata(s_axi_wdata),
                                                                       .
s_axi_wstrb(s_axi_wstrb),
                                                                       .
s_axi_wvalid(s_axi_wvalid),
                                                                       .
s_axi_wready(s_axi_wready),
                                                                       .
s_axi_bresp(s_axi_bresp),
                                                                       .
s_axi_bvalid(s_axi_bvalid),
                                                                       .
s_axi_bready(s_axi_bready),
                                                                       .
s_axi_araddr(s_axi_araddr),
                                                                       .
s_axi_arprot(s_axi_arprot),
                                                                       .
s_axi_arvalid(s_axi_arvalid),
                                                                       .
s_axi_arready(s_axi_arready),
                                                                       .
s_axi_rdata(s_axi_rdata),
                                                                       .
s_axi_rresp(s_axi_rresp),
                                                                       .
s_axi_rvalid(s_axi_rvalid),
                                                                       .
s_axi_rready(s_axi_rready),
.m_axi_awaddr({iic_fmc_axi_awaddr, connect_axi_awaddr}),
.m_axi_awprot({iic_fmc_axi_awprot, connect_axi_awprot}),
.m_axi_awvalid({iic_fmc_axi_awvalid, connect_axi_awvalid}),
.m_axi_awready({iic_fmc_axi_awready, connect_axi_awready}),
.m_axi_wdata({iic_fmc_axi_wdata, connect_axi_wdata}),
.m_axi_wstrb({iic_fmc_axi_wstrb, connect_axi_wstrb}),
.m_axi_wvalid({iic_fmc_axi_wvalid, connect_axi_wvalid}),
.m_axi_wready({iic_fmc_axi_wready, connect_axi_wready}),
.m_axi_bresp({iic_fmc_axi_bresp, connect_axi_bresp}),
.m_axi_bvalid({iic_fmc_axi_bvalid, connect_axi_bvalid}),
.m_axi_bready({iic_fmc_axi_bready, connect_axi_bready}),
.m_axi_araddr({iic_fmc_axi_araddr, connect_axi_araddr}),
.m_axi_arprot({iic_fmc_axi_arprot, connect_axi_arprot}),
.m_axi_arvalid({iic_fmc_axi_arvalid, connect_axi_arvalid}),
.m_axi_arready({iic_fmc_axi_arready, connect_axi_arready}),
.m_axi_rdata({iic_fmc_axi_rdata, connect_axi_rdata}),
.m_axi_rresp({iic_fmc_axi_rresp, connect_axi_rresp}),
.m_axi_rvalid({iic_fmc_axi_rvalid, connect_axi_rvalid}),
.m_axi_rready({iic_fmc_axi_rready, connect_axi_rready})
)
```

Module instance of axi_crossbar_pl for the fmcomms2-3 device.

inst_axi_iic_fmc

```
axi_iic_fmc inst_axi_iic_fmc (
.s_axi_aclk(axi_aclk),
.s_axi_aresetn(axi_aresetn),
.iic2intc_irpt(iic2intc_irpt),
.s_axi_awaddr(iic_fmc_axi_awaddr[8:0]),
.s_axi_awvalid(iic_fmc_axi_awvalid),
.s_axi_awready(iic_fmc_axi_awready),
.s_axi_wdata(iic_fmc_axi_wdata),
.s_axi_wstrb(iic_fmc_axi_wstrb),
.s_axi_wvalid(iic_fmc_axi_wvalid),
                                                                          .
 s_axi_wready(iic_fmc_axi_wready),
                                                                          .
 s_axi_bresp(iic_fmc_axi_bresp),
                                                                          .
 s_axi_bvalid(iic_fmc_axi_bvalid),
                                                                          .
 s_axi_bready(iic_fmc_axi_bready),
                                                                          .
 s_axi_araddr(iic_fmc_axi_araddr[8:0]),
                                                                          .
 s_axi_arvalid(iic_fmc_axi_arvalid),
                                                                          .
 s_axi_arready(iic_fmc_axi_arready),
                                                                          .
 s_axi_rdata(iic_fmc_axi_rdata),
                                                                          .
 s_axi_rresp(iic_fmc_axi_rresp),
                                                                          .
 s_axi_rvalid(iic_fmc_axi_rvalid),
                                                                          .
 s_axi_rready(iic_fmc_axi_rready),
                                                                          .
 sda_i(sda_i),
                                                                          .
 sda_o(sda_o),
                                                                          .
 sda_t(sda_t),
                                                                          .
 scl_i(scl_i),
                                                                          .
 scl_o(scl_o),
                                                                          .
 scl_t(scl_t),
                                                                          .
 gpo()
)
```

Module instance of axi_iic_fmc for the fmcomms2-3 device.

system_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl and ps for zed board.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
1,
parameter
FPGA_FAMILY
 =
4,
parameter
SPEED_GRADE
```

```
 =
10,
parameter
DEV_PACKAGE
 =
14,
parameter
DELAY_REFCLK_FREQUENCY
 =
200,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0
) ( inout [14:0] ddr_addr, inout [ 2:0] ddr_ba, inout ddr_cas_n, inout ddr_
```

System wrapper for pl and ps for zed board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 1 is for 7 series.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 10 is for -1.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 14 is for cl.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

ddr_addr	DDR interface
ddr_ba	DDR interface
ddr_cas_n	DDR interface
ddr_ck_n	DDR interface
ddr_ck_p	DDR interface
ddr_cke	DDR interface
ddr_cs_n	DDR interface
ddr_dm	DDR interface
ddr_dq	DDR interface
ddr_dqs_n	DDR interface
ddr_dqs_p	DDR interface
ddr_odt	DDR interface
ddr_ras_n	DDR interface

ddr_reset_n	DDR interface
ddr_we_n	DDR interface
fixed_io_ddr_vrn	DDR interface
fixed_io_ddr_vrp	DDR interface
fixed_io_mio	ps mio
fixed_io_ps_clk	ps clk
fixed_io_ps_porb	ps por
fixed_io_ps_srstb	ps rst
iic_scl_fmc	fmcomms2-3 i2c
iic_sda_fmc	fmcomms2-3 i2c
gpio_bd	gpio
rx_clk_in_p	fmcomms2-3 rx clk
rx_clk_in_n	fmcomms2-3 rx clk
rx_frame_in_p	fmcomms2-3 rx frame
rx_frame_in_n	fmcomms2-3 rx frame
rx_data_in_p	fmcomms2-3 rx data
rx_data_in_n	fmcomms2-3 rx data
tx_clk_out_p	fmcomms2-3 tx clk
tx_clk_out_n	fmcomms2-3 tx clk
tx_frame_out_p	fmcomms2-3 tx frame
tx_frame_out_n	fmcomms2-3 tx frame
tx_data_out_p	fmcomms2-3 tx data
tx_data_out_n	fmcomms2-3 tx data
txnrx	fmcomms2-3 txnrx
enable	fmcomms2-3 enable
gpio_muxout_tx	fmcomms2-3 gpio
gpio_muxout_rx	fmcomms2-3 gpio
gpio_resetb	fmcomms2-3 gpio
gpio_sync	fmcomms2-3 gpio
gpio_en_agc	fmcomms2-3 gpio
gpio_ctl	fmcomms2-3 gpio
gpio_status	fmcomms2-3 gpio
spi_csn	spi chip select
spi_clk	spi clk
spi_mosi	spi master out
spi_miso	spi master in
spi_udc_csn_tx	spi udc chip select tx
spi_udc_csn_rx	spi udc chip select rx
spi_udc_sclk	spi udc clock
spi_udc_data	spi udc data

INSTANTIANTED MODULES

inst_system_pl_wrapper

```
system_pl_wrapper #(
                                                                        .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                        .
FPGA_FAMILY(FPGA_FAMILY),
                                                                        .
SPEED_GRADE(SPEED_GRADE),
                                                                        .
DEV_PACKAGE(DEV_PACKAGE),
                                                                        .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                        .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                        .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_system_pl_wrapper ( .axi_aclk(s_axi_clk), .axi_aresetn(s_axi_areset
```

Module instance of system_pl_wrapper for the fmcomms2-3 device.

inst_system_ps_wrapper

```
system_ps_wrapper inst_system_ps_wrapper (
                                                                        .
GPIO_I(gpio_i),
                                                                        .
GPIO_O(gpio_o),
                                                                        .
GPIO_T(gpio_t),
                                                                        .
SPI0_SCLK_I(1'b0),
                                                                        .
SPI0_SCLK_O(spi_clk),
                                                                        .
SPI0_MOSI_I(1'b0),
                                                                        .
SPI0_MOSI_O(spi_mosi),
                                                                        .
SPI0_MISO_I(spi_miso),
                                                                        .
SPI0_SS_I(1'b1),
                                                                        .
SPI0_SS_O(spi_csn),
                                                                        .
SPI1_SCLK_I(1'b0),
                                                                        .
SPI1_SCLK_O(spi_udc_sclk),
                                                                        .
SPI1_MOSI_I(spi_udc_data),
                                                                        .
SPI1_MOSI_O(spi_udc_data),
                                                                        .
SPI1_MISO_I(1'b0),
                                                                        .
SPI1_SS_I(1'b1),
                                                                        .
SPI1_SS_O(spi_udc_csn_tx),
SPI1_SS1_O(spi_udc_csn_rx),
SPI1_SS2_O(),
USB0_vbus_pwrfault(~otg_vbusoc),
M_AXI_araddr(w_axi_araddr),
M_AXI_arprot(w_axi_arprot),
M_AXI_arready(w_axi_arready),
M_AXI_arvalid(w_axi_arvalid),
M_AXI_awaddr(w_axi_awaddr),
M_AXI_awprot(w_axi_awprot),
M_AXI_awready(w_axi_awready),
M_AXI_awvalid(w_axi_awvalid),
M_AXI_bready(w_axi_bready),
M_AXI_bresp(w_axi_bresp),
M_AXI_bvalid(w_axi_bvalid),
M_AXI_rdata(w_axi_rdata),
M_AXI_rready(w_axi_rready),
M_AXI_rresp(w_axi_rresp),
M_AXI_rvalid(w_axi_rvalid),
M_AXI_wdata(w_axi_wdata),
M_AXI_wready(w_axi_wready),
M_AXI_wstrb(w_axi_wstrb),
M_AXI_wvalid(w_axi_wvalid),
S_AXI_HP0_arready(),
S_AXI_HP0_awready(adc_hp0_axi_awready),
S_AXI_HP0_bvalid(adc_hp0_axi_bvalid),
S_AXI_HP0_rlast(),
S_AXI_HP0_rvalid(),
S_AXI_HP0_wready(adc_hp0_axi_wready),
S_AXI_HP0_bresp(adc_hp0_axi_bresp),
S_AXI_HP0_rresp(),
S_AXI_HP0_bid(),
S_AXI_HP0_rid(),
S_AXI_HP0_rdata(),
S_AXI_HP0_ACLK(s_axi_clk),
S_AXI_HP0_arvalid(1'b0),
S_AXI_HP0_awvalid(adc_hp0_axi_awvalid),
S_AXI_HP0_bready(adc_hp0_axi_bready),
S_AXI_HP0_rready(1'b0),
S_AXI_HP0_wlast(adc_hp0_axi_wlast),
S_AXI_HP0_wvalid(adc_hp0_axi_wvalid),
S_AXI_HP0_arburst(2'b01),
S_AXI_HP0_arlock(0),
S_AXI_HP0_arsize(3'b011),
S_AXI_HP0_awburst(adc_hp0_axi_awburst),
S_AXI_HP0_awlock(0),
S_AXI_HP0_awsize(adc_hp0_axi_awsize),
S_AXI_HP0_arprot(0),
S_AXI_HP0_awprot(adc_hp0_axi_awprot),
S_AXI_HP0_araddr(0),
S_AXI_HP0_awaddr(adc_hp0_axi_awaddr),
S_AXI_HP0_arcache(4'b0011),
S_AXI_HP0_arlen(0),
S_AXI_HP0_arqos(0),
S_AXI_HP0_awcache(adc_hp0_axi_awcache),
S_AXI_HP0_awlen(adc_hp0_axi_awlen),
S_AXI_HP0_awqos(0),
S_AXI_HP0_arid(0),
S_AXI_HP0_awid(0),
S_AXI_HP0_wid(0),
S_AXI_HP0_wdata(adc_hp0_axi_wdata),
S_AXI_HP0_wstrb(adc_hp0_axi_wstrb),
S_AXI_HP1_arready(dac_hp1_axi_arready),
S_AXI_HP1_awready(),
S_AXI_HP1_bvalid(),
S_AXI_HP1_rlast(dac_hp1_axi_rlast),
S_AXI_HP1_rvalid(dac_hp1_axi_rvalid),
S_AXI_HP1_wready(),

S_AXI_HP1_bresp(),

S_AXI_HP1_rresp(dac_hp1_axi_rresp),

S_AXI_HP1_bid(),

S_AXI_HP1_rid(),

S_AXI_HP1_rdata(dac_hp1_axi_rdata),

S_AXI_HP1_ACLK(s_axi_clk),

S_AXI_HP1_arvalid(dac_hp1_axi_arvalid),

S_AXI_HP1_awvalid(1'b0),

S_AXI_HP1_bready(1'b0),

S_AXI_HP1_rready(dac_hp1_axi_rready),

S_AXI_HP1_wlast(1'b0),

S_AXI_HP1_wvalid(1'b0),

S_AXI_HP1_arburst(dac_hp1_axi_arburst),

S_AXI_HP1_arlock(0),

S_AXI_HP1_arsize(dac_hp1_axi_arsize),

S_AXI_HP1_awburst(2'b01),

S_AXI_HP1_awlock(0),

S_AXI_HP1_awsize(3'b011),

S_AXI_HP1_arprot(dac_hp1_axi_arprot),

S_AXI_HP1_awprot(0),

S_AXI_HP1_araddr(dac_hp1_axi_araddr),

S_AXI_HP1_awaddr(0),

S_AXI_HP1_arcache(dac_hp1_axi_arcache),

S_AXI_HP1_arlen(dac_hp1_axi_arlen),

S_AXI_HP1_arqos(0),

S_AXI_HP1_awcache(4'b0011),

S_AXI_HP1_awlen(0),

S_AXI_HP1_awqos(0),

S_AXI_HP1_arid(0),

S_AXI_HP1_awid(0),

S_AXI_HP1_wid(0),

S_AXI_HP1_wdata(0),
 S_AXI_HP1_wstrb(~0),

 IRQ_F2P({{2{1'b0}}, s_adc_dma_irq, s_dac_dma_irq, s_iic2intc_irpt, {11{1'b0

 FCLK_CLK0(s_axi_clk),

 FCLK_CLK1(s_delay_clk),

 FIXED_IO_mio(fixed_io_mio),

 DDR_cas_n(ddr_cas_n),

 DDR_cke(ddr_cke),

 DDR_ck_n(ddr_ck_n),

 DDR_ck_p(ddr_ck_p),

 DDR_cs_n(ddr_cs_n),

 DDR_reset_n(ddr_reset_n),

 DDR_odt(ddr_odt),

 DDR_ras_n(ddr_ras_n),

 DDR_we_n(ddr_we_n),

 DDR_ba(ddr_ba),

 DDR_addr(ddr_addr),

 FIXED_IO_ddr_vrn(fixed_io_ddr_vrn),

 FIXED_IO_ddr_vrp(fixed_io_ddr_vrp),

 DDR_dm(ddr_dm),

 DDR_dq(ddr_dq),

 DDR_dqs_n(ddr_dqs_n),

 DDR_dqs_p(ddr_dqs_p),

 FIXED_IO_ps_srstb(fixed_io_ps_srstb),

 FIXED_IO_ps_clk(fixed_io_ps_clk),

 FIXED_IO_ps_porb(fixed_io_ps_porb),

 peripheral_aresetn(s_axi_aresetn)
)
```

Module instance of inst_system_ps_wrapper for the built in CPU.

system_pl_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl only for arria10soc board.

License MIT

system_pl_wrapper

```
module system_pl_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
0,
parameter
FPGA_FAMILY
 =
0,
parameter
SPEED_GRADE
```

```
 =
0,
parameter
DEV_PACKAGE
 =
0,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0,
parameter
DELAY_REFCLK_FREQUENCY
 =
200
) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_
```

System wrapper for pl only for arria10soc board.

Parameters

FPGA_TECHNOLOGY
parameter
Type of FPGA, such as Ultrascale, Arria 10. 103 is for Arria 10.

FPGA_FAMILY
parameter
Sub type of fpga, such as GX, SX, etc. 1 is for SX

SPEED_GRADE
parameter
Number that corresponds to the ships recommeneded speed. 2 is for 2.

DEV_PACKAGE
parameter
Specify a number that is equal to the manufactures package. 3 is for FBGA.

ADC_INIT_DELAY
parameter
Initial Delay for the ADC

DAC_INIT_DELAY
parameter
Initial Delay for the DAC

DELAY_REFCLK_FREQUENCY
parameter
Reference clock frequency used for ad_data_in instances

Ports

axi_aclk	AXI Lite control bus
axi_aresetn	AXI Lite control bus
s_axi_awvalid	AXI Lite control bus
s_axi_awaddr	AXI Lite control bus
s_axi_awready	AXI Lite control bus
s_axi_awprot	AXI Lite control bus
s_axi_wvalid	AXI Lite control bus
s_axi_wdata	AXI Lite control bus
s_axi_wstrb	AXI Lite control bus
s_axi_wready	AXI Lite control bus
s_axi_bvalid	AXI Lite control bus
s_axi_bresp	AXI Lite control bus
s_axi_bready	AXI Lite control bus

s_axi_arvalid	AXI Lite control bus
s_axi_araddr	AXI Lite control bus
s_axi_arready	AXI Lite control bus
s_axi_arprot	AXI Lite control bus
s_axi_rvalid	AXI Lite control bus
s_axi_rready	AXI Lite control bus
s_axi_rresp	AXI Lite control bus
s_axi_rdata	AXI Lite control bus
adc_dma_irq	fmcomms2-3 ADC irq
dac_dma_irq	fmcomms2-3 DAC irq
delay_clk	fmcomms2-3 delay clock
rx_clk_in_p	fmcomms2-3 receive clock in
rx_clk_in_n	fmcomms2-3 receive clock in
rx_frame_in_p	fmcomms2-3 receive frame
rx_frame_in_n	fmcomms2-3 receive frame
rx_data_in_p	fmcomms2-3 receive lvds data
rx_data_in_n	fmcomms2-3 receive lvds data
tx_clk_out_p	fmcomms2-3 transmit clock
tx_clk_out_n	fmcomms2-3 transmit clock
tx_frame_out_p	fmcomms2-3 transmit frame
tx_frame_out_n	fmcomms2-3 transmit frame
tx_data_out_p	fmcomms2-3 transmit lvds data
tx_data_out_n	fmcomms2-3 transmit lvds data
enable	fmcomms2-3 enable
txnrx	fmcomms2-3 txnrx select
up_enable	fmcomms2-3 enable input
up_txnrx	fmcomms2-3 txnrx select input
tdd_sync_t	fmcomms2-3 TDD sync i/o
tdd_sync_i	fmcomms2-3 TDD sync i/o
tdd_sync_o	fmcomms2-3 TDD sync i/o
adc_m_dest_axi_awaddr	fmcomms2-3 ADC DMA
adc_m_dest_axi_awlen	fmcomms2-3 ADC DMA
adc_m_dest_axi_awsize	fmcomms2-3 ADC DMA
adc_m_dest_axi_awburst	fmcomms2-3 ADC DMA
adc_m_dest_axi_awprot	fmcomms2-3 ADC DMA
adc_m_dest_axi_awcache	fmcomms2-3 ADC DMA
adc_m_dest_axi_awvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_awready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wdata	fmcomms2-3 ADC DMA
adc_m_dest_axi_wstrb	fmcomms2-3 ADC DMA
adc_m_dest_axi_wready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wvalid	fmcomms2-3 ADC DMA

adc_m_dest_axi_wlast	fmcomms2-3 ADC DMA
adc_m_dest_axi_bvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_bresp	fmcomms2-3 ADC DMA
adc_m_dest_axi_bready	fmcomms2-3 ADC DMA
dac_m_src_axi_arready	fmcomms2-3 DAC DMA
dac_m_src_axi_arvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_araddr	fmcomms2-3 DAC DMA
dac_m_src_axi_arlen	fmcomms2-3 DAC DMA
dac_m_src_axi_arsize	fmcomms2-3 DAC DMA
dac_m_src_axi_arburst	fmcomms2-3 DAC DMA
dac_m_src_axi_arprot	fmcomms2-3 DAC DMA
dac_m_src_axi_arcache	fmcomms2-3 DAC DMA
dac_m_src_axi_rdata	fmcomms2-3 DAC DMA
dac_m_src_axi_rready	fmcomms2-3 DAC DMA
dac_m_src_axi_rvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_rresp	fmcomms2-3 DAC DMA
dac_m_src_axi_rlast	fmcomms2-3 DAC DMA

INSTANTIANTED MODULES

inst_ad9361_pl_wrapper

```
 ad9361_pl_wrapper #(
                                                                    .
 FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                    .
 FPGA_FAMILY(FPGA_FAMILY),
                                                                    .
 SPEED_GRADE(SPEED_GRADE),
                                                                    .
 DEV_PACKAGE(DEV_PACKAGE),
                                                                    .
 ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                    .
 DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                    .
 DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY),
                                                                    .
 AXI_DMAC_ADC_ADDR(32'h00010000),
                                                                    .
 AXI_DMAC_DAC_ADDR(32'h00014000),
                                                                    .
 AXI_AD9361_ADDR(32'h00000000)
) inst_ad9361_pl_wrapper ( .axi_aclk(axi_aclk), .axi_aresetn(axi_aresetn),
```

Module instance of ad9361_pl_wrapper for the fmcomms2-3 device.

system_wrapper.v

AUTHORS

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DATES

2023/12/17

INFORMATION

Brief

System wrapper for pl and ps for arria10soc board.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
103,
parameter
FPGA_FAMILY
 =
1,
parameter
SPEED_GRADE
```

```
 =
2,
parameter
DEV_PACKAGE
 =
3,
parameter
DELAY_REFCLK_FREQUENCY
 =
200,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0
) ( input sys_clk, input sys_resetn, input hps_ddr_ref_clk, output [ 0:0] hp
```

System wrapper for pl and ps for arria10soc board.

Parameters

FPGA_TECHNOLOGY
parameter
Type of FPGA, such as Ultrascale, Arria 10. 103 is for Arria 10.

FPGA_FAMILY
parameter
Sub type of fpga, such as GX, SX, etc. 1 is for SX

SPEED_GRADE
parameter
Number that corresponds to the ships recommeneded speed. 2 is for 2.

DEV_PACKAGE
parameter
Specify a number that is equal to the manufactures package. 3 is for FBGA.

DELAY_REFCLK_FREQUENCY
parameter
Reference clock frequency used for ad_data_in instances

ADC_INIT_DELAY
parameter
Initial Delay for the ADC

DAC_INIT_DELAY
parameter
Initial Delay for the DAC

Ports

sys_clk	Input clock for all clocks
sys_resetn	Input reset for all resets
hps_ddr_ref_clk	DDR port
hps_ddr_clk_p	DDR port
hps_ddr_clk_n	DDR port
hps_ddr_a	DDR port
hps_ddr_ba	DDR port
hps_ddr_bg	DDR port
hps_ddr_cke	DDR port
hps_ddr_cs_n	DDR port
hps_ddr_odt	DDR port
hps_ddr_reset_n	DDR port
hps_ddr_act_n	DDR port

hps_ddr_par	DDR port
hps_ddr_alert_n	DDR port
hps_ddr_dqs_p	DDR port
hps_ddr_dqs_n	DDR port
hps_ddr_dq	DDR port
hps_ddr_dbi_n	DDR port
hps_ddr_rzq	DDR port
hps_eth_rxclk	Ethernet Device
hps_eth_rxctl	Ethernet Device
hps_eth_rxd	Ethernet Device
hps_eth_txclk	Ethernet Device
hps_eth_txctl	Ethernet Device
hps_eth_txd	Ethernet Device
hps_eth_mdc	Ethernet Device
hps_eth_mdio	Ethernet Device
hps_sdio_clk	SD card interface
hps_sdio_cmd	SD card interface
hps_sdio_d	SD card interface
hps_usb_clk	USB interface
hps_usb_dir	USB interface
hps_usb_nxt	USB interface
hps_usb_stp	USB interface
hps_usb_d	USB interface
hps_uart_rx	UART interface
hps_uart_tx	UART interface
hps_i2c_sda	i2c interface
hps_i2c_scl	i2c interface
hps_gpio	GPIO interface
gpio_bd_i	fmcomms2-3 gpio
gpio_bd_o	fmcomms2-3 gpio
rx_clk_in	fmcomms2-3 receive clock in
rx_frame_in_p	fmcomms2-3 receive frame
rx_frame_in_n	fmcomms2-3 receive frame
rx_data_in_p	fmcomms2-3 receive lvds data
rx_data_in_n	fmcomms2-3 receive lvds data
tx_clk_out_p	fmcomms2-3 transmit clock
tx_clk_out_n	fmcomms2-3 transmit clock
tx_frame_out_p	fmcomms2-3 transmit frame
tx_frame_out_n	fmcomms2-3 transmit frame
tx_data_out_p	fmcomms2-3 transmit lvds data
tx_data_out_n	fmcomms2-3 transmit lvds data
enable	fmcomms2-3 enable

txnrx	fmcomms2-3 txnrx select
gpio_resetb	fmcomms2-3 gpio reset
gpio_sync	fmcomms2-3 gpio sync
gpio_en_agc	fmcomms2-3 gpio enable agc
gpio_ctl	fmcomms2-3 control
gpio_status	fmcomms2-3 status
spi_csn	fmcomms2-3 spi select
spi_clk	fmcomms2-3 spi clk
spi_mosi	fmcomms2-3 spi output
spi_miso	fmcomms2-3 spi input

INSTANTIANTED MODULES

inst_system_pl_wrapper

```
system_pl_wrapper #(
                                                                        .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                        .
FPGA_FAMILY(FPGA_FAMILY),
                                                                        .
SPEED_GRADE(SPEED_GRADE),
                                                                        .
DEV_PACKAGE(DEV_PACKAGE),
                                                                        .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                        .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                        .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_system_pl_wrapper ( .axi_aclk(s_axi_clk), .axi_aresetn(s_axi_areset
```

Module instance of system_pl_wrapper for the fmcomms2-3 device.

inst_system_ps_wrapper

```
system_ps_wrapper inst_system_ps_wrapper (
                                                                        .
s_axi_clk_clk(s_axi_clk),
                                                                        .
s_axi_aresetn_reset_n(s_axi_aresetn),
                                                                        .
m_axi_awaddr(w_axi_awaddr),
                                                                        .
m_axi_awprot(w_axi_awprot),
                                                                        .
m_axi_awvalid(w_axi_awvalid),
                                                                        .
m_axi_awready(w_axi_awready),
                                                                        .
m_axi_wdata(w_axi_wdata),
                                                                        .
m_axi_wstrb(w_axi_wstrb),
                                                                          .
m_axi_wvalid(w_axi_wvalid),
                                                                          .
m_axi_wready(w_axi_wready),
                                                                          .
m_axi_bresp(w_axi_bresp),
                                                                          .
m_axi_bvalid(w_axi_bvalid),
                                                                          .
m_axi_bready(w_axi_bready),
                                                                          .
m_axi_araddr(w_axi_araddr),
                                                                          .
m_axi_arprot(w_axi_arprot),
                                                                          .
m_axi_arvalid(w_axi_arvalid),
                                                                          .
m_axi_arready(w_axi_arready),
                                                                          .
m_axi_rdata(w_axi_rdata),
                                                                          .
m_axi_rresp(w_axi_rresp),
                                                                          .
m_axi_rvalid(w_axi_rvalid),
                                                                          .
m_axi_rready(w_axi_rready),
                                                                          .
sys_delay_clk_clk(s_delay_clk),
                                                                          .
sys_clk_clk(sys_clk),
                                                                          .
sys_gpio_bd_in_port(gpio_i[31:0]),
                                                                          .
sys_gpio_bd_out_port(gpio_o[31:0]),
                                                                          .
sys_gpio_in_export(gpio_i[63:32]),
                                                                          .
sys_gpio_out_export(gpio_o[63:32]),
                                                                          .
sys_hps_rstn_reset_n
                                                                          (
sys_resetn),
                                                                          .
sys_rstn_reset_n
                                                                          (
sys_resetn_s),
                                                                          .
sys_hps_io_hps_io_phery_emac0_TX_CLK
                                                                          (
hps_eth_txclk),
                                                                          .
sys_hps_io_hps_io_phery_emac0_TXD0
                                                                          (
hps_eth_txd[0]),
                                                                          .
sys_hps_io_hps_io_phery_emac0_TXD1
                                                                          (
hps_eth_txd[1]),
                                                                          .
sys_hps_io_hps_io_phery_emac0_TXD2
                                                                          (
hps_eth_txd[2]),
                                                                          .
sys_hps_io_hps_io_phery_emac0_TXD3
                                                                          (
hps_eth_txd[3]),
                                                                         .
sys_hps_io_hps_io_phery_emac0_RX_CTL
                                                                         (
hps_eth_rxctl),
                                                                         .
sys_hps_io_hps_io_phery_emac0_TX_CTL
                                                                         (
hps_eth_txctl),
                                                                         .
sys_hps_io_hps_io_phery_emac0_RX_CLK
                                                                         (
hps_eth_rxclk),
                                                                         .
sys_hps_io_hps_io_phery_emac0_RXD0
                                                                         (
hps_eth_rxd[0]),
                                                                         .
sys_hps_io_hps_io_phery_emac0_RXD1
                                                                         (
hps_eth_rxd[1]),
                                                                         .
sys_hps_io_hps_io_phery_emac0_RXD2
                                                                         (
hps_eth_rxd[2]),
                                                                         .
sys_hps_io_hps_io_phery_emac0_RXD3
                                                                         (
hps_eth_rxd[3]),
                                                                         .
sys_hps_io_hps_io_phery_emac0_MDIO
                                                                         (
hps_eth_mdio),
                                                                         .
sys_hps_io_hps_io_phery_emac0_MDC
                                                                         (
hps_eth_mdc),
                                                                         .
sys_hps_io_hps_io_phery_sdmmc_CMD
                                                                         (
hps_sdio_cmd),
                                                                         .
sys_hps_io_hps_io_phery_sdmmc_D0
                                                                         (
hps_sdio_d[0]),
                                                                         .
sys_hps_io_hps_io_phery_sdmmc_D1
                                                                         (
hps_sdio_d[1]),
                                                                         .
sys_hps_io_hps_io_phery_sdmmc_D2
                                                                         (
hps_sdio_d[2]),
                                                                         .
sys_hps_io_hps_io_phery_sdmmc_D3
                                                                         (
hps_sdio_d[3]),
                                                                         .
sys_hps_io_hps_io_phery_sdmmc_D4
                                                                         (
hps_sdio_d[4]),
                                                                         .
sys_hps_io_hps_io_phery_sdmmc_D5
                                                                         (
hps_sdio_d[5]),
                                                                         .
sys_hps_io_hps_io_phery_sdmmc_D6
```

```
(
hps_sdio_d[6]),
.
sys_hps_io_hps_io_phery_sdmmc_D7
(
hps_sdio_d[7]),
.
sys_hps_io_hps_io_phery_sdmmc_CCLK
(
hps_sdio_clk),
.
sys_hps_io_hps_io_phery_usb0_DATA0
(
hps_usb_d[0]),
.
sys_hps_io_hps_io_phery_usb0_DATA1
(
hps_usb_d[1]),
.
sys_hps_io_hps_io_phery_usb0_DATA2
(
hps_usb_d[2]),
.
sys_hps_io_hps_io_phery_usb0_DATA3
(
hps_usb_d[3]),
.
sys_hps_io_hps_io_phery_usb0_DATA4
(
hps_usb_d[4]),
.
sys_hps_io_hps_io_phery_usb0_DATA5
(
hps_usb_d[5]),
.
sys_hps_io_hps_io_phery_usb0_DATA6
(
hps_usb_d[6]),
.
sys_hps_io_hps_io_phery_usb0_DATA7
(
hps_usb_d[7]),
.
sys_hps_io_hps_io_phery_usb0_CLK
(
hps_usb_clk),
.
sys_hps_io_hps_io_phery_usb0_STP
(
hps_usb_stp),
.
sys_hps_io_hps_io_phery_usb0_DIR
(
hps_usb_dir),
.
sys_hps_io_hps_io_phery_usb0_NXT
(
hps_usb_nxt),
.
sys_hps_io_hps_io_phery_uart1_RX
(
hps_uart_rx),
.
sys_hps_io_hps_io_phery_uart1_TX
(
hps_uart_tx),
                                                                   .
sys_hps_io_hps_io_phery_i2c1_SDA
                                                                   (
hps_i2c_sda),
                                                                   .
sys_hps_io_hps_io_phery_i2c1_SCL
                                                                   (
hps_i2c_scl),
                                                                   .
sys_hps_io_hps_io_gpio_gpio1_io5
                                                                   (
hps_gpio[0]),
                                                                   .
sys_hps_io_hps_io_gpio_gpio1_io14
                                                                   (
hps_gpio[1]),
                                                                   .
sys_hps_io_hps_io_gpio_gpio1_io16
                                                                   (
hps_gpio[2]),
                                                                   .
sys_hps_io_hps_io_gpio_gpio1_io17
                                                                   (
hps_gpio[3]),
                                                                   .
sys_hps_out_rstn_reset_n
                                                                   (
sys_hps_resetn),
                                                                   .
sys_hps_fpga_irq1_irq
                                                                  ({
32{1'b0}}),
                                                                   .
sys_hps_dma_data_awid(0),
                                                                   .
sys_hps_dma_data_awaddr(adc_hp0_axi_awaddr),
                                                                   .
sys_hps_dma_data_awlen(adc_hp0_axi_awlen),
                                                                   .
sys_hps_dma_data_awsize(adc_hp0_axi_awsize),
                                                                   .
sys_hps_dma_data_awburst(adc_hp0_axi_awburst),
                                                                   .
sys_hps_dma_data_awlock(0),
                                                                   .
sys_hps_dma_data_awcache(adc_hp0_axi_awcache),
                                                                   .
sys_hps_dma_data_awprot(adc_hp0_axi_awprot),
                                                                   .
sys_hps_dma_data_awvalid(adc_hp0_axi_awvalid),
                                                                   .
sys_hps_dma_data_awready(adc_hp0_axi_awready),
                                                                   .
sys_hps_dma_data_awuser(0),
                                                                   .
sys_hps_dma_data_wid(0),
                                                                   .
sys_hps_dma_data_wdata(adc_hp0_axi_wdata),
                                                                   .
sys_hps_dma_data_wstrb(adc_hp0_axi_wstrb),
                                                                   .
sys_hps_dma_data_wlast(adc_hp0_axi_wlast),
                                                                   .
sys_hps_dma_data_wvalid(adc_hp0_axi_wvalid),
                                                                   .
sys_hps_dma_data_wready(adc_hp0_axi_wready),
sys_hps_dma_data_bid(),
sys_hps_dma_data_bresp(adc_hp0_axi_bresp),
sys_hps_dma_data_bvalid(adc_hp0_axi_bvalid),
sys_hps_dma_data_bready(adc_hp0_axi_bready),
sys_hps_dma_data_arid(0),
sys_hps_dma_data_araddr(dac_hp1_axi_araddr),
sys_hps_dma_data_arlen(dac_hp1_axi_arlen),
sys_hps_dma_data_arsize(dac_hp1_axi_arsize),
sys_hps_dma_data_arburst(dac_hp1_axi_arburst),
sys_hps_dma_data_arlock(0),
sys_hps_dma_data_arcache(dac_hp1_axi_arcache),
sys_hps_dma_data_arprot(dac_hp1_axi_arprot),
sys_hps_dma_data_arvalid(dac_hp1_axi_arvalid),
sys_hps_dma_data_arready(dac_hp1_axi_arready),
sys_hps_dma_data_aruser(0),
sys_hps_dma_data_rid(),
sys_hps_dma_data_rdata(dac_hp1_axi_rdata),
sys_hps_dma_data_rresp(dac_hp1_axi_rresp),
sys_hps_dma_data_rlast(dac_hp1_axi_rlast),
sys_hps_dma_data_rvalid(dac_hp1_axi_rvalid),
sys_hps_dma_data_rready(dac_hp1_axi_rready),
sys_hps_ddr_mem_ck(hps_ddr_clk_p),
sys_hps_ddr_mem_ck_n(hps_ddr_clk_n),
sys_hps_ddr_mem_a(hps_ddr_a),
sys_hps_ddr_mem_act_n(hps_ddr_act_n),
sys_hps_ddr_mem_ba(hps_ddr_ba),
sys_hps_ddr_mem_bg(hps_ddr_bg),
sys_hps_ddr_mem_cke(hps_ddr_cke),
sys_hps_ddr_mem_cs_n(hps_ddr_cs_n),
sys_hps_ddr_mem_odt(hps_ddr_odt),
sys_hps_ddr_mem_reset_n(hps_ddr_reset_n),
sys_hps_ddr_mem_par(hps_ddr_par),
sys_hps_ddr_mem_alert_n(hps_ddr_alert_n),
                                                                         .
sys_hps_ddr_mem_dqs(hps_ddr_dqs_p),
                                                                         .
sys_hps_ddr_mem_dqs_n(hps_ddr_dqs_n),
                                                                         .
sys_hps_ddr_mem_dq(hps_ddr_dq),
                                                                         .
sys_hps_ddr_mem_dbi_n(hps_ddr_dbi_n),
                                                                         .
sys_hps_ddr_oct_oct_rzqin(hps_ddr_rzq),
                                                                         .
sys_hps_ddr_ref_clk_clk(hps_ddr_ref_clk),
                                                                         .
sys_hps_ddr_rstn_reset_n(sys_resetn),
                                                                         .
sys_spi_MISO(spi_miso),
                                                                         .
sys_spi_MOSI(spi_mosi),
                                                                         .
sys_spi_SCLK(spi_clk),
                                                                         .
sys_spi_SS_n(spi_csn),
                                                                         .
irq_irq({s_dac_dma_irq, s_adc_dma_irq, {2{1'b0}}})
)
```

Module instance of inst_system_ps_wrapper for the built in CPU.