system_wrapper.v

AUTHORS

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DATES

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INFORMATION

Brief

System wrapper for pl and ps for zed board.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
1,
parameter
FPGA_FAMILY
 =
4,
parameter
SPEED_GRADE
```

```
 =
10,
parameter
DEV_PACKAGE
 =
14,
parameter
DELAY_REFCLK_FREQUENCY
 =
200,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0
) ( inout [14:0] ddr_addr, inout [ 2:0] ddr_ba, inout ddr_cas_n, inout ddr_c
```

System wrapper for pl and ps for zed board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 1 is for 7 series.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 10 is for -1.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 14 is for cl.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

ddr_addr	DDR interface
ddr_ba	DDR interface
ddr_cas_n	DDR interface
ddr_ck_n	DDR interface
ddr_ck_p	DDR interface
ddr_cke	DDR interface
ddr_cs_n	DDR interface
ddr_dm	DDR interface
ddr_dq	DDR interface
ddr_dqs_n	DDR interface
ddr_dqs_p	DDR interface
ddr_odt	DDR interface
ddr_ras_n	DDR interface

ddr_reset_n	DDR interface
ddr_we_n	DDR interface
fixed_io_ddr_vrn	DDR interface
fixed_io_ddr_vrp	DDR interface
fixed_io_mio	ps mio
fixed_io_ps_clk	ps clk
fixed_io_ps_porb	ps por
fixed_io_ps_srstb	ps rst
iic_scl_fmc	fmcomms2-3 i2c
iic_sda_fmc	fmcomms2-3 i2c
gpio_bd	gpio
rx_clk_in_p	fmcomms2-3 rx clk
rx_clk_in_n	fmcomms2-3 rx clk
rx_frame_in_p	fmcomms2-3 rx frame
rx_frame_in_n	fmcomms2-3 rx frame
rx_data_in_p	fmcomms2-3 rx data
rx_data_in_n	fmcomms2-3 rx data
tx_clk_out_p	fmcomms2-3 tx clk
tx_clk_out_n	fmcomms2-3 tx clk
tx_frame_out_p	fmcomms2-3 tx frame
tx_frame_out_n	fmcomms2-3 tx frame
tx_data_out_p	fmcomms2-3 tx data
tx_data_out_n	fmcomms2-3 tx data
txnrx	fmcomms2-3 txnrx
enable	fmcomms2-3 enable
gpio_muxout_tx	fmcomms2-3 gpio
gpio_muxout_rx	fmcomms2-3 gpio
gpio_resetb	fmcomms2-3 gpio
gpio_sync	fmcomms2-3 gpio
gpio_en_agc	fmcomms2-3 gpio
gpio_ctl	fmcomms2-3 gpio
gpio_status	fmcomms2-3 gpio
spi_csn	spi chip select
spi_clk	spi clk
spi_mosi	spi master out
spi_miso	spi master in
spi_udc_csn_tx	spi udc chip select tx
spi_udc_csn_rx	spi udc chip select rx
spi_udc_sclk	spi udc clock
spi_udc_data	spi udc data

INSTANTIANTED MODULES

inst_system_pl_wrapper

```
system_pl_wrapper #(
                                                                                .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                                .
FPGA_FAMILY(FPGA_FAMILY),
                                                                                .
SPEED_GRADE(SPEED_GRADE),
                                                                                .
DEV_PACKAGE(DEV_PACKAGE),
                                                                                .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                                .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                                .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_system_pl_wrapper ( .axi_aclk(s_axi_clk), .axi_aresetn(s_axi_aresetn
```

Module instance of system_pl_wrapper for the fmcomms2-3 device.

inst_system_ps_wrapper

```
system_ps_wrapper inst_system_ps_wrapper (
                                                                                .
GPIO_I(gpio_i),
                                                                                .
GPIO_O(gpio_o),
                                                                                .
GPIO_T(gpio_t),
                                                                                .
SPI0_SCLK_I(1'b0),
                                                                                .
SPI0_SCLK_O(spi_clk),
                                                                                .
SPI0_MOSI_I(1'b0),
                                                                                .
SPI0_MOSI_O(spi_mosi),
                                                                                .
SPI0_MISO_I(spi_miso),
                                                                                .
SPI0_SS_I(1'b1),
                                                                                .
SPI0_SS_O(spi_csn),
                                                                                .
SPI1_SCLK_I(1'b0),
                                                                                .
SPI1_SCLK_O(spi_udc_sclk),
                                                                                .
SPI1_MOSI_I(spi_udc_data),
                                                                                .
SPI1_MOSI_O(spi_udc_data),
                                                                                .
SPI1_MISO_I(1'b0),
                                                                                .
SPI1_SS_I(1'b1),
                                                                                .
SPI1_SS_O(spi_udc_csn_tx),
```

```
SPI1_SS1_O(spi_udc_csn_rx),
SPI1_SS2_O(),
USB0_vbus_pwrfault(~otg_vbusoc),
M_AXI_araddr(w_axi_araddr),
M_AXI_arprot(w_axi_arprot),
M_AXI_arready(w_axi_arready),
M_AXI_arvalid(w_axi_arvalid),
M_AXI_awaddr(w_axi_awaddr),
M_AXI_awprot(w_axi_awprot),
M_AXI_awready(w_axi_awready),
M_AXI_awvalid(w_axi_awvalid),
M_AXI_bready(w_axi_bready),
M_AXI_bresp(w_axi_bresp),
M_AXI_bvalid(w_axi_bvalid),
M_AXI_rdata(w_axi_rdata),
M_AXI_rready(w_axi_rready),
M_AXI_rresp(w_axi_rresp),
M_AXI_rvalid(w_axi_rvalid),
M_AXI_wdata(w_axi_wdata),
M_AXI_wready(w_axi_wready),
M_AXI_wstrb(w_axi_wstrb),
M_AXI_wvalid(w_axi_wvalid),
S_AXI_HP0_arready(),
S_AXI_HP0_awready(adc_hp0_axi_awready),
S_AXI_HP0_bvalid(adc_hp0_axi_bvalid),
S_AXI_HP0_rlast(),
S_AXI_HP0_rvalid(),
S_AXI_HP0_wready(adc_hp0_axi_wready),
S_AXI_HP0_bresp(adc_hp0_axi_bresp),
S_AXI_HP0_rresp(),
S_AXI_HP0_bid(),
S_AXI_HP0_rid(),
S_AXI_HP0_rdata(),
```

```
S_AXI_HP0_ACLK(s_axi_clk),
S_AXI_HP0_arvalid(1'b0),
S_AXI_HP0_awvalid(adc_hp0_axi_awvalid),
S_AXI_HP0_bready(adc_hp0_axi_bready),
S_AXI_HP0_rready(1'b0),
S_AXI_HP0_wlast(adc_hp0_axi_wlast),
S_AXI_HP0_wvalid(adc_hp0_axi_wvalid),
S_AXI_HP0_arburst(2'b01),
S_AXI_HP0_arlock(0),
S_AXI_HP0_arsize(3'b011),
S_AXI_HP0_awburst(adc_hp0_axi_awburst),
S_AXI_HP0_awlock(0),
S_AXI_HP0_awsize(adc_hp0_axi_awsize),
S_AXI_HP0_arprot(0),
S_AXI_HP0_awprot(adc_hp0_axi_awprot),
S_AXI_HP0_araddr(0),
S_AXI_HP0_awaddr(adc_hp0_axi_awaddr),
S_AXI_HP0_arcache(4'b0011),
S_AXI_HP0_arlen(0),
S_AXI_HP0_arqos(0),
S_AXI_HP0_awcache(adc_hp0_axi_awcache),
S_AXI_HP0_awlen(adc_hp0_axi_awlen),
S_AXI_HP0_awqos(0),
S_AXI_HP0_arid(0),
S_AXI_HP0_awid(0),
S_AXI_HP0_wid(0),
S_AXI_HP0_wdata(adc_hp0_axi_wdata),
S_AXI_HP0_wstrb(adc_hp0_axi_wstrb),
S_AXI_HP1_arready(dac_hp1_axi_arready),
S_AXI_HP1_awready(),
S_AXI_HP1_bvalid(),
S_AXI_HP1_rlast(dac_hp1_axi_rlast),
S_AXI_HP1_rvalid(dac_hp1_axi_rvalid),
```

```
.
S_AXI_HP1_wready(),
.
S_AXI_HP1_bresp(),
.
S_AXI_HP1_rresp(dac_hp1_axi_rresp),
.
S_AXI_HP1_bid(),
.
S_AXI_HP1_rid(),
.
S_AXI_HP1_rdata(dac_hp1_axi_rdata),
.
S_AXI_HP1_ACLK(s_axi_clk),
.
S_AXI_HP1_arvalid(dac_hp1_axi_arvalid),
.
S_AXI_HP1_awvalid(1'b0),
.
S_AXI_HP1_bready(1'b0),
.
S_AXI_HP1_rready(dac_hp1_axi_rready),
.
S_AXI_HP1_wlast(1'b0),
.
S_AXI_HP1_wvalid(1'b0),
.
S_AXI_HP1_arburst(dac_hp1_axi_arburst),
.
S_AXI_HP1_arlock(0),
.
S_AXI_HP1_arsize(dac_hp1_axi_arsize),
.
S_AXI_HP1_awburst(2'b01),
.
S_AXI_HP1_awlock(0),
.
S_AXI_HP1_awsize(3'b011),
.
S_AXI_HP1_arprot(dac_hp1_axi_arprot),
.
S_AXI_HP1_awprot(0),
.
S_AXI_HP1_araddr(dac_hp1_axi_araddr),
.
S_AXI_HP1_awaddr(0),
.
S_AXI_HP1_arcache(dac_hp1_axi_arcache),
.
S_AXI_HP1_arlen(dac_hp1_axi_arlen),
.
S_AXI_HP1_arqos(0),
.
S_AXI_HP1_awcache(4'b0011),
.
S_AXI_HP1_awlen(0),
.
S_AXI_HP1_awqos(0),
.
S_AXI_HP1_arid(0),
.
S_AXI_HP1_awid(0),
.
S_AXI_HP1_wid(0),
.
S_AXI_HP1_wdata(0),
```

```
.
S_AXI_HP1_wstrb(~0),                                                                .
IRQ_F2P({{2{1'b0}}, s_adc_dma_irq, s_dac_dma_irq, s_iic2intc_irpt, {11{1'b0          .
FCLK_CLK0(s_axi_clk),                                                               .
FCLK_CLK1(s_delay_clk),                                                             .
FIXED_IO_mio(fixed_io_mio),                                                         .
DDR_cas_n(ddr_cas_n),                                                               .
DDR_cke(ddr_cke),                                                                   .
DDR_ck_n(ddr_ck_n),                                                                 .
DDR_ck_p(ddr_ck_p),                                                                 .
DDR_cs_n(ddr_cs_n),                                                                 .
DDR_reset_n(ddr_reset_n),                                                           .
DDR_odt(ddr_odt),                                                                   .
DDR_ras_n(ddr_ras_n),                                                               .
DDR_we_n(ddr_we_n),                                                                 .
DDR_ba(ddr_ba),                                                                     .
DDR_addr(ddr_addr),                                                                 .
FIXED_IO_ddr_vrn(fixed_io_ddr_vrn),                                                 .
FIXED_IO_ddr_vrp(fixed_io_ddr_vrp),                                                 .
DDR_dm(ddr_dm),                                                                     .
DDR_dq(ddr_dq),                                                                     .
DDR_dqs_n(ddr_dqs_n),                                                               .
DDR_dqs_p(ddr_dqs_p),                                                               .
FIXED_IO_ps_srstb(fixed_io_ps_srstb),                                               .
FIXED_IO_ps_clk(fixed_io_ps_clk),                                                   .
FIXED_IO_ps_porb(fixed_io_ps_porb),                                                 .
peripheral_aresetn(s_axi_aresetn)
)
```

Module instance of inst_system_ps_wrapper for the built in CPU.