system_pl_wrapper.v

AUTHORS

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DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl only for zcu102 board.

License MIT

system_pl_wrapper

```
module system_pl_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
0,
parameter
FPGA_FAMILY
 =
0,
parameter
SPEED_GRADE
```

```
 =
0,
parameter
DEV_PACKAGE
 =
0,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0,
parameter
DELAY_REFCLK_FREQUENCY
 =
200
) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_
```

System wrapper for pl only for zcu102 board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 3 is for ultrascale+.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 20 is for -2.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 3 is for ff.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

axi_aclk	AXI Lite control bus
axi_aresetn	AXI Lite control bus
s_axi_awvalid	AXI Lite control bus
s_axi_awaddr	AXI Lite control bus
s_axi_awready	AXI Lite control bus
s_axi_awprot	AXI Lite control bus
s_axi_wvalid	AXI Lite control bus
s_axi_wdata	AXI Lite control bus
s_axi_wstrb	AXI Lite control bus
s_axi_wready	AXI Lite control bus
s_axi_bvalid	AXI Lite control bus
s_axi_bresp	AXI Lite control bus
s_axi_bready	AXI Lite control bus

s_axi_arvalid	AXI Lite control bus
s_axi_araddr	AXI Lite control bus
s_axi_arready	AXI Lite control bus
s_axi_arprot	AXI Lite control bus
s_axi_rvalid	AXI Lite control bus
s_axi_rready	AXI Lite control bus
s_axi_rresp	AXI Lite control bus
s_axi_rdata	AXI Lite control bus
adc_dma_irq	fmcomms2-3 ADC irq
dac_dma_irq	fmcomms2-3 DAC irq
delay_clk	fmcomms2-3 delay clock
rx_clk_in_p	fmcomms2-3 receive clock in
rx_clk_in_n	fmcomms2-3 receive clock in
rx_frame_in_p	fmcomms2-3 receive frame
rx_frame_in_n	fmcomms2-3 receive frame
rx_data_in_p	fmcomms2-3 receive lvds data
rx_data_in_n	fmcomms2-3 receive lvds data
tx_clk_out_p	fmcomms2-3 transmit clock
tx_clk_out_n	fmcomms2-3 transmit clock
tx_frame_out_p	fmcomms2-3 transmit frame
tx_frame_out_n	fmcomms2-3 transmit frame
tx_data_out_p	fmcomms2-3 transmit lvds data
tx_data_out_n	fmcomms2-3 transmit lvds data
enable	fmcomms2-3 enable
txnrx	fmcomms2-3 txnrx select
up_enable	fmcomms2-3 enable input
up_txnrx	fmcomms2-3 txnrx select input
tdd_sync_t	fmcomms2-3 TDD sync i/o
tdd_sync_i	fmcomms2-3 TDD sync i/o
tdd_sync_o	fmcomms2-3 TDD sync i/o
adc_m_dest_axi_awaddr	fmcomms2-3 ADC DMA
adc_m_dest_axi_awlen	fmcomms2-3 ADC DMA
adc_m_dest_axi_awsize	fmcomms2-3 ADC DMA
adc_m_dest_axi_awburst	fmcomms2-3 ADC DMA
adc_m_dest_axi_awprot	fmcomms2-3 ADC DMA
adc_m_dest_axi_awcache	fmcomms2-3 ADC DMA
adc_m_dest_axi_awvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_awready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wdata	fmcomms2-3 ADC DMA
adc_m_dest_axi_wstrb	fmcomms2-3 ADC DMA
adc_m_dest_axi_wready	fmcomms2-3 ADC DMA
adc_m_dest_axi_wvalid	fmcomms2-3 ADC DMA

adc_m_dest_axi_wlast	fmcomms2-3 ADC DMA
adc_m_dest_axi_bvalid	fmcomms2-3 ADC DMA
adc_m_dest_axi_bresp	fmcomms2-3 ADC DMA
adc_m_dest_axi_bready	fmcomms2-3 ADC DMA
dac_m_src_axi_arready	fmcomms2-3 DAC DMA
dac_m_src_axi_arvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_araddr	fmcomms2-3 DAC DMA
dac_m_src_axi_arlen	fmcomms2-3 DAC DMA
dac_m_src_axi_arsize	fmcomms2-3 DAC DMA
dac_m_src_axi_arburst	fmcomms2-3 DAC DMA
dac_m_src_axi_arprot	fmcomms2-3 DAC DMA
dac_m_src_axi_arcache	fmcomms2-3 DAC DMA
dac_m_src_axi_rdata	fmcomms2-3 DAC DMA
dac_m_src_axi_rready	fmcomms2-3 DAC DMA
dac_m_src_axi_rvalid	fmcomms2-3 DAC DMA
dac_m_src_axi_rresp	fmcomms2-3 DAC DMA
dac_m_src_axi_rlast	fmcomms2-3 DAC DMA

INSTANTIANTED MODULES

inst_ad9361_pl_wrapper

```
ad9361_pl_wrapper #(
                                                                    .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                    .
FPGA_FAMILY(FPGA_FAMILY),
                                                                    .
SPEED_GRADE(SPEED_GRADE),
                                                                    .
DEV_PACKAGE(DEV_PACKAGE),
                                                                    .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                    .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                    .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY),
                                                                    .
DMA_AXI_PROTOCOL_TO_PS(0),
                                                                    .
AXI_DMAC_ADC_ADDR(32'h9C400000),
                                                                    .
AXI_DMAC_DAC_ADDR(32'h9C420000),
                                                                    .
AXI_AD9361_ADDR(32'h99020000)
) inst_ad9361_pl_wrapper ( .axi_aclk(axi_aclk), .axi_aresetn(axi_aresetn),
```

Module instance of ad9361_pl_wrapper for the fmcomms2-3 device.