system_wrapper.v

AUTHORS

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DATES

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INFORMATION

Brief

System wrapper for pl and ps for zcu102 board.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
3,
parameter
FPGA_FAMILY
 =
4,
parameter
SPEED_GRADE
```

```
 =
20,
parameter
DEV_PACKAGE
 =
3,
parameter
DELAY_REFCLK_FREQUENCY
 =
500,
parameter
ADC_INIT_DELAY
 =
11,
parameter
DAC_INIT_DELAY
 =
0
) ( input [12:0] gpio_bd_i, output [ 7:0] gpio_bd_o, input rx_clk_in_p, inpu
```

System wrapper for pl and ps for zcu102 board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 3 is for ultrascale+.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 20 is for -2.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 3 is for ff.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

gpio_bd_i	gpio
gpio_bd_o	gpio
rx_clk_in_p	fmcomms2-3 rx clk
rx_clk_in_n	fmcomms2-3 rx clk
rx_frame_in_p	fmcomms2-3 rx frame
rx_frame_in_n	fmcomms2-3 rx frame
rx_data_in_p	fmcomms2-3 rx data
rx_data_in_n	fmcomms2-3 rx data
tx_clk_out_p	fmcomms2-3 tx clk
tx_clk_out_n	fmcomms2-3 tx clk
tx_frame_out_p	fmcomms2-3 tx frame
tx_frame_out_n	fmcomms2-3 tx frame

tx_data_out_p	fmcomms2-3 tx data
tx_data_out_n	fmcomms2-3 tx data
txnrx	fmcomms2-3 txnrx
enable	fmcomms2-3 enable
gpio_resetb	fmcomms2-3 gpio
gpio_sync	fmcomms2-3 gpio
gpio_en_agc	fmcomms2-3 gpio
gpio_ctl	fmcomms2-3 gpio
gpio_status	fmcomms2-3 gpio
spi_csn	spi chip select
spi_clk	spi clk
spi_mosi	spi master out
spi_miso	spi master in

INSTANTIANTED MODULES

inst_system_pl_wrapper

```
system_pl_wrapper #(
                                                                                .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                                .
FPGA_FAMILY(FPGA_FAMILY),
                                                                                .
SPEED_GRADE(SPEED_GRADE),
                                                                                .
DEV_PACKAGE(DEV_PACKAGE),
                                                                                .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                                .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                                .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_system_pl_wrapper ( .axi_aclk(s_axi_clk), .axi_aresetn(s_axi_aresetn
```

Module instance of system_pl_wrapper for the fmcomms2-3 device.

inst_system_ps_wrapper

```
system_ps_wrapper inst_system_ps_wrapper (
                                                                                .
M_AXI_araddr(w_axi_araddr),
                                                                                .
M_AXI_arprot(w_axi_arprot),
                                                                                .
M_AXI_arready(w_axi_arready),
                                                                                .
M_AXI_arvalid(w_axi_arvalid),
                                                                                .
M_AXI_awaddr(w_axi_awaddr),
                                                                                .
```

```
M_AXI_awprot(w_axi_awprot),
M_AXI_awready(w_axi_awready),
M_AXI_awvalid(w_axi_awvalid),
M_AXI_bready(w_axi_bready),
M_AXI_bresp(w_axi_bresp),
M_AXI_bvalid(w_axi_bvalid),
M_AXI_rdata(w_axi_rdata),
M_AXI_rready(w_axi_rready),
M_AXI_rresp(w_axi_rresp),
M_AXI_rvalid(w_axi_rvalid),
M_AXI_wdata(w_axi_wdata),
M_AXI_wready(w_axi_wready),
M_AXI_wstrb(w_axi_wstrb),
M_AXI_wvalid(w_axi_wvalid),
S_AXI_HP0_arready(),
S_AXI_HP0_awready(adc_hp0_axi_awready),
S_AXI_HP0_bvalid(adc_hp0_axi_bvalid),
S_AXI_HP0_rlast(),
S_AXI_HP0_rvalid(),
S_AXI_HP0_wready(adc_hp0_axi_wready),
S_AXI_HP0_bresp(adc_hp0_axi_bresp),
S_AXI_HP0_rresp(),
S_AXI_HP0_bid(),
S_AXI_HP0_rid(),
S_AXI_HP0_rdata(),
S_AXI_HP0_ACLK(s_axi_clk),
S_AXI_HP0_arvalid(1'b0),
S_AXI_HP0_awvalid(adc_hp0_axi_awvalid),
S_AXI_HP0_bready(adc_hp0_axi_bready),
S_AXI_HP0_rready(1'b0),
S_AXI_HP0_wlast(adc_hp0_axi_wlast),
S_AXI_HP0_wvalid(adc_hp0_axi_wvalid),
S_AXI_HP0_arburst(2'b01),
```

```
S_AXI_HP0_arlock(0),
S_AXI_HP0_arsize(3'b011),
S_AXI_HP0_awburst(adc_hp0_axi_awburst),
S_AXI_HP0_awlock(0),
S_AXI_HP0_awsize(adc_hp0_axi_awsize),
S_AXI_HP0_arprot(0),
S_AXI_HP0_awprot(adc_hp0_axi_awprot),
S_AXI_HP0_araddr(0),
S_AXI_HP0_awaddr(adc_hp0_axi_awaddr),
S_AXI_HP0_arcache(4'b0011),
S_AXI_HP0_arlen(0),
S_AXI_HP0_arqos(0),
S_AXI_HP0_awcache(adc_hp0_axi_awcache),
S_AXI_HP0_awlen(adc_hp0_axi_awlen),
S_AXI_HP0_awqos(0),
S_AXI_HP0_arid(0),
S_AXI_HP0_awid(0),
S_AXI_HP0_wdata(adc_hp0_axi_wdata),
S_AXI_HP0_wstrb(adc_hp0_axi_wstrb),
S_AXI_HP0_aruser(1'b0),
S_AXI_HP0_awuser(1'b0),
S_AXI_HP1_arready(dac_hp1_axi_arready),
S_AXI_HP1_awready(),
S_AXI_HP1_bvalid(),
S_AXI_HP1_rlast(dac_hp1_axi_rlast),
S_AXI_HP1_rvalid(dac_hp1_axi_rvalid),
S_AXI_HP1_wready(),
S_AXI_HP1_bresp(),
S_AXI_HP1_rresp(dac_hp1_axi_rresp),
S_AXI_HP1_bid(),
S_AXI_HP1_rid(),
S_AXI_HP1_rdata(dac_hp1_axi_rdata),
S_AXI_HP1_ACLK(s_axi_clk),
```

```
S_AXI_HP1_arvalid(dac_hp1_axi_arvalid),
S_AXI_HP1_awvalid(1'b0),
S_AXI_HP1_bready(1'b0),
S_AXI_HP1_rready(dac_hp1_axi_rready),
S_AXI_HP1_wlast(1'b0),
S_AXI_HP1_wvalid(1'b0),
S_AXI_HP1_arburst(dac_hp1_axi_arburst),
S_AXI_HP1_arlock(0),
S_AXI_HP1_arsize(dac_hp1_axi_arsize),
S_AXI_HP1_awburst(2'b01),
S_AXI_HP1_awlock(0),
S_AXI_HP1_awsize(3'b011),
S_AXI_HP1_arprot(dac_hp1_axi_arprot),
S_AXI_HP1_awprot(0),
S_AXI_HP1_araddr(dac_hp1_axi_araddr),
S_AXI_HP1_awaddr(0),
S_AXI_HP1_arcache(dac_hp1_axi_arcache),
S_AXI_HP1_arlen(dac_hp1_axi_arlen),
S_AXI_HP1_arqos(0),
S_AXI_HP1_awcache(4'b0011),
S_AXI_HP1_awlen(0),
S_AXI_HP1_awqos(0),
S_AXI_HP1_arid(0),
S_AXI_HP1_awid(0),
S_AXI_HP1_wdata(0),
S_AXI_HP1_wstrb(~0),
S_AXI_HP1_aruser(1'b0),
S_AXI_HP1_awuser(1'b0),
gpio_i(gpio_i),
gpio_o(gpio_o),
gpio_t(),
peripheral_aresetn(s_axi_aresetn),
pl_clk0(s_axi_clk),
```

```
 pl_clk1(),                                                                                                .
 pl_clk2(s_delay_clk),                                                                                     .
 pl_ps_irq1({{2{1'b0}}, s_adc_dma_irq, s_dac_dma_irq, {4{1'b0}}}),                                         .
 spi0_m_i(spi_miso),                                                                                       .
 spi0_m_o(spi_mosi),                                                                                       .
 spi0_mo_t(),                                                                                              .
 spi0_s_i(1'b0),                                                                                           .
 spi0_s_o(),                                                                                               .
 spi0_sclk_i(1'b0),                                                                                        .
 spi0_sclk_o(spi_clk),                                                                                     .
 spi0_sclk_t(),                                                                                            .
 spi0_so_t(),                                                                                              .
 spi0_ss1_o_n(),                                                                                           .
 spi0_ss2_o_n(),                                                                                           .
 spi0_ss_i_n(1'b1),                                                                                        .
 spi0_ss_n_t(),                                                                                            .
 spi0_ss_o_n(spi_csn),                                                                                     .
 spi1_m_i(1'b0),                                                                                           .
 spi1_m_o(),                                                                                               .
 spi1_mo_t(),                                                                                              .
 spi1_s_i(1'b0),                                                                                           .
 spi1_s_o(),                                                                                               .
 spi1_sclk_i(1'b0),                                                                                        .
 spi1_sclk_o(),                                                                                            .
 spi1_sclk_t(),                                                                                            .
 spi1_so_t(),                                                                                              .
 spi1_ss1_o_n(),                                                                                           .
 spi1_ss2_o_n(),                                                                                           .
 spi1_ss_i_n(1'b1),                                                                                        .
 spi1_ss_n_t(),                                                                                            .
 spi1_ss_o_n()
)
```

Module instance of inst_system_ps_wrapper for the built in CPU.