

# system\_pl\_wrapper.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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System wrapper for pl only for arria10soc board.

### License MIT

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## system\_pl\_wrapper

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```
module system_pl_wrapper #(
    parameter
    FPGA_TECHNOLOGY
    =
    0,
    parameter
    FPGA_FAMILY
    =
    0,
    parameter
    SPEED_GRADE
```

```

    =
    0,
    parameter
    DEV_PACKAGE
    =
    0,
    parameter
    ADC_INIT_DELAY
    =
    23,
    parameter
    DAC_INIT_DELAY
    =
    0,
    parameter
    DELAY_REFCLK_FREQUENCY
    =
    200
  ) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_

```

System wrapper for pl only for arria10soc board.

## Parameters

<b>FPGA_TECHNOLOGY</b> parameter	Type of FPGA, such as Ultrascale, Arria 10. 103 is for Arria 10.
<b>FPGA_FAMILY</b> parameter	Sub type of fpga, such as GX, SX, etc. 1 is for SX
<b>SPEED_GRADE</b> parameter	Number that corresponds to the ships recommended speed. 2 is for 2.
<b>DEV_PACKAGE</b> parameter	Specify a number that is equal to the manufactures package. 3 is for FBGA.
<b>ADC_INIT_DELAY</b> parameter	Initial Delay for the ADC
<b>DAC_INIT_DELAY</b> parameter	Initial Delay for the DAC
<b>DELAY_REFCLK_FREQUENCY</b> parameter	Reference clock frequency used for ad_data_in instances

## Ports

<b>axi_aclk</b>	AXI Lite control bus
<b>axi_aresetn</b>	AXI Lite control bus
<b>s_axi_awvalid</b>	AXI Lite control bus
<b>s_axi_awaddr</b>	AXI Lite control bus
<b>s_axi_awready</b>	AXI Lite control bus
<b>s_axi_awprot</b>	AXI Lite control bus
<b>s_axi_wvalid</b>	AXI Lite control bus
<b>s_axi_wdata</b>	AXI Lite control bus
<b>s_axi_wstrb</b>	AXI Lite control bus
<b>s_axi_wready</b>	AXI Lite control bus
<b>s_axi_bvalid</b>	AXI Lite control bus
<b>s_axi_bresp</b>	AXI Lite control bus
<b>s_axi_bready</b>	AXI Lite control bus

<b>s_axi_arvalid</b>	AXI Lite control bus
<b>s_axi_araddr</b>	AXI Lite control bus
<b>s_axi_arready</b>	AXI Lite control bus
<b>s_axi_arprot</b>	AXI Lite control bus
<b>s_axi_rvalid</b>	AXI Lite control bus
<b>s_axi_rready</b>	AXI Lite control bus
<b>s_axi_rresp</b>	AXI Lite control bus
<b>s_axi_rdata</b>	AXI Lite control bus
<b>adc_dma_irq</b>	fmcomms2-3 ADC irq
<b>dac_dma_irq</b>	fmcomms2-3 DAC irq
<b>delay_clk</b>	fmcomms2-3 delay clock
<b>rx_clk_in_p</b>	fmcomms2-3 receive clock in
<b>rx_clk_in_n</b>	fmcomms2-3 receive clock in
<b>rx_frame_in_p</b>	fmcomms2-3 receive frame
<b>rx_frame_in_n</b>	fmcomms2-3 receive frame
<b>rx_data_in_p</b>	fmcomms2-3 receive lvds data
<b>rx_data_in_n</b>	fmcomms2-3 receive lvds data
<b>tx_clk_out_p</b>	fmcomms2-3 transmit clock
<b>tx_clk_out_n</b>	fmcomms2-3 transmit clock
<b>tx_frame_out_p</b>	fmcomms2-3 transmit frame
<b>tx_frame_out_n</b>	fmcomms2-3 transmit frame
<b>tx_data_out_p</b>	fmcomms2-3 transmit lvds data
<b>tx_data_out_n</b>	fmcomms2-3 transmit lvds data
<b>enable</b>	fmcomms2-3 enable
<b>txnrx</b>	fmcomms2-3 txnrx select
<b>up_enable</b>	fmcomms2-3 enable input
<b>up_txnrx</b>	fmcomms2-3 txnrx select input
<b>tdd_sync_t</b>	fmcomms2-3 TDD sync i/o
<b>tdd_sync_i</b>	fmcomms2-3 TDD sync i/o
<b>tdd_sync_o</b>	fmcomms2-3 TDD sync i/o
<b>adc_m_dest_axi_awaddr</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awlen</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awsz</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awburst</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awprot</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awcache</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awvalid</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_awready</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_wdata</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_wstrb</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_wready</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_wvalid</b>	fmcomms2-3 ADC DMA

<b>adc_m_dest_axi_wlast</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_bvalid</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_bresp</b>	fmcomms2-3 ADC DMA
<b>adc_m_dest_axi_bready</b>	fmcomms2-3 ADC DMA
<b>dac_m_src_axi_arready</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arvalid</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_araddr</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arlen</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arsize</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arburst</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arprot</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_arcache</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_rdata</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_rready</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_rvalid</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_rresp</b>	fmcomms2-3 DAC DMA
<b>dac_m_src_axi_rlast</b>	fmcomms2-3 DAC DMA

## INSTANTIATED MODULES

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### inst\_ad9361\_pl\_wrapper

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```

ad9361_pl_wrapper #(
    FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
    FPGA_FAMILY(FPGA_FAMILY),
    SPEED_GRADE(SPEED_GRADE),
    DEV_PACKAGE(DEV_PACKAGE),
    ADC_INIT_DELAY(ADC_INIT_DELAY),
    DAC_INIT_DELAY(DAC_INIT_DELAY),
    DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY),
    AXI_DMAC_ADC_ADDR(32'h00010000),
    AXI_DMAC_DAC_ADDR(32'h00014000),
    AXI_AD9361_ADDR(32'h00000000)
) inst_ad9361_pl_wrapper ( .axi_aclk(axi_aclk), .axi_aresetn(axi_aresetn),

```

Module instance of ad9361\_pl\_wrapper for the fmcomms2-3 device.