Arria 10 SoC FPGA Development Kit Board

REV	DATE	PAGES	DESCRIPTION
A1		All	INITIAL REVISION A RELEASE
A1.1		22	Change RGMII reference clock source, pull up to 1v8
		40	DP clock netname is changed
		42	LED resitors are changed to 100ohm
		6,52,57	Change ED8101 I2C address to 0X0E and 0X10
		55,68,69	Change DMP3098L to DMG2305UX,
		28	Change netnames
		45	Change Header to 0.1inch header
		55	Add logic to turn off A10 power when MAXV need be reprogrammed.
		55,68	Change PMOS to NMOS for reducing ON resistance
		56	ADD two LDOs for U31
		51	ADD Linear LDOs for U24
		19	HPS DM_alert bit postions are modified based on Quartus report
		38	Move Mictor trace JTAG into 1.8 Bank of Max2
		36	Connect 3V3 to BANK4
		05	Update Clock diagram
A2		21	Add 1K PULL UP resistors for MSEL[0..2], HPS,NPOR, HPSNRST (only in SCH)
		25	Change R98 and R99 to 1K ohm
		22	Change R367 and R378 to 4.7K ohm
		74	Change R646 pull up voltage to I01V8, Change R674 to 100K ohm
		51	Need Install U74,Install D44, R156, DNI R157 Based on FB 282099
		45	Change LCD address to 0x28
		56	Install D43
		60	Update the sense RC netowrk values based on FB 261730, add +-15% voltage adjustable range
		59	Update the sense RC netowrk values based on FB 261730
		66	Update the sense RC netowrk values based on FB 261730
		64	Update the sense RC netowrk values based on FB 261730
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		62	Update the sense RC netowrk values based on FB 261730
		54	Update the sense RC netowrk values based on FB 261730
		57	Change remote senseing point to FGPA pins
		60	Change R495 value from 240K to 226K for generating 1.03V output
		57	Change ED8101P01QI to ED8101P04QI for 0.95V output
		52	Change ED8101P02QI to ED8101P05QI for 0.95V output
		51,52,56,57	Change R5258, R5243, R5045 & R5055 from 2K to 1.5K based on FB302118
		22	Change Linear LDO from LTC3026 to LTC3026-1
B		11,12,20,36	MDIOMDICof EMAC1 and EMAC2 are mapped to IO PINS of MAXV_IO CPLD
		20,36	MOVE HPS_LED2,3, HPS_PB3 and HPS_DIP3 to Share IO port
		23,35	Move dedicate UART port to system MAXV
		51	USE LTM4676A to generate 3.3V power
		56	USE LTM4677 to generate 0.9V power
		45	Change J28 to the Linear Header
		58	Change R655 to 1M ohm 1% resistor for 0.9V output
		16	R230, R237= DNI, R229, R236 =10K to enable hardware mode
		16	Uninstall R253,R238 and install R233 and R232
C		11,12, 22	Change pull up resistor R312,R306,R68,R62 to 1K
			Change U23 to Production Silicon
		68	Change R5510, R454 to 10K ohm
		69	Change R393 to 49.9K ohm

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Arria 10 Dev Kit Block Diagram

HILO_HPS_DC (X40)

Boot Flash DC

10/100/1000 RGMII PHY KSA9031RN

USB 2.0 PHY USB3320

UART to USB

USER Interface

PS

EPCQ FLASH

SEEPROM/ RTC/TEMP

LT_I2C

ClockI2C

Ext I2C 1

Ext I2C 2

PMBUS

LCD

MAXV Block

S P I

1KB EEPROM

DDR3/ DDR4

14-bit IO

RGMII

USB2.0

UART1 TX/RX

4-bit Trace

SPI

I2C1

ASconfigure

EPCQ FLASH

2J 2K

Dedicated_IO

Shared_IO 2L

CCS

Clock Block

10AS066N2F40 **HPS**

DDR3/DDR4 hardcore

DDR3/DDR4 hardcore

PCIE GEN3 x8 Hardcore CVp

SGMII Mac Core

PCIE GEN3 x8 Hardcore

FPGA

3B 3C 3D

1H 1I

3F 3H 3G

3E 3A

1C 1D 1G

1E 1F

1J

2I 2A

120-bit Bus

10 Channels

168-bit Bus

FPGA_IO

MAXV

DPIO SDI IO

3V3IO

72-Bit Bus

S F P + X 2

16 Channels

x2

8 Channels

X1

4 Channels

14-Bit Bus

17-Bit Trace

Debug Bus

Enpirion Power Block

HILO_FPGA_DC (X72)

FMCA

V57.1

FMCB

PCIE EP

2X SGMII PHY 88E1111

PCIE Gen3/2/1 x8 RC

SDI/O

Display Port

FILE_FLASH DC

MAX2

USB Blaster 2

V57.1 Two FMC Slots

ALTERA

Arria 10 Dev Kit Clock Connection

Clock Sources

Clock source blocks:
- SMA → Clock MUX → VCO (OSC_IN, CP1)
- LMK04828 Clock Cleaner, Jitter rms < 0.1ps — U26
- SI52112 Clock Generator, Jitter rms < 1ps — U11
- SI516 Clock Generator, Jitter rms < 1ps — U56
- SI5338A Clock Generator, Jitter rms < 1ps — U42
- SI5338A Clock Generator, Jitter rms < 1ps — U50
- SI5338A Clock Generator, Jitter rms < 1ps — U49
- OSC_50MHz — U51
- OSC_33MHz — Y7
- FMCB — J19
- FMCA — J29

Signal labels:
SMA_LMK_CLK_IN, LMK_SYNC_IN, FBCLK0M2C, CLK_3A, FACLK3BDIR_SYSREF, CLK_EMI, FACLK1M2C, CLK_3E, LMK_CLEAN_CLK, CLK_FAEMI, FACLK0M2C, FACLK2BDIR, RCLOCK_OUT, REFCLK_SMA, LMK_FMCCLK, EXTSMACLK, FBGBTCLK0M2C, CLK_ENET_FPGA, REFCLK_DP, FAGBTCLK0M2C, LMK_FMCCLK, PCIE_REFCLK_QRD, FBGBTCLK1M2C, REFCLK_SDI, FAGBTCLK1M2C, OSC2_CLK_SMA, OSC2_CLK_SYN, OSC2_HPS_CLK, FPGA_RCLK_3G, REFCLK_SMA, CLKUSR_USR, CLK_HPSEMI, FA_EMI_CLK, REFCLK3A, FPGA_REFsys, REFCLK3E, HPS_CLK1

A10 SOC pins: 1C 1D 1E 1F 1G 1H 1I 1J 2A 2I 2J 2K 2L 3A 3B 3C 3D 3E 3F 3G 3H CCS

A10 SOC

Title: **Arria 10 SoC FPGA Development Kit Board**

Size: B
Document Number: 150-0321308   (6XX-44382R)
Rev: C

Date: Thursday, March 31, 2016   Sheet 5 of 78

Arria 10 Dev Kit I2C bus Connection

ADC
LTC2497
(Current of
DC)
Address =
b'0010100'

◄LTBUS►

ADC
LTC2497
Current of
Core, C2
Address =
b'0010110'

A10_HPS_
I2C1

I2C1

LEVEL
Shift
FXMA2102
UMX

SEEPROM
24LC32A

Address =
b'1010001'

◄Bus 1►

RTC
DS1339C

Address =
b'1101000'

◄Bus 1►

TEMP
MAX1619

Address =
b'1001100'

A10_2LI2C

SFP+A

Address =
b'1010000'

◄EXTABus►

PCIE Slot

Address =
b'???'

◄EXTABus►

FMCA slot

Address =
b'???'

A10I2CEN

SFP+B

Address =
b'1010000'

◄EXTBBus►

FMCB slot

Address =
b'???'

Max V

LEVEL
Shift
FXMA2102
UMX

BUS1

Clock
SI5338

Address =
b'1110001'

◄ClockBus►

Clock
SI5338
XCVR

Address =
b'1110000'

◄ClockBus►

Clock
SI5338
EMI Clock

Address =
b'1110011'

MaxV

**2V5 I2C
Bus**

LEVEL
Shift
FXMA2102
UMX

◄PMBUS►

Power
Management
LTC2977

Address =
b'1011100'

◄PMBUS►

LTM4677
0.9V
output

Address =
b'1000010'

PMBUS

LTM4676A
3.3V
output

Address =
b'1001110'

◄PMBUS►

PMBUS
CON

PMBUS

A10PMBUSEN

LEVEL
Shift
FXMA2102
UMX

VID

A10_PMBUSDIS_N

Max V

A10_VID

**5V0 I2C
Bus**

LEVEL
Shift
FXMA2102
UMX

◄LCDbus►

LCD

Address =
b'0101000'

Application of two I2C masters in PMVID bus

FMCB (PCIE END-POINT) XCVRs & 2 x SFP + XCVRs

U23H

Pin	Signal		Net
18	FBGBTCLK0M2CP	AN29	REFCLK_GXBL1C_CHTP
18	FBGBTCLK0M2CN	AN28	REFCLK_GXBL1C_CHTN
18	FBD1C2MN	AT34	GXBL1C_TX_CH5N
18	FBD1C2MP	AT35	GXBL1C_TX_CH5P
18	FBD1M2CN	AM30	GXBL1C_RX_CH5N, GXBL1C_REFCLK5N
18	FBD1M2CP	AM31	GXBL1C_RX_CH5P, GXBL1C_REFCLK5P
18	FBD0C2MN	AU36	GXBL1C_TX_CH4N
18	FBD0C2MP	AU37	GXBL1C_TX_CH4P
18	FBD0M2CN	AN32	GXBL1C_RX_CH4N, GXBL1C_REFCLK4N
18	FBD0M2CP	AN33	GXBL1C_RX_CH4P, GXBL1C_REFCLK4P
18	FBD9C2MN	AV38	GXBL1C_TX_CH3N
18	FBD9C2MP	AV39	GXBL1C_TX_CH3P
18	FBD9M2CN	AP30	GXBL1C_RX_CH3N, GXBL1C_REFCLK3N
18	FBD9M2CP	AP31	GXBL1C_RX_CH3P, GXBL1C_REFCLK3P
18	FBD8C2MN	AV34	GXBL1C_TX_CH2N
18	FBD8C2MP	AV35	GXBL1C_TX_CH2P
18	FBD8M2CN	AR32	GXBL1C_RX_CH2N, GXBL1C_REFCLK2N
18	FBD8M2CP	AR33	GXBL1C_RX_CH2P, GXBL1C_REFCLK2P
14	SFPB_TX_N	AW36	GXBL1C_TX_CH1N
14	SFPB_TX_P	AW37	GXBL1C_TX_CH1P
14	SFPB_RX_N	AT30	GXBL1C_RX_CH1N, GXBL1C_REFCLK1N
14	SFPB_RX_P	AT31	GXBL1C_RX_CH1P, GXBL1C_REFCLK1P
13	SFPA_TX_N	AW32	GXBL1C_TX_CH0N
13	SFPA_TX_P	AW33	GXBL1C_TX_CH0P
13	SFPA_RX_N	AU32	GXBL1C_RX_CH0N, GXBL1C_REFCLK0N
13	SFPA_RX_P	AU33	GXBL1C_RX_CH0P, GXBL1C_REFCLK0P
41	LMK_SFPCLK_P	AR29	REFCLK_GXBL1C_CHBP
41	LMK_SFPCLK_N	AR28	REFCLK_GXBL1C_CHBN
	RREF_BL	AW30	RREF_BL

PCIE Hard Core with CVP
Channel 0, 1

R4078 RREF_BL 2.00k

Tranceiver 1C BanK

A10SOC_1517

U23G

Pin	Signal		Net
		AJ29	REFCLK_GXBL1D_CHTP
		AJ28	REFCLK_GXBL1D_CHTN
18	FBD7C2MN	AM38	GXBL1D_TX_CH5N
18	FBD7C2MP	AM39	GXBL1D_TX_CH5P
18	FBD7M2CN	AH30	GXBL1D_RX_CH5N, GXBL1D_REFCLK5N
18	FBD7M2CP	AH31	GXBL1D_RX_CH5P, GXBL1D_REFCLK5P
18	FBD6C2MN	AN36	GXBL1D_TX_CH4N
18	FBD6C2MP	AN37	GXBL1D_TX_CH4P
18	FBD6M2CN	AJ32	GXBL1D_RX_CH4N, GXBL1D_REFCLK4N
18	FBD6M2CP	AJ33	GXBL1D_RX_CH4P, GXBL1D_REFCLK4P
18	FBD5C2MN	AP38	GXBL1D_TX_CH3N
18	FBD5C2MP	AP39	GXBL1D_TX_CH3P
18	FBD5M2CN	AK34	GXBL1D_RX_CH3N, GXBL1D_REFCLK3N
18	FBD5M2CP	AK35	GXBL1D_RX_CH3P, GXBL1D_REFCLK3P
18	FBD4C2MN	AP34	GXBL1D_TX_CH2N
18	FBD4C2MP	AP35	GXBL1D_TX_CH2P
18	FBD4M2CN	AK30	GXBL1D_RX_CH2N, GXBL1D_REFCLK2N
18	FBD4M2CP	AK31	GXBL1D_RX_CH2P, GXBL1D_REFCLK2P
18	FBD3C2MN	AR36	GXBL1D_TX_CH1N
18	FBD3C2MP	AR37	GXBL1D_TX_CH1P
18	FBD3M2CN	AL32	GXBL1D_RX_CH1N, GXBL1D_REFCLK1N
18	FBD3M2CP	AL33	GXBL1D_RX_CH1P, GXBL1D_REFCLK1P
18	FBD2C2MN	AT38	GXBL1D_TX_CH0N
18	FBD2C2MP	AT39	GXBL1D_TX_CH0P
18	FBD2M2CN	AM34	GXBL1D_RX_CH0N, GXBL1D_REFCLK0N
18	FBD2M2CP	AM35	GXBL1D_RX_CH0P, GXBL1D_REFCLK0P
40	REFCLK0_FMCB_P	AL29	REFCLK_GXBL1D_CHBP
40	REFCLK0_FMCB_N	AL28	REFCLK_GXBL1D_CHBN

PCIE Hard Core with CVP
Channel 2,3,4,5,6,7

Tranceiver 1D BanK

A10SOC_1517

Application	Channel (Bank, number)
PCIE EP	(1C,4);(1C,5);(1D,0);(1D,1); (1D,2);(1D,3);(1D,4);(1D,5)
FMC B Slot DP Transceiver [0:9]	(1C,2);(1C,3);(1C,4);(1C,5); (1D,0);(1D,1);(1D,2);(1D,3); (1D,4);(1D,5);
SFP+ 0 and 1	(1C,0);(1C,1)

PCIE RC XCVRs & 2X SGMII XCVRs & FMCB XCVRs

U23F — Tranceiver 1E BanK

Pin	Net
AE29	REFCLK_GXBL1E_CHTP
AE28	REFCLK_GXBL1E_CHTN
AF38	GXBL1E_TX_CH5N
AF39	GXBL1E_TX_CH5P
AD30	GXBL1E_RX_CH5N, GXBL1E_REFCLK5N
AD31	GXBL1E_RX_CH5P, GXBL1E_REFCLK5P
AG36	GXBL1E_TX_CH4N
AG37	GXBL1E_TX_CH4P
AE32	GXBL1E_RX_CH4N, GXBL1E_REFCLK4N
AE33	GXBL1E_RX_CH4P, GXBL1E_REFCLK4P
AH38	GXBL1E_TX_CH3N
AH39	GXBL1E_TX_CH3P
AF34	GXBL1E_RX_CH3N, GXBL1E_REFCLK3N
AF35	GXBL1E_RX_CH3P, GXBL1E_REFCLK3P
AJ36	GXBL1E_TX_CH2N
AJ37	GXBL1E_TX_CH2P
AF30	GXBL1E_RX_CH2N, GXBL1E_REFCLK2N
AF31	GXBL1E_RX_CH2P, GXBL1E_REFCLK2P
AK38	GXBL1E_TX_CH1N
AK39	GXBL1E_TX_CH1P
AG32	GXBL1E_RX_CH1N, GXBL1E_REFCLK1N
AG33	GXBL1E_RX_CH1P, GXBL1E_REFCLK1P
AL36	GXBL1E_TX_CH0N
AL37	GXBL1E_TX_CH0P
AH34	GXBL1E_RX_CH0N, GXBL1E_REFCLK0N
AH35	GXBL1E_RX_CH0P, GXBL1E_REFCLK0P
AG29	REFCLK_GXBL1E_CHBP
AG28	REFCLK_GXBL1E_CHBN

Input signals (U23F):
- 39 PCIE_REFCLK_QR0_P
- 39 PCIE_REFCLK_QR0_N
- 10 PCIE_TX_N1
- 10 PCIE_TX_P1
- 10 PCIE_RX_N1
- 10 PCIE_RX_P1
- 10 PCIE_TX_N0
- 10 PCIE_TX_P0
- 10 PCIE_RX_N0
- 10 PCIE_RX_P0
- 11 ENETA_TX_N
- 11 ENETA_TX_P
- 11 ENETA_RX_N
- 11 ENETA_RX_P
- 12 ENETB_TX_N
- 12 ENETB_TX_P
- 12 ENETB_RX_N
- 12 ENETB_RX_P
- 40 CLK_ENET_FPGA_P
- 40 CLK_ENET_FPGA_N

PCIE Hard Core Channel 0, 1

A10SOC_1517

U23E — Tranceiver 1F BanK

Pin	Net
AA29	REFCLK_GXBL1F_CHTP
AA28	REFCLK_GXBL1F_CHTN
Y38	GXBL1F_TX_CH5N
Y39	GXBL1F_TX_CH5P
Y34	GXBL1F_RX_CH5N, GXBL1F_REFCLK5N
Y35	GXBL1F_RX_CH5P, GXBL1F_REFCLK5P
AA36	GXBL1F_TX_CH4N
AA37	GXBL1F_TX_CH4P
AA32	GXBL1F_RX_CH4N, GXBL1F_REFCLK4N
AA33	GXBL1F_RX_CH4P, GXBL1F_REFCLK4P
AB38	GXBL1F_TX_CH3N
AB39	GXBL1F_TX_CH3P
AB34	GXBL1F_RX_CH3N, GXBL1F_REFCLK3N
AB35	GXBL1F_RX_CH3P, GXBL1F_REFCLK3P
AC36	GXBL1F_TX_CH2N
AC37	GXBL1F_TX_CH2P
AB30	GXBL1F_RX_CH2N, GXBL1F_REFCLK2N
AB31	GXBL1F_RX_CH2P, GXBL1F_REFCLK2P
AD38	GXBL1F_TX_CH1N
AD39	GXBL1F_TX_CH1P
AC32	GXBL1F_RX_CH1N, GXBL1F_REFCLK1N
AC33	GXBL1F_RX_CH1P, GXBL1F_REFCLK1P
AE36	GXBL1F_TX_CH0N
AE37	GXBL1F_TX_CH0P
AD34	GXBL1F_RX_CH0N, GXBL1F_REFCLK0N
AD35	GXBL1F_RX_CH0P, GXBL1F_REFCLK0P
AC29	REFCLK_GXBL1F_CHBP
AC28	REFCLK_GXBL1F_CHBN

Input signals (U23E):
- 10 PCIE_TX_N7
- 10 PCIE_TX_P7
- 10 PCIE_RX_N7
- 10 PCIE_RX_P7
- 10 PCIE_TX_N6
- 10 PCIE_TX_P6
- 10 PCIE_RX_N6
- 10 PCIE_RX_P6
- 10 PCIE_TX_N5
- 10 PCIE_TX_P5
- 10 PCIE_RX_N5
- 10 PCIE_RX_P5
- 10 PCIE_TX_N4
- 10 PCIE_TX_P4
- 10 PCIE_RX_N4
- 10 PCIE_RX_P4
- 10 PCIE_TX_N3
- 10 PCIE_TX_P3
- 10 PCIE_RX_N3
- 10 PCIE_RX_P3
- 10 PCIE_TX_N2
- 10 PCIE_TX_P2
- 10 PCIE_RX_N2
- 10 PCIE_RX_P2

PCIE Hard Core with Channel 2,3,4,5,6,7

A10SOC_1517

U23D — Tranceiver 1G BanK

Pin	Net
U29	REFCLK_GXBL1G_CHTP
U28	REFCLK_GXBL1G_CHTN
P38	GXBL1G_TX_CH5N
P39	GXBL1G_TX_CH5P
T34	GXBL1G_RX_CH5N, GXBL1G_REFCLK5N
T35	GXBL1G_RX_CH5P, GXBL1G_REFCLK5P
R36	GXBL1G_TX_CH4N
R37	GXBL1G_TX_CH4P
U32	GXBL1G_RX_CH4N, GXBL1G_REFCLK4N
U33	GXBL1G_RX_CH4P, GXBL1G_REFCLK4P
T38	GXBL1G_TX_CH3N
T39	GXBL1G_TX_CH3P
V30	GXBL1G_RX_CH3N, GXBL1G_REFCLK3N
V31	GXBL1G_RX_CH3P, GXBL1G_REFCLK3P
U36	GXBL1G_TX_CH2N
U37	GXBL1G_TX_CH2P
V34	GXBL1G_RX_CH2N, GXBL1G_REFCLK2N
V35	GXBL1G_RX_CH2P, GXBL1G_REFCLK2P
V38	GXBL1G_TX_CH1N
V39	GXBL1G_TX_CH1P
W32	GXBL1G_RX_CH1N, GXBL1G_REFCLK1N
W33	GXBL1G_RX_CH1P, GXBL1G_REFCLK1P
W36	GXBL1G_TX_CH0N
W37	GXBL1G_TX_CH0P
Y30	GXBL1G_RX_CH0N, GXBL1G_REFCLK0N
Y31	GXBL1G_RX_CH0P, GXBL1G_REFCLK0P
W29	REFCLK_GXBL1G_CHBP
W28	REFCLK_GXBL1G_CHBN

Input signals (U23D):
- 40 REFCLK1_FMCB_P
- 40 REFCLK1_FMCB_N
- 43 FBD15C2MN
- 43 FBD15C2MP
- 43 FBD15M2CN
- 43 FBD15M2CP
- 18 FBD14C2MN
- 18 FBD14C2MP
- 18 FBD14M2CN
- 18 FBD14M2CP
- 18 FBD13C2MN
- 18 FBD13C2MP
- 18 FBD13M2CN
- 18 FBD13M2CP
- 43 FBD12C2MN
- 43 FBD12C2MP
- 18 FBD12M2CN
- 18 FBD12M2CP
- 18 FBD11C2MN
- 18 FBD11C2MP
- 18 FBD11M2CN
- 18 FBD11M2CP
- 43 FBD10C2MN
- 43 FBD10C2MP
- 18 FBD10M2CN
- 18 FBD10M2CP
- 18 FBGBTCLK1M2CP
- 18 FBGBTCLK1M2CN

A10SOC_1517

Application / Channel Table

Application	Channel (Bank, number)
PCIE RC	(1E,4);(1E,5);(1F,0);(1F,1); (1F,2);(1F,3);(1F,4);(1F,5)
FMC B Slot DP Transceiver [10:15]	(1G,0);(1G,1);(1G,2);(1G,3); (1G,4);(1G,5);
SGMII A and B	(1E,0);(1E,1)

DP & SDI & FMCA XCVRs & SMA XCVR

U23C — Tranceiver 1H BanK (A10SOC_1517)

Pin	Signal
N29	REFCLK_GXBL1H_CHTP
N28	REFCLK_GXBL1H_CHTN
H38	GXBL1H_TX_CH5N
H39	GXBL1H_TX_CH5P
M34	GXBL1H_RX_CH5N, GXBL1H_REFCLK5N
M35	GXBL1H_RX_CH5P, GXBL1H_REFCLK5P
J36	GXBL1H_TX_CH4N
J37	GXBL1H_TX_CH4P
N32	GXBL1H_RX_CH4N, GXBL1H_REFCLK4N
N33	GXBL1H_RX_CH4P, GXBL1H_REFCLK4P
K38	GXBL1H_TX_CH3N
K39	GXBL1H_TX_CH3P
P30	GXBL1H_RX_CH3N, GXBL1H_REFCLK3N
P31	GXBL1H_RX_CH3P, GXBL1H_REFCLK3P
L36	GXBL1H_TX_CH2N
L37	GXBL1H_TX_CH2P
P34	GXBL1H_RX_CH2N, GXBL1H_REFCLK2N
P35	GXBL1H_RX_CH2P, GXBL1H_REFCLK2P
M38	GXBL1H_TX_CH1N
M39	GXBL1H_TX_CH1P
R32	GXBL1H_RX_CH1N, GXBL1H_REFCLK1N
R33	GXBL1H_RX_CH1P, GXBL1H_REFCLK1P
N36	GXBL1H_TX_CH0N
N37	GXBL1H_TX_CH0P
T30	GXBL1H_RX_CH0N, GXBL1H_REFCLK0N
T31	GXBL1H_RX_CH0P, GXBL1H_REFCLK0P
R29	REFCLK_GXBL1H_CHBP
R28	REFCLK_GXBL1H_CHBN

Left-side signals (U23C):
- 17 FAGBTCLK0M2CP → N29
- 17 FAGBTCLK0M2CN → N28
- 17 FAD5C2MN → H38
- 17 FAD5C2MP → H39
- 17 FAD5M2CN → M34
- 17 FAD5M2CP → M35
- 17 FAD4C2MN → J36
- 17 FAD4C2MP → J37
- 17 FAD4M2CN → N32
- 17 FAD4M2CP → N33
- 17 FAD3C2MN → K38
- 17 FAD3C2MP → K39
- 17 FAD3M2CN → P30
- 17 FAD3M2CP → P31
- 17 FAD2C2MN → L36
- 17 FAD2C2MP → L37
- 17 FAD2M2CN → P34
- 17 FAD2M2CP → P35
- 17 FAD1C2MN → M38
- 17 FAD1C2MP → M39
- 17 FAD1M2CN → R32
- 17 FAD1M2CP → R33
- 17 FAD0C2MN → N36
- 17 FAD0C2MP → N37
- 17 FAD0M2CN → T30
- 17 FAD0M2CP → T31
- 17 FAGBTCLK1M2CP → R29
- 17 FAGBTCLK1M2CN → R28

U23B — Tranceiver 1I BanK (A10SOC_1517)

Pin	Signal
J29	REFCLK_GXBL1I_CHTP
J28	REFCLK_GXBL1I_CHTN
D34	GXBL1I_TX_CH5N
D35	GXBL1I_TX_CH5P
H34	GXBL1I_RX_CH5N, GXBL1I_REFCLK5N
H35	GXBL1I_RX_CH5P, GXBL1I_REFCLK5P
D38	GXBL1I_TX_CH4N
D39	GXBL1I_TX_CH4P
J32	GXBL1I_RX_CH4N, GXBL1I_REFCLK4N
J33	GXBL1I_RX_CH4P, GXBL1I_REFCLK4P
E36	GXBL1I_TX_CH3N
E37	GXBL1I_TX_CH3P
K30	GXBL1I_RX_CH3N, GXBL1I_REFCLK3N
K31	GXBL1I_RX_CH3P, GXBL1I_REFCLK3P
F34	GXBL1I_TX_CH2N
F35	GXBL1I_TX_CH2P
K34	GXBL1I_RX_CH2N, GXBL1I_REFCLK2N
K35	GXBL1I_RX_CH2P, GXBL1I_REFCLK2P
F38	GXBL1I_TX_CH1N
F39	GXBL1I_TX_CH1P
L32	GXBL1I_RX_CH1N, GXBL1I_REFCLK1N
L33	GXBL1I_RX_CH1P, GXBL1I_REFCLK1P
G36	GXBL1I_TX_CH0N
G37	GXBL1I_TX_CH0P
M30	GXBL1I_RX_CH0N, GXBL1I_REFCLK0N
M31	GXBL1I_RX_CH0P, GXBL1I_REFCLK0P
L29	REFCLK_GXBL1I_CHBP
L28	REFCLK_GXBL1I_CHBN

Left-side signals (U23B):
- 40 REFCLK_SMA_P → J29
- 40 REFCLK_SMA_N → J28
- SMA_XCVR_TX_N → D34
- SMA_XCVR_TX_P → D35
- SMA_XCVR_RX_N → H34
- SMA_XCVR_RX_P → H35
- 17 FAD9C2MN → E36
- 17 FAD9C2MP → E37
- 17 FAD9M2CN → K30
- 17 FAD9M2CP → K31
- 17 FAD8C2MN → F34
- 17 FAD8C2MP → F35
- 17 FAD8M2CN → K34
- 17 FAD8M2CP → K35
- 17 FAD7C2MN → F38
- 17 FAD7C2MP → F39
- 17 FAD7M2CN → L32
- 17 FAD7M2CP → L33
- 17 FAD6C2MN → G36
- 17 FAD6C2MP → G37
- 17 FAD6M2CN → M30
- 17 FAD6M2CP → M31
- 41 LMK_FMCCLK_P → L29
- 41 LMK_FMCCLK_N → L28

U23A — Tranceiver 1J BanK (A10SOC_1517)

2.00k R4079 → A28 RREF_TL

Pin	Signal
A28	RREF_TL
E29	REFCLK_GXBL1J_CHTP
E28	REFCLK_GXBL1J_CHTN
A32	GXBL1J_TX_CH5N
A33	GXBL1J_TX_CH5P
B30	GXBL1J_RX_CH5N, GXBL1J_REFCLK5N
B31	GXBL1J_RX_CH5P, GXBL1J_REFCLK5P
C32	GXBL1J_TX_CH4N
C33	GXBL1J_TX_CH4P
D30	GXBL1J_RX_CH4N, GXBL1J_REFCLK4N
D31	GXBL1J_RX_CH4P, GXBL1J_REFCLK4P
B34	GXBL1J_TX_CH3N
B35	GXBL1J_TX_CH3P
E32	GXBL1J_RX_CH3N, GXBL1J_REFCLK3N
E33	GXBL1J_RX_CH3P, GXBL1J_REFCLK3P
A36	GXBL1J_TX_CH2N
A37	GXBL1J_TX_CH2P
F30	GXBL1J_RX_CH2N, GXBL1J_REFCLK2N
F31	GXBL1J_RX_CH2P, GXBL1J_REFCLK2P
B38	GXBL1J_TX_CH1N
B39	GXBL1J_TX_CH1P
G32	GXBL1J_RX_CH1N, GXBL1J_REFCLK1N
G33	GXBL1J_RX_CH1P, GXBL1J_REFCLK1P
C36	GXBL1J_TX_CH0N
C37	GXBL1J_TX_CH0P
H30	GXBL1J_RX_CH0N, GXBL1J_REFCLK0N
H31	GXBL1J_RX_CH0P, GXBL1J_REFCLK0P
G29	REFCLK_GXBL1J_CHBP
G28	REFCLK_GXBL1J_CHBN

Left-side signals (U23A):
- 39 REFCLK_SDI_P → E29
- 39 REFCLK_SDI_N → E28
- 16 SDI_TX_N → A32
- 16 SDI_TX_P → A33
- 16 SDI_RX_N → B30
- 16 SDI_RX_P → B31
- 15 DP_ML_LANE_N0 → B34
- 15 DP_ML_LANE_P0 → B35
- 15 DP_ML_LANE_N1 → A36
- 15 DP_ML_LANE_P1 → A37
- 15 DP_ML_LANE_N2 → B38
- 15 DP_ML_LANE_P2 → B39
- 15 DP_ML_LANE_N3 → C36
- 15 DP_ML_LANE_P3 → C37
- 40 REFCLK_DP_P → G29
- 40 REFCLK_DP_N → G28

SMA Connectors

C43 0.1uF SMA_XCVR_RX_C_P
C42 0.1uF SMA_XCVR_RX_C_N

SMA Connector Interface: J6, J1
RX SMA Connector Interface: J21, J12

Application Table

Application	Channel (Bank, number)
SMA	(1I,5)
FMC A Slot DP Transceiver [0:9]	(1H,0);(1H,1);(1H,2);(1H,3]; (1H,4);(1H,5);(1I,0);(1I,1); (1I,2);(1I,3);
SDI	(1J,5)
Display Port	(1J,0);(1J,1);(1J,2);(1J,3)

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ALTERA

PCI Express GEN3 X 8 Connector

J57
PCIE-098-02-F-D-TH

B pin	Signal	Signal	A pin
B1	+12V	PRSNT1_N	A1
B2	+12V	+12V	A2
B3	+12V	+12V	A3
B4	+12V	GND	A4
B5	GND	JTAG_TCK	A5
B6	SMCLK	JTAG_TDI	A6
B7	SMDAT	JTAG_TDO	A7
B8	GND	JTAG_TMS	A8
B9	+3_3V	+3_3V	A9
B10	JTAG_TRSTN	+3_3V	A10
B11	+3_3VAUX	PERST_N	A11
	WAKE_N	KEY	
B12	RSVD1	GND	A12
B13	GND	REFCLK+	A13
B14	PET0P	REFCLK-	A14
B15	PET0N	GND	A15
B16	GND	PER0P	A16
B17	PRSNT2_N_X1	PER0N	A17
B18	GND	GND	A18
B19	PET1P	RSVD2	A19
B20	PET1N	GND	A20
B21	GND	PER1P	A21
B22	GND	PER1N	A22
B23	PET2P	GND	A23
B24	PET2N	GND	A24
B25	GND	PER2P	A25
B26	GND	PER2N	A26
B27	PET3P	GND	A27
B28	PET3N	GND	A28
B29	GND	PER3P	A29
B30	RSVD3	PER3N	A30
B31	PRSNT2_N_X4	GND	A31
B32	GND	RSVD4	A32
B33	PET4P	RSVD5	A33
B34	PET4N	GND	A34
B35	GND	PER4P	A35
B36	GND	PER4N	A36
B37	PET5P	GND	A37
B38	PET5N	GND	A38
B39	GND	PER5P	A39
B40	GND	PER5N	A40
B41	PET6P	GND	A41
B42	PET6N	GND	A42
B43	GND	PER6P	A43
B44	GND	PER6N	A44
B45	PET7P	GND	A45
B46	PET7N	GND	A46
B47	GND	PER7P	A47
B48	PRSNT2_N_X8	PER7N	A48
B49	GND	GND	A49

72 PCIE_DC_3V3

PCIE_DC_3V3

PCIE_12V   PCIE_12V

49 PCIE_12V

45 EXTA_SCL   R4165 DNI
13,17,45 EXTA_SDA   R4166 DNI

PCIE_aux3V3

69 PCIE_aux3V3   37 PCIE_TRSTN

36 PCIE_WAKE_N

PCIE_TCK   37
PCIE_TDI   37
PCIE_TDO   37
PCIE_TMS   37

PCIE_DC_3V3

R4163   4.7K

PCIE_PERSTn   35

PCIE_REFCLK_SYN_P   39
PCIE_REFCLK_SYN_N   39

8 PCIE_TX_P0   C1530 0.22uF   PCIE_TX_CP0
8 PCIE_TX_N0   C1531 0.22uF   PCIE_TX_CN0

PCIE_RX_P0   8
PCIE_RX_N0   8

8 PCIE_TX_P1   C1532 0.22uF   PCIE_TX_CP1
8 PCIE_TX_N1   C1533 0.22uF   PCIE_TX_CN1

PCIE_RX_P1   8
PCIE_RX_N1   8

8 PCIE_TX_P2   C1534 0.22uF   PCIE_TX_CP2
8 PCIE_TX_N2   C1535 0.22uF   PCIE_TX_CN2

PCIE_RX_P2   8
PCIE_RX_N2   8

8 PCIE_TX_P3   C1536 0.22uF   PCIE_TX_CP3
8 PCIE_TX_N3   C1537 0.22uF   PCIE_TX_CN3

PCIE_RX_P3   8
PCIE_RX_N3   8

8 PCIE_TX_P4   C1538 0.22uF   PCIE_TX_CP4
8 PCIE_TX_N4   C1539 0.22uF   PCIE_TX_CN4

PCIE_RX_P4   8
PCIE_RX_N4   8

8 PCIE_TX_P5   C1540 0.22uF   PCIE_TX_CP5
8 PCIE_TX_N5   C1541 0.22uF   PCIE_TX_CN5

PCIE_RX_P5   8
PCIE_RX_N5   8

8 PCIE_TX_P6   C1542 0.22uF   PCIE_TX_CP6
8 PCIE_TX_N6   C1543 0.22uF   PCIE_TX_CN6

PCIE_RX_P6   8
PCIE_RX_N6   8

8 PCIE_TX_P7   C1544 0.22uF   PCIE_TX_CP7
8 PCIE_TX_N7   C1545 0.22uF   PCIE_TX_CN7

PCIE_RX_P7   8
PCIE_RX_N7   8

35,36,37 PCIE_PRSNT2n

X1   X4   X8   KEY

75-ohm to 100-ohm XCVR traces.

PCIE_12V

C1546	C1547	C1548	C1549	C1550	C1551
22uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

PCIE_DC_3V3

C1552	C1553	C1554	C1555
0.1uF	0.1uF	0.1uF	100uF 6.3V

PCIE_aux3V3

C1556
0.1uF

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10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber

Place near 88E1111 PHY

SGMII Mode (default)

88E1111-B2-CAA1C000   EOL
88E1111-B2-NDC2C000   Replacement

U8A 88E1111
U8B 88E1111

DVDD = 1.0V
DVDD = 1.2V

ENET_DVDD = 1.0V/0.207A

LTC3025-1

U6 25.00MHz

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10/100/1000 Ethernet XCVR

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autosel, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber

U9A 88E1111

GMII / MII / RTBI INTERFACE

MDI INTERFACE

MGMT

TEST

SGMII INTERFACE

JTAG

Place near 88E1111 PHY

IO_1V8   36,37,68
IO_3V3   69
IO_2V5   36,68
IO_5V   50

C220 0.1uF   C263 0.1uF   C211 0.1uF   C218 0.1uF   C233 0.1uF   C247 0.1uF   C205 0.1uF   C217 0.1uF

SGMII Mode (default)

ENETB_TXC_P   C36 0.1uF   ENETB_TX_P 8
ENETB_TXC_N   C35 0.1uF   ENETB_TX_N 8
ENETB_RXC_P   C34 0.1uF   ENETB_RX_P 8
ENETB_RXC_N   C33 0.1uF   ENETB_RX_N 8

88E1111-B2-CAA1C000   EOL
88E1111-B2-NDC2C000   Replacement

U9B 88E1111

DVDD = 1.0V
DVDD = 1.2V

ENETB_DVDD

C264 0.1uF   C232 0.1uF   C231 0.1uF   C219 0.1uF   C248 0.1uF

D5 GREEN_LED   240 R343   ENETB_LED_TX
D2 GREEN_LED   240 R334   ENETB_LED_RX
D6 GREEN_LED   240 R344   ENEB_LED_LINK1000
D8 GREEN_LED   240 R352   ENETB_LED_LINK100
D10 GREEN_LED 240 R358   ENETB_LED_LINK10

U7 25.00MHz
EN VCC
GND OUT
R49 10K
C212 0.01uF

R322 4.99K   R323 4.7K

J3 7499111001A

U3 LTC3025-1
BIAS OUT
IN   ADJ
SHDN GND
EP_GND
C182 1uF
C8 10uF
R28 15K
R22
10K
C189 22uF   C188 2.2uF

ENET_DVDD = 1.0V/0.207A

R306 1.00K
R305 4.7K
R304 4.7K
R303 4.7K

ENETB_MDIO   27
ENETB_MDC   27
ENETB_INTn   36
ENETB_RESETn 36

ENETB_2p5V_RESETn
ENETB_2p5V_MDIO
ENETB_2p5V_MDC
ENETB_2p5V_INTn
ENETB_RSET

BMDI_P0 BMDI_N0
BMDI_P1 BMDI_N1
BMDI_P2 BMDI_N2
BMDI_P3 BMDI_N3

R44 49.9   R43 49.9   R307 49.9   R308 49.9   R42 49.9   R41 49.9   R40 49.9   R39 49.9
C195 0.01uF   C9 0.01uF   C196 0.01uF   C197 0.01uF

R331 0   R333 0

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ALTERA

Small Form Factor Pluggable Plus (SFP+) Port A

69 IO_3V3

IO_3V3

C269
0.1uF

C270
10uF

L19 1.0uH

SFPB_VCCT

C290
0.1uF

SFPA_VCCT

L20 1.0uH

SFPB_VCCR

SFPA_VCCR

C291
0.1uF

C298
10uF

Optical (SFP+) Transceiver Cage & Connector 0

J7

16	VCCT	TD_P	18
15	VCCR	TD_N	19
13	RD_P	RX_LOS	8
12	RD_N	TX_FAULT	2
3	TX_DISABLE	VEET	1
7	RS0	VEET	17
9	RS1	VEET	20
6	MOD_ABS	VEER	10
5	SCL	VEER	11
4	SDA	VEER	14
21	CAGE_GND	CAGE_GND	32
22	CAGE_GND	CAGE_GND	33
23	CAGE_GND	CAGE_GND	34
24	CAGE_GND	CAGE_GND	35
25	CAGE_GND	CAGE_GND	36
26	CAGE_GND	CAGE_GND	37
27	CAGE_GND	CAGE_GND	38
28	CAGE_GND	CAGE_GND	39
29	CAGE_GND	CAGE_GND	40
30	CAGE_GND	CAGE_GND	41
31	CAGE_GND	MH1	41
	CAGE_GND	MH2	42

SFP+_AND_CAGE

7 SFPA_RX_P
7 SFPA_RX_N

35 SFPA_TXDISABLE
35 SFPA_RATESEL0
35 SFPA_RATESEL1

35 SFPA_MOD0_PRSNTn
45 EXTA_SCL
10,17,45 EXTA_SDA

SFPA_TX_P 7
SFPA_TX_N 7

SFPA_LOS 35
SFPA_TXFAULT 35

B5

SFP+_CAGE

GND_CAGE

<Agile Part Number>

GND_CAGE

Optical (SFP) Transceiver Cage & Connector 1
I2C Address is 1010000 or 1010001.

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Small Form Factor Pluggable Plus (SFP+) Port B

69 IO_3V3

IO_3V3

C267 0.1uF
C268 10uF

L17 1.0uH

C288 0.1uF

SFPB_VCCT

SFPB_VCCT

L18 1.0uH

SFPB_VCCR

SFPB_VCCR

C289 0.1uF
C297 10uF

Optical (SFP+) Transceiver Cage & Connector 0

J8

Pin	Signal	Signal	Pin
16	VCCT	TD_P	18
15	VCCR	TD_N	19
13	RD_P	RX_LOS	8
12	RD_N	TX_FAULT	2
3	TX_DISABLE	VEET	1
7	RS0	VEET	17
9	RS1	VEET	20
6	MOD_ABS	VEER	10
5	SCL	VEER	11
4	SDA	VEER	14
21	CAGE_GND	CAGE_GND	32
22	CAGE_GND	CAGE_GND	33
23	CAGE_GND	CAGE_GND	34
24	CAGE_GND	CAGE_GND	35
25	CAGE_GND	CAGE_GND	36
26	CAGE_GND	CAGE_GND	37
27	CAGE_GND	CAGE_GND	38
28	CAGE_GND	CAGE_GND	39
29	CAGE_GND	CAGE_GND	40
30	CAGE_GND	CAGE_GND	41
31	CAGE_GND	MH1	41
	CAGE_GND	MH2	42

SFP+_AND_CAGE

7   SFPB_RX_P
7   SFPB_RX_N

35   SFPB_TXDISABLE
35   SFPB_RATESEL0
35   SFPB_RATESEL1

35   SFPB_MOD0_PRSNTn
18,45   EXTB_SCL
18,45   EXTB_SDA

SFPB_TX_P   7
SFPB_TX_N   7

SFPB_LOS   35
SFPB_TXFAULT   35

GND_CAGE   GND_CAGE

Optical (SFP) Transceiver Cage & Connector 1
I2C Address is 1010000 or 1010001.

B6

SFP+_CAGE

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Display Port (x4)

1) TX uses diff sstl18 configuration, which is able to meet peak-to-peak differential voltage and common mode voltage spec for DP.
2) RX uses LVDS input, but user need to ensure pin voltage at NF receiver end is <1.9v.
   a. If the channel is AC couple, then user need to choose the correct Vbias_RX so that Vpin < 1.9v. The spec is 0 - 2v, which is quite wide. Selecting Vbias_Rx at 2v region will cause NF device to have reliability issue.
   b. If the channel is DC couple, user need to make sure TX common mode voltage + ground reference differences between Tx and Rx will not cause Vpin for NF to be higher than 1.9v.

IO_3V3

R806   100K

C893
2.2uF

DP_3V3

U71
5 IN   OUT 4   1%
1 NC1   R802
6 NC2   SETI 3   280K
2 FLAG
7 ON   GND_PAD 9
8 GND

MAX14523B
0.5A maximum current

C888
0.1uF

36 DP_OCn
36 DP_ON

DP_3V3

C134   C133
0.1uF   0.1uF

82401646   82401646

D38 VDD GND IO6 IO5   VDD GND IO6 IO5 D37
8   7   6   5   8   7   6   5
IO1 IO2 IO3 IO4   IO1 IO2 IO3 IO4
1   2   3   4   1   2   3   4

DP_3V3

J46
20 DP_PWR   ML_LANE_0P 1   DP_ML_LANE_CP0   C854 0.1uF   DP_ML_LANE_P0   DP_ML_LANE_P0 9
                ML_LANE_0N 3   DP_ML_LANE_CN0   DP_ML_LANE_N0   DP_ML_LANE_N0 9
18 HP_DETECT
R792   100K DP_HOT_PLUG 19 RTN   ML_LANE_1P 4   DP_ML_LANE_CP1   C855 0.1uF   DP_ML_LANE_P1   DP_ML_LANE_P1 9
R793   0   DP_RTN   ML_LANE_1N 6   DP_ML_LANE_CN1   C856 0.1uF   DP_ML_LANE_N1   DP_ML_LANE_N1 9
R790   1M   DP_3p3V_CONFIG1 13 CONFIG1   ML_LANE_2P 7   DP_ML_LANE_CP2   C857 0.1uF   DP_ML_LANE_P2   DP_ML_LANE_P2 9
R791   1M   DP_3p3V_CONFIG2 14 CONFIG2   ML_LANE_2N 9   DP_ML_LANE_CN2   C858 0.1uF   DP_ML_LANE_N2   DP_ML_LANE_N2 9
2 GND   ML_LANE_3P 10 DP_ML_LANE_CP3   C859 0.1uF   DP_ML_LANE_P3   DP_ML_LANE_P3 9
8 GND   ML_LANE_3N 12 DP_ML_LANE_CN3   C860 0.1uF   DP_ML_LANE_N3   DP_ML_LANE_N3 9
11 GND   C2453 0.1uF
16 GND
              AUX_CH_P 15 DP_AUX_CP
              AUX_CH_N 17 DP_AUX_CN   Auxilary Channel -> Bidirctional LVDS 1Mbps/(720Mbps optional).
21 MH1   MH3 23
22 MH2   MH4 24   Quartus IO Standard = BLVDS
0472720024   TX -> DIFF SSTL-1.8
                             RX -> LVDS
                         FogBugz Case 135234 & 147387

36 DP_CONFIG1
36 DP_CONFIG2

1M   R765
R   GND_DP
4.7nF C878 GND_DP

GND_DP

IO_1V8   IO_3V3
                    IO_1V8 36,37,68
                    IO_3V3 69

IO_1V8
IO_3V3

Usually 3.3V for
DP, but Arria 10
is 1.8V LVDS.

DP_AUX_CP   C137 0.1uF

R223 R750   R224 100K   R216 49.9
10K   DNI

VBIAS_DP   DP_AUX_CHR_P R217 22.0   DP_AUX_CH_P 27
                                   DP_AUX_CHR_N R218 22.0   DP_AUX_CH_N 27

C848 C847 R220   DP_3V3   DNI R211
10uF 0.1uF 10K   DNI   DP_AUX_DE 36
                      R219 49.9   R212
              R225 100K
              C138 0.1uF   DP_AUX_D 36
                                   DP_AUX_CHB_P
                                   DP_AUX_CHB_N   DP_AUX_REn 36

36 DP_HOT_PLUG

U28
3 GND D+ 1
        D- 2
TPD2EUSB30   DP_AUX_R 36

U27
                        DE 3
6 A   D 4
7 B   RE_n 2
                R 1

IO_3V3

C830   8 VCC
0.1uF   5 GND

DNI

SDI Cable Driver, Equalizer, and SMB

SDI_SPI_CS0 36
SDI_SPI_MOSI 36
SDI_SPI_M1SO 36
SDI_SPI_CLK 36

75 Ohm Single-Ended Impedance

IO_2V5

SDI_AVDD

L11 120 Ohm FB

C846 C853 C871 C877
0.1uF 0.1uF 0.01uF 0.01uF

M22468 Pin compatible to:
M22428 (Gen2 3G/6G SDI Cable Driver)
M23428 (12G Cable Driver)

C155 4.7uF SDI_TXBNC_P 1

J48
HDBNC

2 3 4 5

100 Ohm Differential Impedance

SDI_AVDD

9 SDI_TX_P   C146 4.7uF

9 SDI_TX_N   C145 4.7uF

R230 DNI

U29

2	AVDD1	SDO1P	13
7	AVDD2	SDO1N	12

SDI_TXCAP_P 16 SDIP   SDO2P 11 SDI_TXDRV_P
SDI_TXCAP_N 1   SDIN   SDO2N 10 SDI_TXDRV_N

ENABLE Hardware Mode R229 10K 15 MODE_SEL

MF0 4
MF1 6
MF2 8
MF3 14

R749 10K SDI_AVDD
R226 10K

36 SDI_TX_SD_HDn   9 SD_xHD

R754 750 SDI_TX_RSET

5 RSET

AVSS 3
GNDPAD 17

M23428

Layout Notes:
DNI for resistors and
capacitors for GEN2
devices.
Minimize stubs in
layout.

Pull-down for 12G

Layout Notes (M23428) SDI Cable Driver:
- The RSET resistor should be located close to pin 5.
- Remove GND under pin 5 and the RSET resistor.
- The 49.9-ohm resistors should be placed close to device pins 16 and 1 (SDIP/SDIN).

C154 4.7uF R247 75

IO_2V5

IO_2V5 36,68

75 Ohm Single-Ended Impedance

L13 1nH
1 2

J49
HDBNC

1 SDI_IN_P1   SDI_EQIN_P   C158 4.7uF

R248 75

DNI for 12G

4.7uF for 12G

2.5V_SDI

M22544 Pin Compatible to:
M23544 (12G EQ + Reclocker)

2.5V_SDI

L12 120 Ohm FB IO_2V5

C852 C875 C876 C851
0.1uF 0.1uF 0.01uF 0.01uF

5 4 3 2

SDI_EQIN_N   C159 4.7uF

4.7uF for 12G

R237 DNI
R764 10K

U30

SDI CABLE EQUALIZER

SDI_EQIN_P1 3 SDIP   VCC 20
SDI_EQIN_N1 4 SDIN   VCC 24

2.5V_SDI

DISABLE SDO1 -> 7 SDO1_DISABLE

R235 75-ohm for 12G

36 SDI_XHD_RATE
36 SDI_MF4_status

8 MF4
9 SD_xHD

SDO0P 15 SDO_P
SDO0N 14 SDO_N

C135 4.7uF SDI_RX_P 9
C136 4.7uF SDI_RX_N 9

MUTEREF 11 MUTEREF

SDO1N 17
SDO1P 18

100 Ohm Differential Impedance

MODE_SEL = 0 -> HARDWARE MODE

R748 DNI   R236 10K MODE_SEL 6 MODE_SEL

36 SDI_MF0_BYPASS_present
36 SDI_MF1_SLEEP_MISO
36 SDI_MF2_MUTE_SCLK
36 SDI_MF3_MOSI

MF0_BYPASS 10 MF0
MF1_AUTO_SLEEP 19 MF1
MF2_MUTE 21 MF2
MF3_xSD 22 MF3

R753 0

VEE 1
VICM 5
VEE 12
VEE 16
VEE 23
VEE 25

C157 1uF
C156 10uF

1uF and 10uF for 12G

D39
GREEN_LED

36 SDI_xCS_CS

R222 49.9

13 xCS

VEE_PAD

M23544

2.5V_SDI

R221 DNI

Layout Notes (M22544) SDI Cable Equalizer:
- The AGC 33nF capacitor should be located close to the device pins 8 and 9 (AGC+/AGC-).
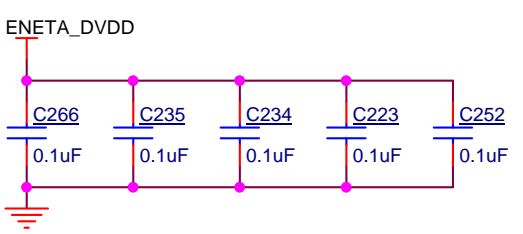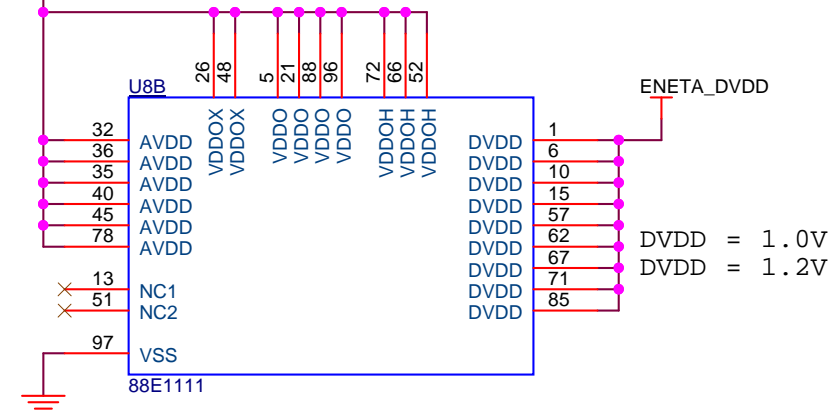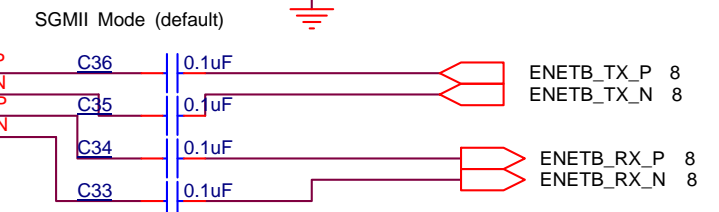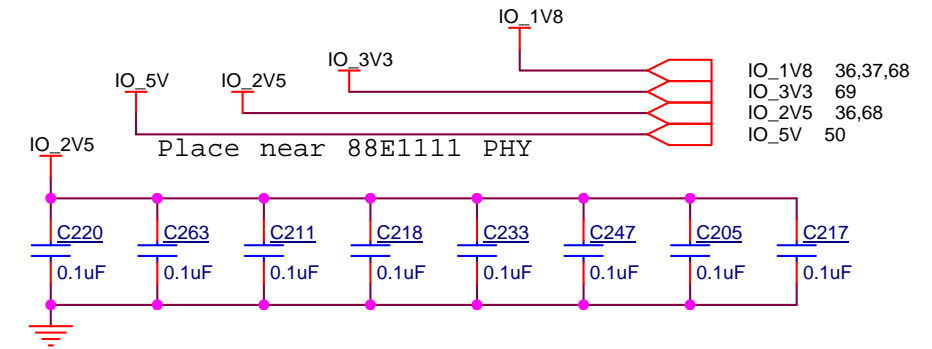- Clear GND under the AGC 33nF capacitor.

Altera Corporation,101 innovation Dr, San Jose, CA 95134

Title: **Arria 10 SoC FPGA Development Kit Board**

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Size: B
Document Number: 150-0321308 (6XX-44382R)
Rev: C

Date: Thursday, March 31, 2016
Sheet 16 of 78

FMC (V57.1) PORT A

Title: Arria 10 SoC FPGA Development Kit Board

Size: B
Document Number: 150-0321308 (6XX-44382R)
Rev: C
Date: Thursday, March 31, 2016 Sheet 17 of 78

J29A — ASP-134486-01

28 FALAP0	G6	LA_P0_CC	LA_P16	G18	FALAP16 28
28 FALAN0	G7	LA_N0_CC	LA_N16	G19	FALAN16 28
43 FALAP1	D8	LA_P1_CC	LA_P17	D20	FALAP17 28
43 FALAN1	D9	LA_N1_CC	LA_N17	D21	FALAN17 28
28 FALAP2	H7	LA_P2	LA_P18_CC	C22	FALAP18 28
28 FALAN2	H8	LA_N2	LA_N18_CC	C23	FALAN18 28
28 FALAP3	G9	LA_P3	LA_P19	H22	FALAP19 28
28 FALAN3	G10	LA_N3	LA_N19	H23	FALAN19 28
28 FALAP4	H10	LA_P4	LA_P20	G21	FALAP20 28
43 FALAN4	H11	LA_N4	LA_N20	G22	FALAN20 28
43 FALAP5	D11	LA_P5	LA_P21	H25	FALAP21 28
43 FALAN5	D12	LA_N5	LA_N21	H26	FALAN21 28
28 FALAP6	C10	LA_P6	LA_P22	G24	FALAP22 28
28 FALAN6	C11	LA_N6	LA_N22	G25	FALAN22 28
28 FALAP7	H13	LA_P7	LA_P23	D23	FALAP23 29
28 FALAN7	H14	LA_N7	LA_N23	D24	FALAN23 29
28 FALAP8	G12	LA_P8	LA_P24	H28	FALAP24 29
28 FALAN8	G13	LA_N8	LA_N24	H29	FALAN24 29
28 FALAP9	D14	LA_P9	LA_P25	G27	FALAP25 29
28 FALAN9	D15	LA_N9	LA_N25	G28	FALAN25 29
28 FALAP10	C14	LA_P10	LA_P26	D26	FALAP26 29
28 FALAN10	C15	LA_N10	LA_N26	D27	FALAN26 29
28 FALAP11	H16	LA_P11	LA_P27	C26	FALAP27 29
28 FALAN11	H17	LA_N11	LA_N27	C27	FALAN27 29
28 FALAP12	G15	LA_P12	LA_P28	H31	FALAP28 29
28 FALAN12	G16	LA_N12	LA_N28	H32	FALAN28 29
28 FALAP13	D17	LA_P13	LA_P29	G30	FALAP29 29
28 FALAN13	D18	LA_N13	LA_N29	G31	FALAN29 29
28 FALAP14	C18	LA_P14	LA_P30	H34	FALAP30 29
28 FALAN14	C19	LA_N14	LA_N30	H35	FALAN30 29
28 FALAP15	H19	LA_P15	LA_P31	G33	FALAP31 29
28 FALAN15	H20	LA_N15	LA_N31	G34	FALAN31 29
			LA_P32	H37	FALAP32 29
			LA_N32	H38	FALAN32 29
			LA_P33	G36	FALAP33 29
			LA_N33	G37	FALAN33 29

J29C — ASP-134486-01 (HB bus, FAHBP/FAHBN signals)

J29B — ASP-134486-01 (HA bus, FAHAP/FAHAN signals)

J29D — ASP-134486-01

9 FAD0C2MP	C2	DP0_C2M_P	DP0_M2C_P	C6	FAD0M2CP 9
9 FAD0C2MN	C3	DP0_C2M_N	DP0_M2C_N	C7	FAD0M2CN 9
9 FAD1C2MP	A22	DP1_C2M_P	DP1_M2C_P	A2	FAD1M2CP 9
9 FAD1C2MN	A23	DP1_C2M_N	DP1_M2C_N	A3	FAD1M2CN 9
9 FAD2C2MP	A26	DP2_C2M_P	DP2_M2C_P	A6	FAD2M2CP 9
9 FAD2C2MN	A27	DP2_C2M_N	DP2_M2C_N	A7	FAD2M2CN 9
9 FAD3C2MP	A30	DP3_C2M_P	DP3_M2C_P	A10	FAD3M2CP 9
9 FAD3C2MN	A31	DP3_C2M_N	DP3_M2C_N	A11	FAD3M2CN 9
9 FAD4C2MP	A34	DP4_C2M_P	DP4_M2C_P	A14	FAD4M2CP 9
9 FAD4C2MN	A35	DP4_C2M_N	DP4_M2C_N	A15	FAD4M2CN 9
9 FAD5C2MP	A38	DP5_C2M_P	DP5_M2C_P	A18	FAD5M2CP 9
9 FAD5C2MN	A39	DP5_C2M_N	DP5_M2C_N	A19	FAD5M2CN 9
9 FAD6C2MP	B36	DP6_C2M_P	DP6_M2C_P	B16	FAD6M2CP 9
9 FAD6C2MN	B37	DP6_C2M_N	DP6_M2C_N	B17	FAD6M2CN 9
9 FAD7C2MP	B32	DP7_C2M_P	DP7_M2C_P	B12	FAD7M2CP 9
9 FAD7C2MN	B33	DP7_C2M_N	DP7_M2C_N	B13	FAD7M2CN 9
9 FAD8C2MP	B28	DP8_C2M_P	DP8_M2C_P	B8	FAD8M2CP 9
9 FAD8C2MN	B29	DP8_C2M_N	DP8_M2C_N	B9	FAD8M2CN 9
9 FAD9C2MP	B24	DP9_C2M_P	DP9_M2C_P	B4	FAD9M2CP 9
9 FAD9C2MN	B25	DP9_C2M_N	DP9_M2C_N	B5	FAD9M2CN 9
	D4	GBTCLK0_M2C_P			FAGBTCLK0M2CP 9
	D5	GBTCLK0_M2C_N			FAGBTCLK0M2CN 9
	B20	GBTCLK1_M2C_P			FAGBTCLK1M2CP 9
	B21	GBTCLK1_M2C_N			FAGBTCLK1M2CN 9

J29E — ASP-134486-01

FMCA_aux3V3	D32	3P3VAUX	VADJ	E39	
65 FMCA_aux3V3			VADJ	F40	FMCAVADJ 66
72 FMCA_DC_3V3	D40	3P3V	VADJ	G39	
	C39	3P3V	VADJ	H40	
FMCA_DC_3V3	D36	3P3V			
	D38	3P3V	VIO_B_M2C	K40	FAM2CVIO 36
			VIO_B_M2C	J39	
FMCA_12V	C35	12P0V	VREF_B_M2C	K1	FAREFB
FMCA_12V	C37	12P0V	VREF_A_M2C	H1	FAREFA
FAPG_C2M	D1	PG_C2M	PG_M2C	F1	FAM2CPgood 35
35,36,38,42 FAPRSNT_N	H2	PRSNT_M2C_L			
10,13,45 EXTA_SDA	C31	SDA	TRST	D34	FATRST 37
45 EXTA_SCL	C30	SCL	TMS	D33	FATMS 37
			TDO	D31	FATDO 37
43 FACLK2BIDIRP	K4	CLK2_BIDIR_P	TDI	D30	FATDI 37
43 FACLK2BIDIRN	K5	CLK2_BIDIR_N	TCK	D29	FATCK 37
43 FACLK3BIDIRP	J2	CLK3_BIDIR_PCLK0_M2C_P	H4	FACLK0M2CP 43
43 FACLK3BIDIRN	J3	CLK3_BIDIR_NCLK0_M2C_N	H5	FACLK0M2CN 43
		CLK1_M2C_P	G2	FACLK1M2CP 43
36 FACLKDIR	B1	CLK_DIR	CLK1_M2C_N	G3	FACLK1M2CN 43
	C34	GA0	RES0	B40	
	D35	GA1			

J29F — ASP-134486-01 (GND pins)

Capacitors:
C503 1uF — FAREFA
C502 1uF — FAREFB
C825 10uF, C816 10uF — FAM2CVIO
C2388 10uF — FMCA_aux3V3
C813 10uF — FMCA_DC_3V3
C784 1uF — FMCA_12V
C815 10uF, C814 10uF — FMCAVADJ

R5517
R5382 1.00K
R5378 1.00k R690 DNI 100K
R704 DNI R5381 1.00K
35 FAC2MPgood DNI R5518

I2C ADDRESS: b'10100010

FMC (16 XCVRS + LAP) PORT B

This page is a hardware schematic diagram (Sheet 18 of 78). It consists of connector symbols (J19A, J19B, J19C, J19D, J19E, J19F — all ASP-134486-01), signal nets, capacitors, and resistors.

J19A (ASP-134486-01)

Net	Pin	Signal	Signal	Pin	Net
30 FBLAP0	G6	LA_P0_CC	LA_P16	G18	FBLAP16 30
30 FBLAN0	G7	LA_N0_CC	LA_N16	G19	FBLAN16 30
43 FBLAP1	D8	LA_P1_CC	LA_P17	D20	FBLAP17 30
43 FBLAN1	D9	LA_N1_CC	LA_N17	D21	FBLAN17 30
30 FBLAP2	H7	LA_P2	LA_P18_CC	C22	FBLAP18 30
30 FBLAN2	H8	LA_N2	LA_N18_CC	C23	FBLAN18 30
30 FBLAP3	G9	LA_P3	LA_P19	H22	FBLAP19 30
30 FBLAN3	G10	LA_N3	LA_N19	H23	FBLAN19 30
30 FBLAP4	H10	LA_P4	LA_P20	G21	FBLAP20 29
30 FBLAN4	H11	LA_N4	LA_N20	G22	FBLAN20 29
43 FBLAP5	D11	LA_P5	LA_P21	H25	FBLAP21 29
43 FBLAN5	D12	LA_N5	LA_N21	H26	FBLAN21 29
30 FBLAP6	C10	LA_P6	LA_P22	G24	FBLAP22 29 43
30 FBLAN6	C11	LA_N6	LA_N22	G25	FBLAN22 29 43
30 FBLAP7	H13	LA_P7	LA_P23	D23	FBLAP23 29
30 FBLAN7	H14	LA_N7	LA_N23	D24	FBLAN23 29
30 FBLAP8	G12	LA_P8	LA_P24	H28	FBLAP24 29
30 FBLAN8	G13	LA_N8	LA_N24	H29	FBLAN24 29
30 FBLAP9	D14	LA_P9	LA_P25	G27	FBLAP25 29
30 FBLAN9	D15	LA_N9	LA_N25	G28	FBLAN25 29
30 FBLAP10	C14	LA_P10	LA_P26	D26	FBLAP26 29 8
30 FBLAN10	C15	LA_N10	LA_N26	D27	FBLAN26 29 8
30 FBLAP11	H16	LA_P11	LA_P27	C26	FBLAP27 29
30 FBLAN11	H17	LA_N11	LA_N27	C27	FBLAN27 29
30 FBLAP12	G15	LA_P12	LA_P28	H31	FBLAP28 36
30 FBLAN12	G16	LA_N12	LA_N28	H32	FBLAN28 36
30 FBLAP13	D17	LA_P13	LA_P29	G30	FBLAP29 36
30 FBLAN13	D18	LA_N13	LA_N29	G31	FBLAN29 36
30 FBLAP14	C18	LA_P14	LA_P30	H34	FBLAP30 36
30 FBLAN14	H19	LA_N14	LA_N30	H35	FBLAN30 36 8
30 FBLAP15	H19	LA_P15	LA_P31	G33	FBLAP31 36 8
30 FBLAN15	H20	LA_N15	LA_N31	G34	FBLAN31 36
			LA_P32	H37	FBLAP32 36
			LA_N32	H38	FBLAN32 36
			LA_P33	G36	FBLAP33 36
			LA_N33	G37	FBLAN33 36

J19C (ASP-134486-01)

FBD11C2MP C358 0.1uF FBT11P K25 HB_P0_CC HB_P11 J30
FBD11C2MN C359 0.1uF FBT11N K26 HB_N0_CC HB_N11 J31
HB_P1 J24 ... HB_N12 F32
HB_N1 J25 ... HB_P12 F31
HB_P2 F22 ... HB_P13 E30
HB_N2 F23 ... HB_N13 E31
HB_P3 E21 K34 FBT14P C406 0.1uF FBD14C2MP 8
HB_N3 E22 K35 FBT14N C416 0.1uF FBD14C2MN 8
HB_P4 F25 ... HB_P15 J33
HB_N4 F26 ... HB_N15 J34
HB_P5 E24 ... HB_P16 F34
HB_N5 E23 ... HB_N16 F34
FBHA_P6M FBT12P K28 HB_P6_CC HB_P17_CC K37 FBT15P FBHA_P17M 43
FBHA_N6M FBT12N K29 HB_N6_CC HB_N17_CC K38 FBT15N FBHA_N17M 43
HB_P7 J27 ... HB_P18 J36 FBHBP18 36
HB_N7 J28 ... HB_N18 J37 FBHBN18 36
HB_P8 F28 ... HB_P19 E33 FBHBP19 36
HB_N8 F29 ... HB_N19 E34 FBHBN19 36
HB_P9 E27 ... HB_P20 F37 FBHBP20 36
HB_N9 E28 ... HB_N20 E36 FBHBN20 36
FBD13C2MP C393 0.1uF FBT13P K31 HB_P10 HB_P21 E37 FBHBP21 36
FBD13C2MN C394 0.1uF FBT13N K32 HB_N10 HB_N21 FBHBN21 36

J19B (ASP-134486-01)

HA_P0_CC HA_P12 F13
HA_N0_CC HA_N12 F14
HA_P1_CC HA_P13 E12
HA_N1_CC HA_N13 E13
HA_P2 HA_P14 J15
HA_N2 HA_N14 J16
HA_P3 HA_P15 F16
HA_N3 HA_N15 F17
HA_P4 HA_N16 E16
HA_N4 HA_P16 E15
HA_P5 HA_P17_CC K16 FBR14P C319 0.1uF FBD14M2CP 8
HA_N5 HA_N17_CC K17 FBR14N C329 0.1uF FBD14M2CN 8
HA_P6 HA_P18 J18
HA_N6 HA_N18 J19
HA_P7 HA_P19 F19 FMB_SYNC_CD 30
HA_N7 HA_N19 F20 FMB_SYNC_AB 30
30 FMB_SYNCP F10 HA_P8 HA_P20 E18
30 FMB_SYNCN F11 HA_N8 HA_N20 E19 FBHA_P20 29
HA_P9 E9 HA_P21 K19 FBR15P FBHA_N20 29
HA_N9 E10 HA_N21 K20 FBR15N FBHA_P21M 43
C313 0.1uF FBR13P K13 HA_P10 HA_P22 J21 FBHA_N21M 43
C318 0.1uF FBR13N K14 HA_N10 HA_N22 J22 FBHA_P22 29
HA_P11 J12 HA_P23 K22 FBT10P FBHA_N22 29
HA_N11 J13 HA_N23 K23 FBT10N FBHA_P23M 43
FBD12M2CP C301 0.1uF FBR12P K10 FBHA_N23M 43
FBD12M2CN C308 0.1uF FBR12N K11

FBD11M2CP C284 0.1uF FBR11P K7
FBD11M2CN C292 0.1uF FBR11N K8

FBD13M2CP C313 0.1uF FBR13P K13
FBD13M2CN C318 0.1uF FBR13N K14

J19D (ASP-134486-01)

Net	Pin	Signal	Signal	Pin	Net
7 FBD0C2MP	C2	DP0_C2M_P	DP0_M2C_P	C6	FBD0M2CP 7
7 FBD0C2MN	C3	DP0_C2M_N	DP0_M2C_N	C7	FBD0M2CN 7
7 FBD1C2MP	A22	DP1_C2M_P	DP1_M2C_P	A2	FBD1M2CP 7
7 FBD1C2MN	A23	DP1_C2M_N	DP1_M2C_N	A3	FBD1M2CN 7
7 FBD2C2MP	A26	DP2_C2M_P	DP2_M2C_P	A6	FBD2M2CP 7
7 FBD2C2MN	A27	DP2_C2M_N	DP2_M2C_N	A7	FBD2M2CN 7
7 FBD3C2MP	A30	DP3_C2M_P	DP3_M2C_P	A10	FBD3M2CP 7
7 FBD3C2MN	A31	DP3_C2M_N	DP3_M2C_N	A11	FBD3M2CN 7
7 FBD4C2MP	A34	DP4_C2M_P	DP4_M2C_P	A14	FBD4M2CP 7
7 FBD4C2MN	A35	DP4_C2M_N	DP4_M2C_N	A15	FBD4M2CN 7
7 FBD5C2MP	A38	DP5_C2M_P	DP5_M2C_P	A18	FBD5M2CP 7
7 FBD5C2MN	A39	DP5_C2M_N	DP5_M2C_N	A19	FBD5M2CN 7
7 FBD6C2MP	B36	DP6_C2M_P	DP6_M2C_P	B16	FBD6M2CP 7
7 FBD6C2MN	B37	DP6_C2M_N	DP6_M2C_N	B17	FBD6M2CN 7
7 FBD7C2MP	B32	DP7_C2M_P	DP7_M2C_P	B12	FBD7M2CP 7
7 FBD7C2MN	B33	DP7_C2M_N	DP7_M2C_N	B13	FBD7M2CN 7
7 FBD8C2MP	B28	DP8_C2M_P	DP8_M2C_P	B8	FBD8M2CP 7
7 FBD8C2MN	B29	DP8_C2M_N	DP8_M2C_N	B9	FBD8M2CN 7
7 FBD9C2MP	B24	DP9_C2M_P	DP9_M2C_P	B4	FBD9M2CP 7
7 FBD9C2MN	B25	DP9_C2M_N	DP9_M2C_N	B5	FBD9M2CN 7
	D4	GBTCLK0_M2C_P			FBGBTCLK0M2CP 7
	D5	GBTCLK0_M2C_N			FBGBTCLK0M2CN 7
	B20	GBTCLK1_M2C_P			FBGBTCLK1M2CP 8
	B21	GBTCLK1_M2C_N			FBGBTCLK1M2CN 8

J19E (ASP-134486-01)

FMCB_aux3V3 D32 3P3VAUX VADJ E39 FMCBVADJ 67
65 FMCB_aux3V3 D40 3P3V VADJ F40
72 FMCB_DC_3V3 C39 3P3V VADJ G39
FMCB_DC_3V3 D36 3P3V VADJ H40
D38 3P3V VIO_B_M2C K40 FBM2CVIO
VIO_B_M2C J39 FBM2CVIO 36
49 FMCB_12V C35 12P0V VREF_B_M2C K1
FMCB_12V C37 12P0V VREF_A_M2C H1 FBREFA
FBPG_C2M D1 PG_C2M PG_M2C F1
35,36,38,42 FBPRSNT_N H2 PRSNT_M2C_L TRST D34 FBTRST 37
14,45 EXTB_SDA C31 SDA TMS D33 FBTMS 37
14,45 EXTB_SCL C30 SCL TDO D31 FBTDO 37
TDI D30 FBTDI 37
8 FBD10M2CP C274 0.1uF FBR10P K4 CLK2_BIDIR_P TCK D29 FBTCK 37
8 FBD10M2CN C283 0.1uF FBR10N K5 CLK2_BIDIR_N
J2 CLK3_BIDIR_PCLK0_M2C_P H4 FBCLK0M2CP 30
J3 CLK3_BIDIR_NCLK0_M2C_N H5 FBCLK0M2CN 30
B1 CLK1_M2C_P G2 FBCLK1M2CP 43
CLK_DIR CLK1_M2C_N G3 FBCLK1M2CN 43
C34 GA0 RES0 B40
D35 GA1

Resistors (lower left)

R5359 1.00k
R5519
R5355 1.00k
R457 DNI
100K
R464 DNI
R5358 1.00k
35 FBC2MPgood DNI R5520

FMCB_aux3V3
FMCB_DC_3V3

J19F (ASP-134486-01) — GND connector

(Two columns of GND pins, left-side pins E20–C33 and right-side pins E17–C36, all connected to GND.)

FMCBVADJ C446 10uF C447 10uF
FBREFA C238 1uF
FMCB_aux3V3 C405 10uF
FMCB_DC_3V3 C434 10uF
FMCB_12V C424 1uF
FBM2CVIO C466 10uF C448 10uF

HPS HILO DDR3/DDR4 IOs

U23J — IO BANK 2K, HPS Memory BANK

Signal	Pin	IO Description
24 HMEM_DQ_ADDR_CMD0	P25	IO, LVDS2K_1N, DQ4L
24 HMEM_DQ_ADDR_CMD3	N25	IO, LVDS2K_1P, DQ4L
24 HMEM_DQ_ADDR_CMD4	L26	IO, LVDS2K_2N, DQ4L
24 HMEM_DQ_ADDR_CMD2	K26	IO, LVDS2K_2P, DQ4L
24 HMEM_DQ_ADDR_CMD1	M25	IO, LVDS2K_3N, DQ4L
24 HMEM_DQ_ADDR_CMD5	L25	IO, LVDS2K_3P, DQ4L
24 HMEM_DQS_ADDR_CMD_N	L24	IO, LVDS2K_4N, DQSN4L
24 HMEM_DQS_ADDR_CMD_P	K25	IO, LVDS2K_4P, DQS4L
24 HMEM_DQ_ADDR_CMD6	N24	IO, LVDS2K_5N, DQ4L
24 HMEM_DQ_ADDR_CMD7	M24	IO, LVDS2K_5P, DQ4L
24 HMEM_DQ_ADDR_CMD8	J25	IO, LVDS2K_6N, DQ4L
	J26	IO, LVDS2K_6P, DQ4L
24 HMEM_ADDR_CMD18	J24	IO, LVDS2K_7N, DQ5L
24 HMEM_ADDR_CMD17	H24	IO, LVDS2K_7P, DQ5L
24 HMEM_ADDR_CMD16	E25	IO, LVDS2K_8N, DQ5L
24 HMEM_ADDR_CMD19	D25	IO, LVDS2K_8P, DQ5L
24 HMEM_ADDR_CMD26	F23	IO, LVDS2K_9N, DQ5L
24 HMEM_ADDR_CMD15	F24	IO, LVDS2K_9P, DQ5L
24 HMEM_ADDR_CMD14	G25	IO, PLL_2K_CLKOUT1N, LVDS2K_10N, DQSN5L
24 HMEM_ADDR_CMD13	G26	IO, PLL_2K_CLKOUT1P, PLL_2K_CLKOUT1, PLL_2K_FB1, LVDS2K_10P, DQS5L
24 HMEM_ADDR_CMD12	F26	IO, LVDS2K_11N, DQ5L
	E26	IO, RZQ_2K, LVDS2K_11P, DQ5L
	G24	IO, CLK_2K_1N, LVDS2K_12N, DQ5L
	F25	IO, CLK_2K_1P, LVDS2K_12P, DQ5L
24 HMEM_ADDR_CMD11	D24	IO, CLK_2K_0N, LVDS2K_13N, DQ6L
24 HMEM_ADDR_CMD10	C24	IO, CLK_2K_0P, LVDS2K_13P, DQ6L
24 HMEM_ADDR_CMD9	E23	IO, LVDS2K_14N, DQ6L
24 HMEM_ADDR_CMD8	D23	IO, LVDS2K_14P, DQ6L
24 HMEM_ADDR_CMD7	C23	IO, PLL_2K_CLKOUT0N, LVDS2K_15N, DQ6L
24 HMEM_ADDR_CMD6	B22	IO, PLL_2K_CLKOUT0P, PLL_2K_CLKOUT0, PLL_2K_FB0, LVDS2K_15P, DQ6L
24 HMEM_ADDR_CMD5	B24	IO, LVDS2K_16N, DQSN6L
24 HMEM_ADDR_CMD4	C25	IO, LVDS2K_16P, DQS6L
24 HMEM_ADDR_CMD3	C21	IO, LVDS2K_17N, DQ6L
24 HMEM_ADDR_CMD2	C22	IO, LVDS2K_17P, DQ6L
24 HMEM_ADDR_CMD1	C26	IO, LVDS2K_18N, DQ6L
24 HMEM_ADDR_CMD0	B26	IO, LVDS2K_18P, DQ6L
24 HMEM_ADDR_CMD31	A18	IO, LVDS2K_19N, DQ7L
24 HMEM_ADDR_CMD30	A17	IO, LVDS2K_19P, DQ7L
24 HMEM_CLK_N	B19	IO, LVDS2K_20N, DQ7L
24 HMEM_CLK_P	B20	IO, LVDS2K_20P, DQ7L
24 HMEM_ADDR_CMD21	A23	IO, LVDS2K_21N, DQ7L
24 HMEM_ADDR_CMD20	A24	IO, LVDS2K_21P, DQ7L
24 HMEM_ADDR_CMD25	A25	IO, LVDS2K_22N, DQSN7L
24 HMEM_ADDR_CMD24	A26	IO, LVDS2K_22P, DQS7L
24 HMEM_ADDR_CMD23	B21	IO, LVDS2K_23N, DQ7L
24 HMEM_ADDR_CMD22	A22	IO, LVDS2K_23P, DQ7L
24 HMEM_ADDR_CMD27	A19	IO, LVDS2K_24N, DQ7L
24 HMEM_ADDR_CMD28	A20	IO, LVDS2K_24P, DQ7L

RZQ_2K
R654 240

IO BANK 2K, HPS Memory BANK

A10SOC_1517

U23K — IO BANK 2J, HPS Memory BANK

Signal	Pin	IO Description
24 HPSMEM_DMA0	AV26	IO, LVDS2J_1N, DQ8L
24 HMEM_DQA4	AV27	IO, LVDS2J_1P, DQ8L
24 HMEM_DQA5	AU27	IO, LVDS2J_2N, DQ8L
24 HMEM_DQA6	AU28	IO, LVDS2J_2P, DQ8L
24 HMEM_DQA1	AV28	IO, LVDS2J_3N, DQ8L
24 HMEM_DQA0	AW28	IO, LVDS2J_3P, DQ8L
24 HMEM_DQSA_N0	AW25	IO, LVDS2J_4N, DQSN8L
24 HMEM_DQSA_P0	AW26	IO, LVDS2J_4P, DQS8L
24 HMEM_DQA2	AV24	IO, LVDS2J_5N, DQ8L
24 HMEM_DQA3	AW24	IO, LVDS2J_5P, DQ8L
24 HMEM_DQA7	AV23	IO, LVDS2J_6N, DQ8L
	AW23	IO, LVDS2J_6P, DQ8L
24 HPSMEM_DMA1	AU25	IO, LVDS2J_7N, DQ9L
24 HMEM_DQA8	AU26	IO, LVDS2J_7P, DQ9L
24 HMEM_DQA11	AR26	IO, LVDS2J_8N, DQ9L
24 HMEM_DQA10	AT26	IO, LVDS2J_8P, DQ9L
24 HMEM_DQA14	AT23	IO, LVDS2J_9N, DQ9L
24 HMEM_DQA12	AU24	IO, LVDS2J_9P, DQ9L
24 HMEM_DQSA_N1	AT24	IO, PLL_2J_CLKOUT1N, LVDS2J_10N, DQSN9L
24 HMEM_DQSA_P1	AT25	IO, PLL_2J_CLKOUT1P, PLL_2J_CLKOUT1, PLL_2J_FB1, LVDS2J_10P, DQS9L
24 HMEM_DQA13	AP25	IO, LVDS2J_11N, DQ9L
24 HMEM_DQA9	AR25	IO, RZQ_2J, LVDS2J_11P, DQ9L
24 HMEM_DQA15	AR25	IO, CLK_2J_1N, LVDS2J_12N, DQ9L
	AP23	IO, CLK_2J_1P, LVDS2J_12P, DQ9L
	AP24	IO, CLK_2J_0N, LVDS2J_13N, DQ10L
24 HPSMEM_DMA2	AN26	IO, CLK_2J_0P, LVDS2J_13P, DQ10L
24 HMEM_DQA22	AP26	IO, LVDS2J_14N, DQ10L
24 HMEM_DQA17	AN23	IO, LVDS2J_14P, DQ10L
24 HMEM_DQA18	AN24	IO, PLL_2J_CLKOUT0N, LVDS2J_15N, DQ10L
24 HMEM_DQA19	AK26	IO, PLL_2J_CLKOUT0P, PLL_2J_CLKOUT0, PLL_2J_FB0, LVDS2J_15P, DQ10L
24 HMEM_DQA16	AL26	IO, LVDS2J_16N, DQSN10L
24 HMEM_DQSA_N2	AL25	IO, LVDS2J_16P, DQS10L
24 HMEM_DQSA_P2	AM25	IO, LVDS2J_17N, DQ10L
24 HMEM_DQA20	AK23	IO, LVDS2J_17P, DQ10L
24 HMEM_DQA21	AL23	IO, LVDS2J_18N, DQ10L
24 HMEM_DQA23	AM24	IO, LVDS2J_18P, DQ10L
	AL24	IO, LVDS2J_19N, DQ11L
24 HPSMEM_DMA3	AH25	IO, LVDS2J_19P, DQ11L
24 HMEM_DQA31	AJ26	IO, LVDS2J_20N, DQ11L
24 HMEM_DQA30	AH23	IO, LVDS2J_20P, DQ11L
24 HMEM_DQA27	AH24	IO, LVDS2J_21N, DQ11L
24 HMEM_DQA29	AJ23	IO, LVDS2J_21P, DQ11L
24 HMEM_DQA28	AJ24	IO, LVDS2J_22N, DQSN11L
24 HMEM_DQSA_N3	AJ25	IO, LVDS2J_22P, DQS11L
24 HMEM_DQSA_P3	AK25	IO, LVDS2J_23N, DQ11L
24 HMEM_DQA25	AF25	IO, LVDS2J_23P, DQ11L
24 HMEM_DQA26	AG25	IO, LVDS2J_24N, DQ11L
24 HMEM_DQA24	AF24	IO, LVDS2J_24P, DQ11L
24 HMEM_ADDR_CMD29	AG24	

IO BANK 2J, HPS Memory BANK

A10SOC_1517

R651 100

CLK_HPSEMI_N 40
CLK_HPSEMI_P 40

All HPS memory IO pin assignment must be same as Quartus'

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HPS Shared IOs

U23I

Signal	Pin	Bank Description
25 USB_CLK	D18	IO, DQ0L, GPIO0_IO0,NAND_ADQ0,UART0_CTS_N,USB0_CLK,SDMMC_DATA0,SPIM0_SS1_N,SPIS0_CLK
25 USB_STP	E18	IO, DQ0L, GPIO0_IO1,NAND_ADQ1,UART0_RTS_N,USB0_STP,SDMMC_CMD,SPIM1_SS1_N,SPIS0_MOSI
25 USB_DIR	C19	IO, DQ0L, GPIO0_IO2,NAND_WE_N,UART0_TX,USB0_DIR,SDMMC_CCLK,SPIS0_SS0_N,I2C1_SDA
25 USB_DATA0	D19	IO, DQ0L, GPIO0_IO3,NAND_RE_N,UART0_RX,USB0_DATA0,SDMMC_DATA1,SPIS0_MISO,I2C1_SCL
25 USB_DATA1	E17	IO, DQ0L, GPIO0_IO4,NAND_WP_N,UART1_CTS_N,QSPI_SS2,USB0_DATA1,SDMMC_DATA2,SPIM0_CLK,I2C0_SDA
25 USB_NXT	F17	IO, DQ0L, GPIO0_IO5,NAND_ADQ2,UART1_RTS_N,QSPI_SS3,USB0_NXT,SDMMC_DATA3,SPIM0_MOSI,I2C0_SCL
25 USB_DATA2	C17	IO, DQSN0L, GPIO0_IO6,NAND_ADQ3,UART1_TX,USB0_DATA2,SDMMC_DATA4,SPIM0_MISO,EMAC2_MDIO,I2C_EMAC2_SDA
25 USB_DATA3	C18	IO, DQS0L, GPIO0_IO7,NAND_CLE,UART1_RX,USB0_DATA3,SDMMC_DATA5,SPIM0_SS0_N,EMAC2_MDC,I2C_EMAC2_SCL
25 USB_DATA4	D21	IO, DQ0L, GPIO0_IO8,NAND_ADQ4,USB0_DATA4,SDMMC_DATA6,SPIM1_CLK,SPIS1_CLK,EMAC1_MDIO,I2C_EMAC1_SDA
25 USB_DATA5	D20	IO, DQ0L, GPIO0_IO9,NAND_ADQ5,USB0_DATA5,SDMMC_DATA7,SPIM1_MOSI,SPIS1_MOSI,EMAC1_MDC,I2C_EMAC1_SCL
25 USB_DATA6	E21	IO, DQ0L, GPIO0_IO10,NAND_ADQ6,USB0_DATA6,SPIM1_MISO,SPIS1_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
25 USB_DATA7	E22	IO, DQ0L, GPIO0_IO11,NAND_ADQ7,USB0_DATA7,SPIM1_SS0_N,SPIS1_MISO,EMAC0_MDC,I2C_EMAC0_SCL
22 ENET_HPS_GTX_CLK	H18	IO, DQ1L, GPIO0_IO12,NAND_ALE,USB1_CLK,EMAC0_TX_CLK
22 ENET_HPS_TX_EN	H19	IO, DQ1L, GPIO0_IO13,NAND_RB,USB1_STP,EMAC0_TX_CTL
22 ENET_HPS_RX_CLK	F18	IO, DQ1L, GPIO0_IO14,NAND_CE_N,USB1_DIR,EMAC0_RX_CLK
22 ENET_HPS_RX_DV	G17	IO, DQ1L, GPIO0_IO15,USB1_DATA0,EMAC0_RX_CTL
22 ENET_HPS_TXD0	E20	IO, DQ1L, GPIO0_IO16,NAND_ADQ8,USB1_DATA1,EMAC0_TXD0
22 ENET_HPS_TXD1	F20	IO, DQ1L, GPIO0_IO17,NAND_ADQ9,USB1_NXT,EMAC0_TXD1
22 ENET_HPS_RXD0	G20	IO, PLL_2L_CLKOUT1N, DQSN1L, GPIO_IO18,NAND_ADQ10,USB1_DATA2,EMAC0_RXD0
22 ENET_HPS_RXD1	G21	IO, PLL_2L_CLKOUT1P, PLL_2_L_CLKOUT1, PLL_2L_FB1, DQS1L, GPIO0_IO19,NAND_ADQ11,USB1_DATA3,EMAC0_RXD1,SPIM1_SS1_N
22 ENET_HPS_TXD2	F19	IO, DQ1L, GPIO0_IO20,NAND_ADQ12,UART0_CTS_N,USB1_DATA4,EMAC0_TXD2,SPIM1_CLK,SPIS0_CLK,I2C1_SDA
22 ENET_HPS_TXD3	G19	IO, RZQ_2L, DQ1L, GPIO0_IO21,NAND_ADQ13,UART0_RTS_N,USB1_DATA5,EMAC0_TXD3,SPIM1_MOSI,SPIS0_MOSI,I2C1_SCL
22 ENET_HPS_RXD2	F22	IO, CLK_2L_1N, DQ1L, GPIO0_IO22,NAND_ADQ14,UART0_TX,USB1_DATA6,EMAC0_RXD2,SPIM1_MISO,SPIS0_SS0_N,I2C0_SDA
22 ENET_HPS_RXD3	G22	IO, CLK_2L_1P, DQ1L, GPIO0_IO23,NAND_ADQ15,UART0_RX,USB1_DATA7,EMAC0_RXD3,SPIM1_SS0_N,SPIS0_MISO,I2C0_SCL
35 SPIM1_CLK	K18	IO, CLK_2L_0N, DQ2L, GPIO1_IO0,NAND_ADQ0,UART0_CTS_N,EMAC1_TX_CLK,SPIM1_CLK
35 SPIM1_MOSI	L19	IO, CLK_2L_0P, DQ2L, GPIO1_IO1,NAND_ADQ1,UART0_RTS_N,EMAC1_TX_CTL,SPIM1_MOSI
35 SPIM1_MISO	H22	IO, DQ2L, GPIO1_IO2,NAND_WE_N,UART0_TX,EMAC1_RX_CLK,SPIS0_CLK,I2C0_SDA
35 SPIM1_SS0_N	H21	IO, DQ2L, GPIO1_IO3,NAND_RE_N,UART0_RX,EMAC1_RX_CTL,SPIM1_SS0_N,I2C0_SCL
35 SPIM1_SS1_N	J21	IO, DQ2L, GPIO1_IO4,NAND_WP_N,UART1_CTS_N,EMAC1_TXD0,SPIM1_SS1_N,SPIS1_CLK
35 A10SH_GPIO0	J20	IO, PLL_2L_CLKOUT0P, PLL_2L_CLKOUT0, PLL_2L_FB0, DQ2L, GPIO1_IO5,NAND_ADQ2,UART1_RTS_N,EMAC1_TXD1,SPIS1_MOSI
35 HPSUARTA_TX	J18	IO, DQSN2L, GPIO1_IO6,NAND_ADQ3,UART1_TX,EMAC1_RXD0,SPIS1_SS0_N,I2C1_SDA
35 HPSUARTA_RX	J19	IO, DQS2L, GPIO1_IO7,NAND_CLE,UART1_RX,EMAC1_RXD1,SPIS1_MISO,I2C1_SCL
42 USER_PB_HPS3	H23	IO, DQ2L, GPIO1_IO8,NAND_ADQ4,EMAC1_TXD2,SPIS0_CLK,EMAC2_MDIO,I2C_EMAC2_SDA
42 USER_DIPSW_HPS3	J23	IO, DQ2L, GPIO1_IO9,NAND_ADQ5,EMAC1_TXD3,SPIS0_MOSI,EMAC2_MDC,I2C_EMAC2_SCL
22 ENET_HPS_MDIO	K21	IO, DQ2L, GPIO1_IO10,NAND_ADQ6,EMAC1_RXD2,SPIS0_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
22 ENET_HPS_MDC	K20	IO, DQ2L, GPIO1_IO11,NAND_ADQ7,EMAC1_RXD3,SPIS0_MISO,EMAC0_MDC,I2C_EMAC0_SCL
SH_SDA	L20	IO, DQ3L, GPIO1_IO12,NAND_ALE,EMAC2_TX_CLK,SDMMC_DATA0,I2C1_SDA
SH_SCL	M20	IO, DQ3L, GPIO1_IO13,NAND_RB,EMAC2_TX_CTL,SDMMC_CMD,I2C1_SCL
35 A10SH_GPIO1	N20	IO, DQ3L, GPIO1_IO14,NAND_CE_N,UART1_TX,EMAC2_RX_CLK,SDMMC_CCLK
23 TRACE_CIK	P20	IO, DQ3L, GPIO1_IO15,UART1_RX,TRACE_CLK,EMAC2_RX_CTL,SDMMC_DATA1
35 A10SH_GPIO2	K23	IO, DQ3L, GPIO1_IO16,NAND_ADQ8,UART1_CTS_N,QSPI_SS2,EMAC2_TXD0,SDMMC_DATA2
35 A10SH_GPIO3	L23	IO, DQ3L, GPIO1_IO17,NAND_ADQ9,UART1_RTS_N,QSPI_SS3,EMAC2_TXD1,SDMMC_DATA3,SPIM0_SS1_N
42 USER_DIPSW_HPS2	N23	IO, DQSN3L, GPIO1_IO18,NAND_ADQ10,EMAC2_RXD0,SDMMC_DATA4,SPIM0_MISO,EMAC1_MDIO,I2C_EMAC1_SDA
42 USER_LED_HPS3	N22	IO, DQS3L, GPIO1_IO19,NAND_ADQ11,TRACE_CLK,EMAC2_RXD1,SDMMC_DATA5,SPIM0_SS0_N,EMAC1_MDC,I2C_EMAC1_SCL
23 TRACE_D0	K22	IO, DQ3L, GPIO1_IO20,NAND_ADQ12,TRACE_D0,EMAC2_TXD2,SDMMC_DATA6,SPIM0_CLK,SPIS1_CLK,I2C_EMAC2_SDA
23 TRACE_D1	L22	IO, DQ3L, GPIO1_IO21,NAND_ADQ13,TRACE_D1,EMAC2_TXD3,SDMMC_DATA7,SPIM0_MOSI,SPIS1_MOSI,I2C_EMAC2_SCL
23 TRACE_D2	M22	IO, DQ3L, GPIO1_IO22,NAND_ADQ14,TRACE_D2,EMAC2_RXD2,SPIM0_MISO,SPIS1_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
23 TRACE_D3	M21	IO, DQ3L, GPIO1_IO23,NAND_ADQ15,TRACE_D3,EMAC2_RXD3,SPIM0_SS0_N,SPIS1_MISO,EMAC0_MDC,I2C_EMAC0_SCL

IO BANK 2L, 3V0,2V5,1V8 BANK

A10SOC_1517

IO_1V8 36,37,68

IO_3V3 69

HOSTPROCESSOR_I2C

R501 4.7K R500 4.7K

U55

7	B0	A0	2
6	B1	A1	3
		OE	5
8	VCCB	VCCA	1
		GND	4

FXMA2102UMX

A10_2L_SDA 35,45
A10_2L_SCL 35,45
A10I2CEN 35

C437 0.1uF

C436 0.1uF

1.00k R4077

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IO_1V8

IO_1V8   36,37,68
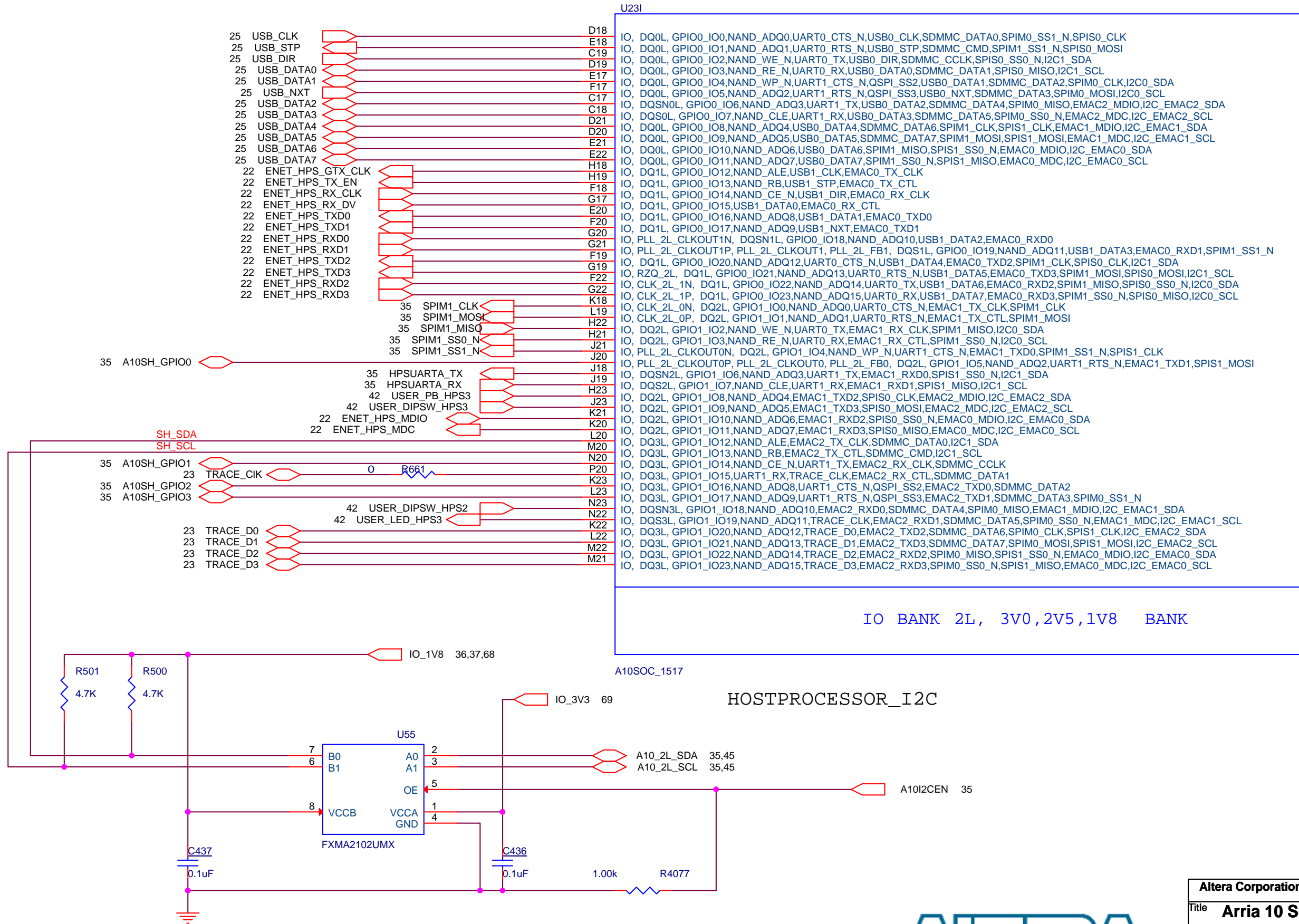
AS QSPI FLASH

U19

64MB, 1.8V Serial Flash Memory
Put the device close to Max V

HPS_BOOT
FLASH_PORT

EPCQ1024L

FPGA CONF, HPS Dedicated IO, 1V8 Bankd

A10SOC_1517

Bootsel bits are configured in Bootflash daughter card

Table 5-1: BOOTSEL Values for each Flash Memory Device Selection

BOOTSEL Field Value	Flash Device
0x0	Reserved
0x1	FPGA (HPS-to-FPGA bridge)
0x2	1.8V NAND flash memory
0x3	3.3V NAND flash memory
0x4	1.8V SD/MMC flash memory with external transceiver
0x5	3.3V SD/MMC flash memory with external transceiver
0x6	1.8V SPI or quad SPI flash memory
0x7	3.3V SPI or quad SPI flash memory

Table 7-3: MSEL Pin Settings for Each Configuration Scheme of Arria 10 Devices

Configuration Scheme	V_{CCPGM} (V)	Power-On Reset (POR) Delay	Valid MSEL[2..0]
FPP (x8, x16, and x32)	1.8	Fast	000
		Standard	001
PS	1.8	Fast	000
		Standard	001
AS (x1 and x4)	1.8	Fast	010
		Standard	011
JTAG-based configuration	—	—	Use any valid MSEL pin settings above

Title **Arria 10 SoC FPGA Development Kit Board**

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10/100/1000 Ethernet - HPS

U12A KSZ9031RN

- R68 1.00K
- R80 4.7K
- R67 4.7K
- R62 1.00K

IO_1V8

- 20 ENET_HPS_MDC — 36 MDC
- 20 ENET_HPS_MDIO — 37 MDIO
- 35 ENET_HPS_RESETn — 42 RESET_N
- 35 ENET_HPS_INTn — 38 INT_N/PME_N2

IO_3V3

- RX_CLK_PHYAD2 35 — ENET_HPS_RX_CLK 20
- GTX_CLK 24 — ENET_HPS_GTX_CLK 20
- TX_EN 25 — ENET_HPS_TX_EN 20
- RX_DV_CLK125_EN 33 — ENET_HPS_RX_DV 20

IO_5V IO_2V5 IO_1V8 IO_3V3

- IO_3V3 69
- IO_1V8 36,37,68
- IO_2V5 36,68
- IO_5V 50

J5 ENET_L829-1J1T-43

- 13 YK Yellow
- 14 YA — R7 220
- 11 TD0_P
- 12 CT0 — CT0
- 10 TD0_N
- 4 TD1_P
- 6 CT1 — CT1
- 5 TD1_N
- 3 TD2_P
- 1 CT2 — CT2
- 2 TD2_N
- 8 TD3_P
- 7 CT3 — CT3
- 9 TD3_N
- 18 GND_TAB
- 19 GND_TAB
- 15 OK Orange
- 17 GK Green
- 16 GOA — R8 220

MDI INTERFACE

- MDI_HPS_P0 2 TXRXP_A
- MDI_HPS_N0 3 TXRXM_A
- MDI_HPS_P1 5 TXRXP_B
- MDI_HPS_N1 6 TXRXM_B
- MDI_HPS_P2 7 TXRXP_C
- MDI_HPS_N2 8 TXRXM_C
- MDI_HPS_P3 10 TXRXP_D
- MDI_HPS_N3 11 TXRXM_D

- TXD3 22 — ENET_HPS_TXD3 20
- TXD2 21 — ENET_HPS_TXD2 20
- TXD1 20 — ENET_HPS_TXD1 20
- TXD0 19 — ENET_HPS_TXD0 20

- RXD0_MODE0 32 — ENET_HPS_RXD0 20
- RXD1_MODE1 31 — ENET_HPS_RXD1 20
- RXD2_MODE2 28 — ENET_HPS_RXD2 20
- RXD3_MODE3 27 — ENET_HPS_RXD3 20

- R340 12.1K ENET_RSET — 48 ISET
- CLK125_NDO_LED_MODE 41

- 17 LED1_PHYAD0/PME_N1
- 15 LED2_PHYAD1
- 46 XI
- 45 XO

IO_1V8 BOOT-STRAPS

R57	DNI	ENET_HPS_LED2_LINK	
R61	DNI	ENET_HPS_LED1_LINK	
R70	4.7K	ENET_HPS_RXD3	
R72	4.7K	ENET_HPS_RXD2	
R74	4.7K	ENET_HPS_RXD1	
R76	4.7K	ENET_HPS_RXD0	
R77	DNI	ENET_HPS_RX_DV	
R81	4.7K	ENET_HPS_RX_CLK	
R63	4.7K	CLK125_NDO_LED_MODE	

R367	4.7K	
R378	4.7K	
R69	DNI	
R71	DNI	
R73	DNI	
R75	DNI	
R78	4.7K	
R79	DNI	
R351	DNI	

ETHERNET INTERFACE

- C15 0.01uF CT0
- C13 0.01uF CT1
- C12 0.01uF CT2
- C14 0.01uF CT3

R5497 10K

U72 25.00MHz
- 1 EN VCC 4
- 2 GND OUT 3

IO_2V5

C242 0.01uF

1.2V AVDLL_PLL

U10 LT3026-1
- 1 IN1 BST 5 — C26 1uF — 1.2V_AVDLL_PLL
- 2 IN2
- 4 GNDS OUT2 10
- OUT1 9
- 6 SHDN ADJ 8 — R341 2.00K
- PG 7
- GND 3
- GND 11

- C21 10uF
- R342 10K
- R124 1.00K
- C24 22uF
- C22 2.2uF

IO_2V5

U12B KSZ9031RN

3.3V_AVDDH
- 47 NC1
- 12 AVDDH
- 1 AVDDH

1.8V_DVDDH
- 40 DVDDH
- 16 DVDDH
- 34 DVDDH

- 49 P_GND
- 13 NC
- 29 VSS

- AVDDL_PLL 44 — 1.2V_AVDLL_PLL
- LDO_O 43
- AVDDL 9 — 1.2V_AVDDL
- AVDDL 4

- DVDDL 18 — 1.2V_DVDDL
- DVDDL 14
- DVDDL 39
- DVDDL 30
- DVDDL 26
- DVDDL 23

Capacitor networks

1.2V_AVDLL_PLL
- C16 22uF
- C25 2.2uF
- C261 0.1uF

1.2V_AVDLL_PLL — L1 3A, 30 Ohm FB — 1.2V_AVDLL
- C23 22uF
- C243 2.2uF
- C229 0.1uF

- L16 3A, 30 Ohm FB — 1.2V_DVDDL
- C245 22uF
- C280 2.2uF
- C281 0.1uF

IO_3V3 — L15 3A, 30 Ohm FB — 3.3V_AVDDH
- C210 22uF
- C228 2.2uF
- C230 0.1uF

IO_1V8 — L2 3A, 30 Ohm FB — 1.8V_DVDDH
- C28 22uF
- C262 2.2uF
- C244 0.1uF

IO_3V3
- C203 10uF
- C37 10uF

Place near KSZ9021RN PHY

NAME	Pin	Value	Description
PHYAD2	35	1	ID = b"111"
PHYAD1	15	1	
PHYAD0	17	1	
MODE3	27	1	RGMII (10/100/1000)
MODE2	28	1	
MODE1	31	1	
MODE0	32	1	
ClK125_EN	33	0	No clockoutput
LED_MODE	41	1	singal led mode

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ALTERA

Connectors of Boot flash, file flash,early trace and fast trace

J20 (Mictor Fast Trace) — Mictor38P

Pin	Signal		Pin	Signal
1	NC1	NC3	2	
3	NC2	NC4	4	
5	GND	TRACECLK	6	
7	TRIGINTRIGOUT		8	FTRACE_CLK 27,38
9	nSRST	NC	10	
11	TDO/SWO/TREF		12	
13	RTCK	Vsupply	14	
15	TCK	TD7	16	
17	TMS	TD6	18	FTRACE_D7 27,38
19	TDI	TD5	20	FTRACE_D6 27,38
21	nTRST	TD4	22	FTRACE_D5 27,38
23	TD15	TD3	24	FTRACE_D4 27,38
25	TD14	TD2	26	FTRACE_D3 27,38
27	TD13	TD1	28	FTRACE_D2 27,38
29	TD12	Logic0A	30	FTRACE_D1 27,38
31	TD11	Logic0B	32	
33	TD10	LOGIC1	34	
35	TD9	TRACECTL	36	
37	TD8	TD0	38	FTRACE_D0 27,38
	GND1		39	
	GND2		40	
	GND3		41	
	GND4		42	
	GND5		43	

Mictor Fast Trace

Signals to J20:
38 FTRACE_PROC_RESETn
38 FTRACE_JTAG_TDO
38 FTRACE_JTAG_TCK
38 FTRACE_JTAG_TMS
38 FTRACE_JTAG_TDI
38 FTRACE_JTAG_TRSTn
27,38 FTRACE_D15
27,38 FTRACE_D14
27,38 FTRACE_D13
27,38 FTRACE_D12
27,38 FTRACE_D11
27,38 FTRACE_D10
27,38 FTRACE_D9
27,38 FTRACE_D8

R384 10K
R413 10K
R414 DNI R415
FMICTOR_PWR1   0_Ohms
R416   DNI
FMIC_30   R417 10K
FMIC_32   R418 10K
FMIC_34   R419 10K
R420 10K
IO_1V8

J43 (Mictor Early Trace) — Mictor38P

Pin	Signal		Pin	Signal
1	NC1	NC3	2	
3	NC2	NC4	4	
5	GND	TRACECLK	6	
7	TRIGINTRIGOUT		8	
9	nSRST	NC	10	
11	TDO/SWO/TREF		12	TRACE_CIK 20
13	RTCK	Vsupply	14	
15	TCK	TD7	16	
17	TMS	TD6	18	
19	TDI	TD5	20	
21	nTRST	TD4	22	
23	TD15	TD3	24	
25	TD14	TD2	26	TRACE_D3 20
27	TD13	TD1	28	TRACE_D2 20
29	TD12	Logic0A	30	TRACE_D1 20
31	TD11	Logic0B	32	
33	TD10	LOGIC1	34	MIC_34
35	TD9	TRACECTL	36	
37	TD8	TD0	38	TRACE_D0 20
	GND1		39	
	GND2		40	
	GND3		41	
	GND4		42	
	GND5		43	

Mictor Early Trace

Signals to J43:
38 MICTOR_PROC_RESETn
38 MICTOR_JTAG_TDO
38 MICTOR_JTAG_TCK
38 MICTOR_JTAG_TMS
38 MICTOR_JTAG_TDI
38 MICTOR_JTAG_TRSTn

R809 10K
R772 10K
R771 DNI R770
MICTOR_PWR1   0_Ohms
R784 DNI
MICTOR_JTAG_TDO
R769 10K
R768 10K
R783 10K
R782 10K
IO_1V8

U77 / U78 — SN74LVC1G126

U77: 1 OE, 2 A, 4 Y, 3 GND, 5 VCC
U78: 1 OE, 2 A, 4 Y, 3 GND, VCC
35 dedicated_OE
35 dedicated_RX
dedicated_TX 35

C350 0.1uF
C204 0.1uF
C246 0.1uF
C296 0.1uF
IO_1V8

J23 — Boot Flash Slot (QTH-030-02-L-D-A)

21 HPS_DIO1
21 HPS_DIO4
21 HPS_DIO10
21 HPS_DIO12
21 HPS_DIO2
21 HPS_DIO8
21 HPS_DIO9
HPS_DIO0 21
HPS_DIO5 21
HPS_DIO11 21
HPS_DIO13 21
HPS_DIO3 21
HPS_DIO7 21
HPS_DIO6 21

35 BF_Presentn
BQSPI_RESETN 35
C413 0.1uF
IO_3V3
MH1 MHOLE4-40
STDoff2 8mmStandoff

Boost Flash Slot

J11 — File Flash Slot (QTH-030-02-L-D-A)

27 FILE_DIO1
27 FILE_DIO4
27 FILE_DIO10
27 FILE_DIO12
27 FILE_DIO2
27 FILE_DIO8
27 FILE_DIO9
FILE_DIO0 27
FILE_DIO5 27
FILE_DIO11 27
FILE_DIO13 27
FILE_DIO3 27
FILE_DIO7 27
FILE_DIO6 27

35 File_Presentn
FILE_RESETN 35
IO_3V3
C295 0.1uF
MH2 MHOLE4-40
STDoff1 8mmStandoff

File Flash Slot

U15 — EPCQ1024L (MAXV PS Flash)

Pin	Signal		Pin	Signal
B4	VCC	DQ0	D3	MFD0 35
C	C	DQ1	D2	MFD1 35
C2	S#	W#/VPP/DQ2	C4	MFD2 35
B3	VSS	HOLD#/DQ3	D4	MFD3 35
A2	NC1	NC9	C5	
A3	NC2	NC10	D1	
A4	NC3	NC11	D5	
A5	NC4	NC12	E1	
B1	NC5	NC13	E2	
B5	NC6	NC14	E3	
C1	NC7	NC15	E4	
C3	NC8	NC16	E5	

35 MFCLK
35 MFCSN
R435 10K
R439 10K
1V8
C374 0.1uF
C364 0.1uF

MAXV PS Flash

IO_1V8 1V8
IO_3V3
1V8   35,54
IO_1V8 36,37,68
IO_3V3 69

ALTERA

J26A — HiLo EMI - EMI SIGNALS

Pin	Signal		Signal	Pin	Signal
F1	MEM_ADDR_CMD0		MEM_DQ_ADDR_CMD0	R6	HMEM_DQ_ADDR_CMD0 19
H1	MEM_ADDR_CMD1		MEM_DQ_ADDR_CMD1	T1	HMEM_DQ_ADDR_CMD1 19
F2	MEM_ADDR_CMD2		MEM_DQ_ADDR_CMD2	R2	HMEM_DQ_ADDR_CMD2 19
G2	MEM_ADDR_CMD3		MEM_DQ_ADDR_CMD3	U2	HMEM_DQ_ADDR_CMD3 19
H2	MEM_ADDR_CMD4		MEM_DQ_ADDR_CMD4	U3	HMEM_DQ_ADDR_CMD4 19
J2	MEM_ADDR_CMD5		MEM_DQ_ADDR_CMD5	T4	HMEM_DQ_ADDR_CMD5 19
K2	MEM_ADDR_CMD6		MEM_DQ_ADDR_CMD6	U4	HMEM_DQ_ADDR_CMD6 19
G3	MEM_ADDR_CMD7		MEM_DQ_ADDR_CMD7	T5	HMEM_DQ_ADDR_CMD7 19
J3	MEM_ADDR_CMD8		MEM_DQ_ADDR_CMD8	U5	HMEM_DQ_ADDR_CMD8 19
L3	MEM_ADDR_CMD9				
E4	MEM_ADDR_CMD10		MEM_DQS_ADDR_CMD_P	V4	HMEM_DQS_ADDR_CMD_P 19
F4	MEM_ADDR_CMD11		MEM_DQS_ADDR_CMD_N	V5	HMEM_DQS_ADDR_CMD_N 19
G4	MEM_ADDR_CMD12				
H4	MEM_ADDR_CMD13		MEM_CLK_P	V1	HMEM_CLK_P 19
J4	MEM_ADDR_CMD14		MEM_CLK_N	V2	HMEM_CLK_N 19
K4	MEM_ADDR_CMD15				
M1	MEM_ADDR_CMD16				
M2	MEM_ADDR_CMD17		CONFIG0	L6	
N2	MEM_ADDR_CMD18		CONFIG1	M6	
L4	MEM_ADDR_CMD19				
P5	MEM_ADDR_CMD20				
M5	MEM_ADDR_CMD21		RFU2	H5	
P1	MEM_ADDR_CMD22		RFU3	K5	
R4	MEM_ADDR_CMD23		RFU4	N6	
M4	MEM_ADDR_CMD24		RFU5	R7	
R3	MEM_ADDR_CMD25		RFU6	R8	
L2	MEM_ADDR_CMD26				
K1	MEM_ADDR_CMD27				
P2	MEM_ADDR_CMD28				
N4	MEM_ADDR_CMD29				
P4	MEM_ADDR_CMD30				
N3	MEM_ADDR_CMD31				

VDDQ_1.1V_SET and VDDQ_1.8V_SET NOT USED
Only support DDR3 and DDR4

DMA / DQ signals

Pin	Signal	Signal	Pin
B10	MEM_DMA0	MEM_DMB0	M16
C4	MEM_DMA1	MEM_DMB1	U16
B17	MEM_DMA2	MEM_DMB2	U11
F17	MEM_DMA3	MEM_DMB3	U6
A4	MEM_DQA0	MEM_DQB0	H16
B4	MEM_DQA1	MEM_DQB1	J16
B5	MEM_DQA2	MEM_DQB2	K16
B6	MEM_DQA3	MEM_DQB3	L16
A8	MEM_DQA4	MEM_DQB4	H17
B8	MEM_DQA5	MEM_DQB5	K17
B9	MEM_DQA6	MEM_DQB6	K18
A10	MEM_DQA7	MEM_DQB7	L18
B1	MEM_DQA8	MEM_DQB8	M17
B2	MEM_DQA9	MEM_DQB9	N18
C2	MEM_DQA10	MEM_DQB10	P17
C3	MEM_DQA11	MEM_DQB11	P18
E3	MEM_DQA12	MEM_DQB12	R18
D4	MEM_DQA13	MEM_DQB13	T16
D1	MEM_DQA14	MEM_DQB14	T17
D2	MEM_DQA15	MEM_DQB15	T18
A12	MEM_DQA16	MEM_DQB16	U15
B12	MEM_DQA17	MEM_DQB17	U14
B13	MEM_DQA18	MEM_DQB18	V14
B14	MEM_DQA19	MEM_DQB19	T13
C15	MEM_DQA20	MEM_DQB20	T12
A16	MEM_DQA21	MEM_DQB21	U12
B16	MEM_DQA22	MEM_DQB22	V12
A18	MEM_DQA23	MEM_DQB23	T10
C16	MEM_DQA24	MEM_DQB24	U10
D16	MEM_DQA25	MEM_DQB25	V10
E16	MEM_DQA26	MEM_DQB26	T9
F16	MEM_DQA27	MEM_DQB27	T8
D17	MEM_DQA28	MEM_DQB28	U8
C18	MEM_DQA29	MEM_DQB29	U7
D18	MEM_DQA30	MEM_DQB30	V6
E18	MEM_DQA31	MEM_DQB31	R16
E2	MEM_DQA32	MEM_DQB32	T6
G16	MEM_DQA33	MEM_DQB33	

Pin	Signal	Signal	Pin
A6	MEM_DQSA_P0	MEM_DQSB_P0	H18
A7	MEM_DQSA_N0	MEM_DQSB_N0	J18
A2	MEM_DQSA_P1	MEM_DQSB_P1	U18
A3	MEM_DQSA_N1	MEM_DQSB_N1	V18
A14	MEM_DQSA_P2	MEM_DQSB_P2	V16
A15	MEM_DQSA_N2	MEM_DQSB_N2	V17
F18	MEM_DQSA_P3	MEM_DQSB_P3	V8
G18	MEM_DQSA_N3	MEM_DQSB_N3	V9
A11	MEM_QKA_N0	MEM_QKB_N0	M18
B18	MEM_QKA_N1	MEM_QKB_N1	V13

HLS-180324-B-12

J26B — HiLo EMI - POWER

HILOHPS_VDD

VEXT = 2.5V

Pin	Signal		Pin	Signal
C7	VDD		L11	VEXT
C9	VDD		L13	VEXT
C11	VDD		M8	VEXT
C13	VDD		M10	VEXT
D6	VDD		M12	VEXT
D8	VDD		M14	VEXT
D10	VDD		N7	VEXT
D12	VDD		N9	VEXT
D14	VDD		N11	VEXT
E7	VDD		N13	VEXT
E9	VDD		P8	VEXT
E11	VDD		P10	VEXT
E13	VDD		P12	VEXT
F6	VDD		P14	VEXT
F8	VDD			
F10	VDD			

VDD = 1.1(DEFAULT)

62 HILOHPS_VDD

Pin	Signal
G15	VDD_1.2V_SET
D5	VDD_1.25V_SET
E15	VDD_1.30V_SET
J15	VDD_1.35V_SET
L15	VDD_1.5V_SET
N16	VDD_1.8V_SET

62 HILOHPS_1V2_SETn
62 HILOHPS_1V35_SETn
62 HILOHPS_1V5_SETn

HILOHPS_VDD

Pin	Signal		VTT
F12	VDDQ	J7	2.5V/3.3V (VTT)
F14	VDDQ	J9	2.5V/3.3V (VTT)
G7	VDDQ	K6	2.5V/3.3V (VTT)
G9	VDDQ	K8	2.5V/3.3V (VTT)
G11	VDDQ	K10	2.5V/3.3V (VTT)
G13	VDDQ	K12	2.5V/3.3V (VTT)
H6	VDDQ	J11	2.5V/3.3V (VTT)
H8	VDDQ	L7	2.5V/3.3V (VTT)
H10	VDDQ	L9	2.5V/3.3V (VTT)
H12	VDDQ		

VDDQ = 1.1(DEFAULT)

IO_2V5   L11 / L13 → IO_2V5 36,68
IO_3V3   J7 / J9 → IO_3V3 69

Pin	Signal
N15	VDDQ_1.1V_SET
P16	VDDQ_1.2V_SET
F5	VDDQ_1.25V_SET
R15	VDDQ_1.30V_SET
R14	VDDQ_1.35V_SET
R12	VDDQ_1.5V_SET
R11	VDDQ_1.8V_SET

Pin	Signal
H14	VREF
J13	VREF
K14	VREF

HILOHPS_VDD
R5492 240
R5493 240
C1558 0.1uF

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J26C — HiLo EMI - GND

GND pins: A1, A5, A9, A13, A17, B3, B7, B11, B15, C1, C5, C6, C8, C10, C12, C14, C17, D3, D7, D9, D11, D13, D15, E1, E5, E6, E8, E10, E12, E14, E17, F3, F7, F9, F11, F13, F15, G1, G5, G6, G8, G10, G12, G14, G17, H3, H7, H9, H11, H13, H15, J1, J5, J6, J8 — GND

J10, J12, J14, J17, K3, K7, K9, K11, K13, K15, L1, L5, L8, L10, L12, L14, L17, M3, M7, M9, M11, M13, M15, N1, N5, N8, N10, N12, N14, N17, P3, P6, P7, P9, P11, P13, P15, R1, R5, R9, R10, R13, R17, T3, T7, T11, T15, U1, U5, U9, U13, U17, V3, V7, V11, V15 — GND

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Decoupling (HILOHPS_VDD)

HMEM_DQSB_P0 — R5332 1.00k
HMEM_DQSB_P1 — R5333 1.00k
HMEM_DQSB_P2 — R5334 1.00k
HMEM_DQSB_P3 — R5335 1.00k
R5336 1.00k
R5337 1.00k
R5339 1.00k
HMEM_DQSB_N0 — R5338 1.00k
HMEM_DQSB_N1
HMEM_DQSB_N2
HMEM_DQSB_N3

C511 10uF / 1uF / C595 0.1uF / C596
Place near HILO connector J14 VDD pins

C512 10uF / 1uF / C563 0.1uF / C562
Place near HILO connector J14 VDDQ pins

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USB Ports

Current limit for Rseti of 137k is 1.013A

USB INTERFACE

35 USB_VFlagn

20 USB_DATA0
20 USB_DATA1
20 USB_DATA2
20 USB_DATA3
20 USB_DATA4
20 USB_DATA5
20 USB_DATA6
20 USB_DATA7

USB 2.0 OTG

IO_5V
IO_3V3   69
IO_5V   50
IO_1V8   36,37,68

C10 2.2uF

U4 MAX14523B
5 IN OUT 4
1 NC1
6 NC2 SETI 3
2 FLAG
7 ON GND 8
GND_PAD

R17 1%
137K
C4 0.1uF

R45 DNI
USB_5.0V
USB_VFlagn

R302 10K

C483 4.7uF

U22 USB3320

Pin	Signal
32	VDDIO
20	VDD3.3
21	VBAT
30	VDD1.8
28	VDD1.8
12	NC

3	DATA0	CPEN	17	USB_CPEN
4	DATA1	SPK_r	16
6	DATA2	SPK_L	15
7	DATA3	VBUS	22	USB_VBUS
9	DATA4	DM	19	USB_D_N
10	DATA5	DP	18	USB_D_P
13	DATA6	ID	23	USB_ID
	DATA7			
1	CLKOUT	XO	25	USB_XO
2	NXT	REFCLK	26	USB_XI
31	DIR	REFSEL2	14
29	STP	REFSEL0	8
24	RBIAS	REFSEL1	11
27	RESET	GND_FLAG	33

10K
R560 USB_DATA0
R561 USB_DATA1
R562 USB_DATA2
R563 USB_DATA3
R564 USB_DATA4
R565 USB_DATA5
R566 USB_DATA6
R567 USB_DATA7

IO_3V3
R513 DNI

USB_CLKR
USB_NXTR
USB_DIRR
USB_STP
USB_RBIAS
USB_RESET_PHY

R100 1.00K

C5 4.7uF

J4 MICRO_USB_CONN
1 VBUS
2 D-
3 D+
4 ID
5

Y4 24MHz
C62 30pF
R106 1M
C61 30pF

USB HPS Port

USB_FPGA_5.0V
USB_FPGA_1.8V

U32 LT3010
8 IN OUT 1
7 NC7
6 NC6 SENSE 3
5 SHDNn GND 4
NC3
EPAD 9

C889 1uF
R767 2.21K
C153 0.01uF
C881 1uF
R227 5.23K

IO_1V8

20 USB_CLK   R105   10
20 USB_NXT   R102   10
20 USB_DIR   R104   10
20 USB_STP

R101 8.06K
R99 1.00K

35 USB_RESET   R98   1.00K USB_RESET_PHY

USB FPGA INTERFACE

REFSEL[2:0] = 0X7, Reference Frequency = 24Mhz

USB_FPGA_5.0V
USB_FPGA_1.8V
USB_FPGA_3.3V

36 USB_MAXV_D0
36 USB_MAXV_D1
36 USB_MAXV_D2
36 USB_MAXV_D3
36 USB_MAXV_D4
36 USB_MAXV_D5
36 USB_MAXV_D6
36 USB_MAXV_D7

USB TI GUI Port

10K
R245
R262
R259
R267
R246
R264
R265
R263

U33 FT245RQ

30	DATA0	VCCIO	1
2	DATA1	VCC	19
32	DATA2	3V3VOUT	16
8	DATA3	USBDM	15	USB_F_D_N
31	DATA4	USBDP	14	USB_F_D_P
6	DATA5	TXE#	21
7	DATA6	RXF#	22
3	DATA7	OSCI	27
		OSCO	28
11	WR	PWREN#	9
10	RD#	GND	4
18	RESET#	GND	17
26	TEST	GND	20
		AGND	24
		GND_PAD	33

NC0 NC1 NC2 NC3 NC4 NC5
12 13 12 29 23

USB_FPGA_5.0V
5V_F_USB
C171 0.01uF
C168 4.7uF
3A, 30 Ohm FB
L14
J47 MICRO_USB_CONN
1 VBUS
2 D-
3 D+
4 ID
5
R266 0

USB_FPGA_2.5V
R268 10K

36 USB_MAXV_WR
36 USB_MAXV_RDn
36 USB_MAXV_RESET

R766 0
USB_F_RESET_PHY

R228 4.7K
USB_FPGA_1.8V

USB_MAXV_TXEn 36
USB_MAXV_RXFn 36

PLACE NEAR USB3320

MAX USB

USB_1V8
IO_3V3
IO_1V8

C485 0.1uF
C460 0.1uF
C459 0.1uF
C472 0.1uF
C473 0.1uF
C458 4.7uF
C471 0.1uF
C484 0.1uF

UART to USB PORT

UART

U13 — FT232R

Pin	Signal
30	TXD
2	RXD
32	RTS
8	CTS
31	DTR
6	DSR
7	DCD
3	RI
18	RESET
22	CBUS0
21	CBUS1
10	CBUS2
11	CBUS3
9	CBUS4
19	VCC
16	3V3OUT
1	VCCIO
15	USBDM
14	USBDP
25	NC1
23	NC2
5	NC3
12	NC4
13	NC5
29	NC6
27	OSCI
28	OSCO

TEST 26, GND3 20, GND2 17, GND1 4, AGND 24, EPAD_GND 33

35 UARTA_RX
35 UARTA_TX
35 RESET_HPS_UARTA_N
69 IO_3V3

XJ2 881545-2
J18 DNI 1 2

Green_LED D12 220 R366 UARTA_TX_LED
Green_LED D11 220 R368 UARTA_RX_LED

IO_3V3
3.3V_USB_UARTA R64 10K PWR_ENA
5V_USB_UARTA R357 4.7K
RESET_HPS_UARTA_N R356 10K

3.3V_USB_UARTA R82 VIO_USB_UARTA 0
R83 DNI
5V_USB_UARTA L4 742792780
DMA_N
DPA_P
R56 0

C275 39pF   C257 39pF

U41 TPD4S012DRYR
VBUS 6, ID 3, D+ 1, D- 2, NC 5, GND 4

J10
USB MINI-B-SMT
10, 11, 1, 2, 3, 4, 5, 6, 7, 8, 9

3.3V_USB_UARTA C276 0.1uF C27 2.2uF
VIO_USB_UARTA C294 0.1uF C293 2.2uF
5V_USB_UARTA C285 0.1uF C286 4.7uF

TP43

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FPBA 1.8V IOs for File Flash and Debug port

U37 (MAX3378)

Pin	Signal		Pin	Signal
14	VCC		1	VL
13	IO VCC1		2	IO VL1
12	IO VCC2		3	IO VL2
11	IO VCC3		4	IO VL3
10	IO VCC4		5	IO VL4
9	NC2		6	NC1
8	/TS		7	GND

IO_2V5 C208 0.1uF C209 0.1uF
IO_1V8

11 ENETA_MDIO
11 ENETA_MDC
12 ENETB_MDIO
12 ENETB_MDC
35 ENET_DISABLE_N

FPGA_IO[3:0]

FPGA_IO0 — R327 4.7K
FPGA_IO1 — R326 4.7K
FPGA_IO2 — R325 4.7K
FPGA_IO3 — R324 4.7K
C207 0.1uF

U23L — IO BANK 2A, 1V8 BANK (A10SOC_1517)

Pin	Signal
AH18	IO, LVDS2A_1N, DQ28L, DATA0
AJ18	IO, LVDS2A_1P, DQ28L, DATA1
AH17	IO, LVDS2A_2N, DQ28L, DATA2
AJ16	IO, LVDS2A_2P, DQ28L, DATA3
AK17	IO, LVDS2A_3N, DQ28L, DATA4
AK16	IO, LVDS2A_3P, DQ28L, DATA5
AK18	IO, LVDS2A_4N, DQSN28L, DATA6
AL17	IO, LVDS2A_4P, DQS28L, DATA7
AH19	IO, LVDS2A_5N, DQ28L, DATA8
AJ19	IO, LVDS2A_5P, DQ28L, DATA9
AL19	IO, LVDS2A_6N, DQ28L, DATA10
AL18	IO, LVDS2A_6P, DQ28L, DATA11
AM17	IO, LVDS2A_7N, DQ29L, DATA12
AN17	IO, LVDS2A_7P, DQ29L, DATA13
AM20	IO, LVDS2A_8N, DQ29L, DATA14
AM19	IO, LVDS2A_8P, DQ29L, DATA15
AM16	IO, LVDS2A_9N, DQ29L, DATA16
AN16	IO, LVDS2A_9P, DQ29L, DATA17
AP16	IO, PLL_2A_CLKOUT1N, LVDS2A_10N, DQSN29L, DATA18
AR16	IO, PLL_2A_CLKOUT1P, PLL_2A_CLKOUT1, PLL_2A_FB1, LVDS2A_10P, DQS29L, DATA19
AN19	IO, LVDS2A_11N, DQ29L, NCEO
AP19	IO, RZQ_2A, LVDS2A_11P, DQ29L
AN18	IO, CLK_2A_1N, LVDS2A_12N, DQ29L, DATA20
AP18	IO, CLK_2A_1P, LVDS2A_12P, DQ29L, DATA21
AR18	IO, CLK_2A_0N, LVDS2A_13N, DQ30L, DATA22
AT18	IO, CLK_2A_0P, LVDS2A_13P, DQ30L, DATA23
AR17	IO, LVDS2A_14N, DQ30L, DATA24
AT17	IO, LVDS2A_14P, DQ30L, DATA25
AT19	IO, PLL_2A_CLKOUT0N, LVDS2A_15N, DQ30L, DATA26
AU19	IO, PLL_2A_CLKOUT0P, PLL_2A_CLKOUT0, PLL_2A_FB0, LVDS2A_15P, DQ30L, DATA27
AT20	IO, LVDS2A_16N, DQSN30L, DATA28
AU20	IO, LVDS2A_16P, DQS30L, DATA29
AU17	IO, LVDS2A_17N, DQ30L, DATA30
AU16	IO, LVDS2A_17P, DQ30L, DATA31
AP20	IO, LVDS2A_18N, DQ30L, CLKUSR
AR20	IO, LVDS2A_18P, DQ30L, PR_REQUEST
AV16	IO, LVDS2A_19N, DQ31L, PR_READY
AW16	IO, LVDS2A_19P, DQ31L, NPERSTL0
AV19	IO, LVDS2A_20N, DQ31L, PR_DONE
AV18	IO, LVDS2A_20P, DQ31L, NPERSTL1
AV17	IO, LVDS2A_21N, DQ31L, PR_ERROR
AW18	IO, LVDS2A_21P, DQ31L
AV22	IO, LVDS2A_22N, DQSN31L, CVP_CONFDONE
AW21	IO, LVDS2A_22P, DQS31L
AW20	IO, LVDS2A_23N, DQ31L, INIT_DONE
AW19	IO, LVDS2A_23P, DQ31L, DEV_OE
AU21	IO, LVDS2A_24N, DQ31L, CRCERROR
AV21	IO, LVDS2A_24P, DQ31L, DEV_CLRN

35 PS_D0
23 FILE_DIO0
23 FILE_DIO1
23 FILE_DIO2
23 FILE_DIO3
23 FILE_DIO4
23 FILE_DIO5
23 FILE_DIO6
23 FILE_DIO7
23 FILE_DIO8
23 FILE_DIO9
23 FILE_DIO10
23 FILE_DIO11
23 FILE_DIO12
23 FILE_DIO13
23,38 FTRACE_D0
23,38 FTRACE_D1
23,38 FTRACE_D2
23,38 FTRACE_D3
23,38 FTRACE_D4
23,38 FTRACE_D5
23,38 FTRACE_D6
35 CLK_50M_FPGA
37 USB_FPGA_CLK
23,38 FTRACE_D7
23,38 FTRACE_D8
23,38 FTRACE_D9
23,38 FTRACE_D10
23,38 FTRACE_D11
23,38 FTRACE_D12
23,38 FTRACE_D13
23,38 FTRACE_D14
23,38 FTRACE_D15
23,38 FTRACE_CLK
39 CLKUSR
FPGA_IO1
FPGA_IO0
35,36 PCIE1V8_PERSTn
35 FPGA_IO4
35,36 PCIE1V8_PERST1n
FPGA_IO3
35 FPGA_IO5
35 CVP_CONFDONE
FPGA_IO2
35 CRCERROR
35 DEV_CLRN

UART_TX
UART_RX

U23X — 2I IO BANK, 1V8 BANK (A10SOC_1517)

Pin	Signal
AV29	DNU1
AV30	DNU2
AT22	IO, LVDS2I_7N, DQ13L
AU22	IO, LVDS2I_7P, DQ13L
AR22	IO, LVDS2I_8N, DQ13L
AR23	IO, LVDS2I_8P, DQ13L
AL22	IO, LVDS2I_9N, DQ13L
AM22	IO, LVDS2I_9P, DQ13L
AP21	IO, PLL_2I_CLKOUT1N, LVDS2I_10N, DQSN13L
AR21	IO, PLL_2I_CLKOUT1P, PLL_2I_CLKOUT1, PLL_2I_FB1, LVDS2I_10P, DQS13L
AN22	IO, LVDS2I_11N, DQ13L
AN21	IO, RZQ_2I, LVDS2I_11P, DQ13L
AL20	IO, CLK_2I_1N, LVDS2I_12N, DQ13L
AM21	IO, CLK_2I_1P, LVDS2I_12P, DQ13L
AG16	DNU3
AG17	DNU4
AF17	DNU5
A2	NC1
A3	NC2
AE20	NC3
AF20	NC4
AG20	NC5
AG21	NC6
AG22	NC7
AH21	NC8
AH22	NC9
AJ20	NC10
AJ21	NC11
AK20	NC12
AK21	NC13
AK22	NC14
AV1	NC15
AV2	NC16
AV3	NC17
AW2	NC18
AW3	NC19
B1	NC20
P19	NC21
W15	NC22
W16	NC23

15 DP_AUX_CH_N
15 DP_AUX_CH_P
36 FPGAIO_N
36 FPGAIO_P
36 FPGAIO12_N
36 FPGAIO12_P
36 FPGAIO11_N
36 FPGAIO11_P
36 FPGAIO10_N
36 FPGAIO10_P
36 FPGAIO1_N
36 FPGAIO1_P

FPGA_PMVID

U58 (FXMA2102UMX)

Pin	Signal		Pin	Signal
7	B0		2	A0
6	B1		3	A1
			5	OE
8	VCCB		1	VCCA
			4	GND

IO_1V8 R525 10K R550 10K
IO_1V8
VID_SCL_1V8
VID_SDA_1V8
IO_3V3
PMbus_SCL_3V3 45,51,56,73
PMbus_SDA_3V3 45,51,56,73
1.00k R4076
C482 0.1uF
C470 0.1uF
A10PMBUSEN 35

J41
1
2 TSENSE_FAN_CNTL
22_23_2021
B3
FAN_2pin_Conn
MAIN_12V 49
Q43 FDV305N G
FAN_EN 35

IO_1V8
IO_3V3
IO_2V5
IO_1V8 36,37,68
IO_3V3 69
IO_2V5 36,68

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FPGA IOs for LVDS links of FMC A Port

U23M

Net	Pin	IO
17 FAHAN0	P15	IO, LVDS3H_1N, DQ32R
17 FAHAP0	P14	IO, LVDS3H_1P, DQ32R
17 FAHAN1	N14	IO, LVDS3H_2N, DQ32R
17 FAHAP1	M14	IO, LVDS3H_2P, DQ32R
17 FAHAN2	J14	IO, LVDS3H_3N, DQ32R
17 FAHAP2	J13	IO, LVDS3H_3P, DQ32R
17 FAHAN3	L15	IO, LVDS3H_4N, DQSN32R
17 FAHAP3	L14	IO, LVDS3H_4P, DQS32R
17 FAHAN4	L13	IO, LVDS3H_5N, DQ32R
17 FAHAP4	L12	IO, LVDS3H_5P, DQ32R
17 FAHAN5	K13	IO, LVDS3H_6N, DQ32R
17 FAHAP5	K12	IO, LVDS3H_6P, DQ32R
17 FALAN0	H14	IO, LVDS3H_7N, DQ33R
17 FALAP0	G14	IO, LVDS3H_7P, DQ33R
17 FALAN3	D14	IO, LVDS3H_8N, DQ33R
17 FALAP3	C14	IO, LVDS3H_8P, DQ33R
17 FALAN2	D13	IO, LVDS3H_9N, DQ33R
17 FALAP2	C13	IO, LVDS3H_9P, DQ33R
43 FA_LA_DEVCLK_N	E13	IO, PLL_3H_CLKOUT1N, LVDS3H_10N, DQSN33R
43 FA_LA_DEVCLK_P	E12	IO, PLL_3H_CLKOUT1P, PLL_3H_CLKOUT1, PLL_3H_FB1, LVDS3H_10P, DQS33R
17 FALAN4	H13	IO, LVDS3H_11N, DQ33R
	H12	IO, RZQ_3H, LVDS3H_11P, DQ33R
43 FA_LA_SYSREF_N	F14	IO, CLK_3H_1N, LVDS3H_12N, DQ33R
43 FA_LA_SYSREF_P	F13	IO, CLK_3H_1P, LVDS3H_12P, DQ33R
17 FAHAN6	C12	IO, CLK_3H_0N, LVDS3H_13N, DQ34R
17 FAHAP6	C11	IO, CLK_3H_0P, LVDS3H_13P, DQ34R
17 FAHAN7	E11	IO, LVDS3H_14N, DQ34R
17 FAHAP7	D11	IO, LVDS3H_14P, DQ34R
17 FAHAN8	G12	IO, PLL_3H_CLKOUT0N, LVDS3H_15N, DQ34R
17 FAHAP8	F12	IO, PLL_3H_CLKOUT0P, PLL_3H_CLKOUT0, PLL_3H_FB0, LVDS3H_15P, DQ34R
17 FAHAN9	G10	IO, LVDS3H_16N, DQSN34R
17 FAHAP9	F10	IO, LVDS3H_16P, DQS34R
17 FAHAN10	E10	IO, LVDS3H_17N, DQ34R
17 FAHAP10	D10	IO, LVDS3H_17P, DQ34R
17 FAHAN11	H11	IO, LVDS3H_18N, DQ34R
17 FAHAP11	G11	IO, LVDS3H_18P, DQ34R
17 FALAN6	B10	IO, LVDS3H_19N, DQ35R
17 FALAP6	A10	IO, LVDS3H_19P, DQ35R
17 FALAN7	B9	IO, LVDS3H_20N, DQ35R
17 FALAP7	A9	IO, LVDS3H_20P, DQ35R
17 FALAN8	B12	IO, LVDS3H_21N, DQ35R
17 FALAP8	B11	IO, LVDS3H_21P, DQ35R
17 FALAN9	A13	IO, LVDS3H_22N, DQSN35R
17 FALAP9	A12	IO, LVDS3H_22P, DQS35R
17 FALAN10	A8	IO, LVDS3H_23N, DQ35R
17 FALAP10	A7	IO, LVDS3H_23P, DQ35R
17 FALAN11	D9	IO, LVDS3H_24N, DQ35R
17 FALAP11	C9	IO, LVDS3H_24P, DQ35R

IO BANK 3H, 1V8 BANK

A10SOC_1517

U23N

Net	Pin	IO
17 FAHAN12	F8	IO, LVDS3G_1N, DQ36R
17 FAHAP12	E8	IO, LVDS3G_1P, DQ36R
17 FAHAN13	C7	IO, LVDS3G_2N, DQ36R
17 FAHAP13	B7	IO, LVDS3G_2P, DQ36R
17 FAHAN14	D8	IO, LVDS3G_3N, DQ36R
17 FAHAP14	C8	IO, LVDS3G_3P, DQ36R
17 FAHAN15	C6	IO, LVDS3G_4N, DQSN36R
17 FAHAP15	B6	IO, LVDS3G_4P, DQS36R
17 FAHAN16	B5	IO, LVDS3G_5N, DQ36R
17 FAHAP16	A5	IO, LVDS3G_5P, DQ36R
17 FAHAN17	B4	IO, LVDS3G_6N, DQ36R
17 FAHAP17	A4	IO, LVDS3G_6P, DQ36R
17 FALAN20	C4	IO, LVDS3G_7N, DQ37R
17 FALAP20	C3	IO, LVDS3G_7P, DQ37R
17 FALAN21	D3	IO, LVDS3G_8N, DQ37R
17 FALAP21	C2	IO, LVDS3G_8P, DQ37R
17 FAHAN22	F7	IO, LVDS3G_9N, DQ37R
17 FAHAP22	E7	IO, LVDS3G_9P, DQ37R
17 FALAN15	D5	IO, PLL_3G_CLKOUT1N, LVDS3G_10N, DQSN37R
17 FALAP15	D4	IO, PLL_3G_CLKOUT1P, PLL_3G_CLKOUT1, PLL_3G_FB1, LVDS3G_10P, DQS37R
17 FALAN16	E6	IO, LVDS3G_11N, DQ37R
	D6	IO, RZQ_3G, LVDS3G_11P, DQ37R
	F5	IO, CLK_3G_1N, LVDS3G_12N, DQ37R
	E5	IO, CLK_3G_1P, LVDS3G_12P, DQ37R
17 FAHAN19	H9	IO, CLK_3G_0N, LVDS3G_13N, DQ38R
17 FAHAP19	H8	IO, CLK_3G_0P, LVDS3G_13P, DQ38R
17 FALAN17	G9	IO, LVDS3G_14N, DQ38R
17 FALAP17	F9	IO, LVDS3G_14P, DQ38R
	K8	IO, PLL_3G_CLKOUT0N, LVDS3G_15N, DQ38R
	J8	IO, PLL_3G_CLKOUT0P, PLL_3G_CLKOUT0, PLL_3G_FB0, LVDS3G_15P, DQ38R
17 FALAN19	G6	IO, LVDS3G_16N, DQSN38R
17 FALAP19	G5	IO, LVDS3G_16P, DQS38R
17 FALAN18	H7	IO, LVDS3G_17N, DQ38R
17 FALAP18	G7	IO, LVDS3G_17P, DQ38R
17 FAHAN23	J6	IO, LVDS3G_18N, DQ38R
17 FAHAP23	H6	IO, LVDS3G_18P, DQ38R
17 FAHAN20	L10	IO, LVDS3G_19N, DQ39R
17 FAHAP20	K10	IO, LVDS3G_19P, DQ39R
17 FALAN13	K11	IO, LVDS3G_20N, DQ39R
17 FALAP13	J11	IO, LVDS3G_20P, DQ39R
17 FALAN12	N13	IO, LVDS3G_21N, DQ39R
17 FALAP12	M12	IO, LVDS3G_21P, DQ39R
17 FAHAN21	N11	IO, LVDS3G_22N, DQSN39R
17 FAHAP21	M10	IO, LVDS3G_22P, DQS39R
17 FALAN14	J10	IO, LVDS3G_23N, DQ39R
17 FALAP14	J9	IO, LVDS3G_23P, DQ39R
17 FAHAN18	N12	IO, LVDS3G_24N, DQ39R
17 FAHAP18	M11	IO, LVDS3G_24P, DQ39R

IO BANK 3G, 1V8 BANK

A10SOC_1517

17 FALAP16 — 0 R670 — RZQ_3G

R658 DNI — 43 FPGA_RCLK_3Gn / 43 FPGA_RCLK_3Gp

17 FALAP4 — 0 R671 — RZQ_3H

R659 DNI

43 FA_EMI_CLKN
43 FA_EMI_CLKP
R653 100

Title: **Arria 10 SoC FPGA Development Kit Board**

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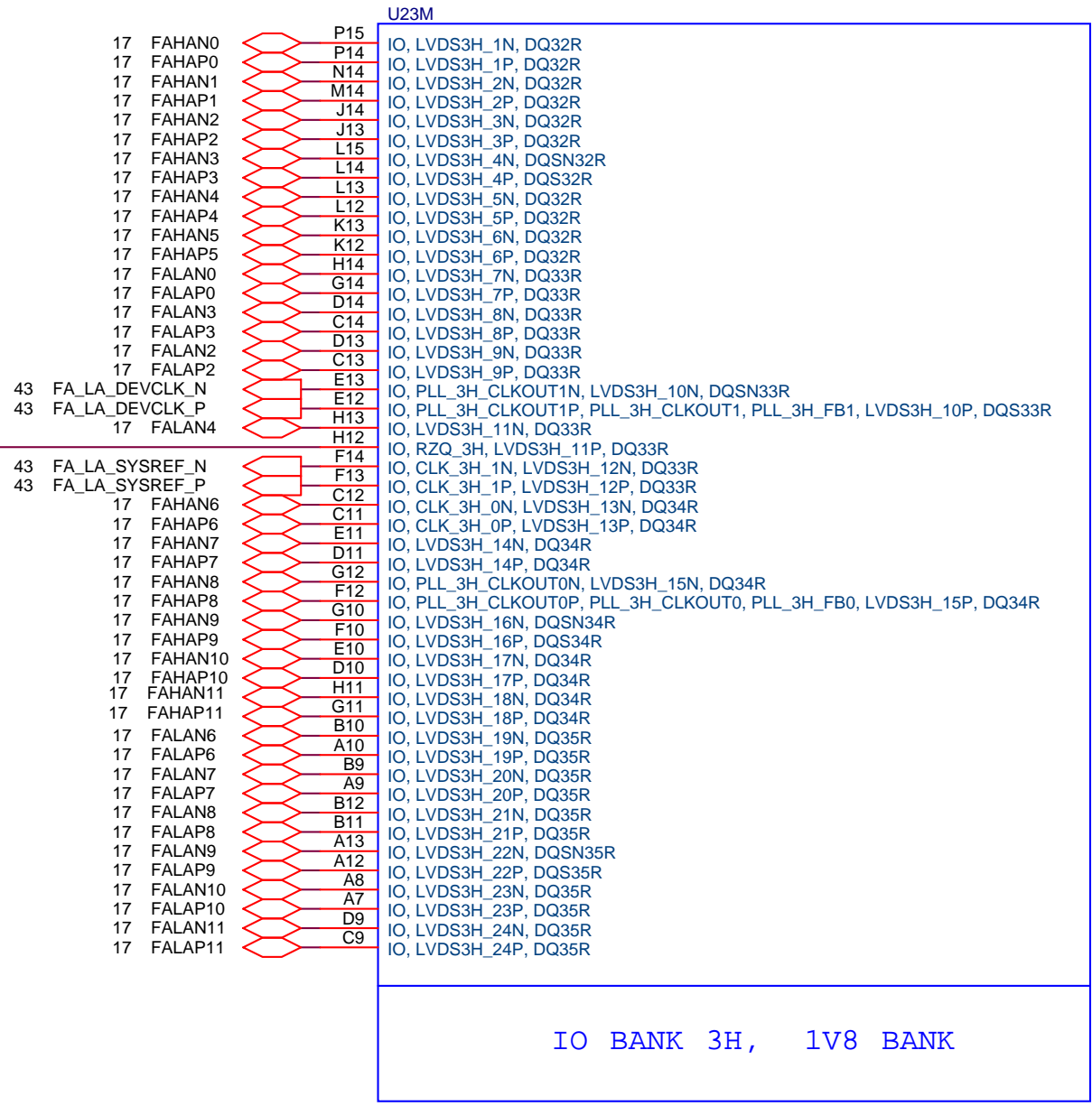Date: Thursday, March 31, 2016   Sheet   28   of   78

FPGA IOs for LVDS links of FMC A Port and FMC B Port

U23O

Ref	Pin	Signal
17	FALAN22	G4	IO, LVDS3F_1N, DQ40R
17	FALAP22	F4	IO, LVDS3F_1P, DQ40R
17	FALAN23	D1	IO, LVDS3F_2N, DQ40R
17	FALAP23	C1	IO, LVDS3F_2P, DQ40R
17	FALAN24	E2	IO, LVDS3F_3N, DQ40R
17	FALAP24	E1	IO, LVDS3F_3P, DQ40R
17	FALAN25	F3	IO, LVDS3F_4N, DQSN40R
17	FALAP25	E3	IO, LVDS3F_4P, DQS40R
17	FALAN26	G2	IO, LVDS3F_5N, DQ40R
17	FALAP26	F2	IO, LVDS3F_5P, DQ40R
17	FALAN27	H2	IO, LVDS3F_6N, DQ40R
17	FALAP27	G1	IO, LVDS3F_6P, DQ40R
17	FAHBN0	J5	IO, LVDS3F_7N, DQ41R
17	FAHBP0	J4	IO, LVDS3F_7P, DQ41R
17	FAHBN1	J1	IO, LVDS3F_8N, DQ41R
17	FAHBP1	H1	IO, LVDS3F_8P, DQ41R
17	FAHBN2	H4	IO, LVDS3F_9N, DQ41R
17	FAHBP2	H3	IO, LVDS3F_9P, DQ41R
17	FAHBN3	K2	IO, PLL_3F_CLKOUT1N, LVDS3F_10N, DQSN41R
17	FAHBP3	K1	IO, PLL_3F_CLKOUT1P, PLL_3F_CLKOUT1, PLL_3F_FB1, LVDS3F_10P, DQS41R
17	FAHBN4	L3	IO, LVDS3F_11N, DQ41R
		L2	IO, RZQ_3F, LVDS3F_11P, DQ41R
17	FAHBN5	K3	IO, CLK_3F_1N, LVDS3F_12N, DQ41R
17	FAHBP5	J3	IO, CLK_3F_1P, LVDS3F_12P, DQ41R
17	FAHBN6	N7	IO, CLK_3F_0N, LVDS3F_13N, DQ42R
17	FAHBP6	N6	IO, CLK_3F_0P, LVDS3F_13P, DQ42R
17	FAHBN7	K6	IO, LVDS3F_14N, DQ42R
17	FAHBP7	K5	IO, LVDS3F_14P, DQ42R
17	FAHBN8	L7	IO, PLL_3F_CLKOUT0N, LVDS3F_15N, DQ42R
17	FAHBP8	K7	IO, PLL_3F_CLKOUT0P, PLL_3F_CLKOUT0, PLL_3F_FB0, LVDS3F_15P, DQ42R
17	FAHBN9	M7	IO, LVDS3F_16N, DQSN42R
17	FAHBP9	M6	IO, LVDS3F_16P, DQS42R
17	FAHBN10	M4	IO, LVDS3F_17N, DQ42R
17	FAHBP10	L4	IO, LVDS3F_17P, DQ42R
17	FALAN28	M5	IO, LVDS3F_18N, DQ42R
17	FALAP28	L5	IO, LVDS3F_18P, DQ42R
17	FALAN29	P10	IO, LVDS3F_19N, DQ43R
17	FALAP29	N9	IO, LVDS3F_19P, DQ43R
17	FAHBN13	M9	IO, LVDS3F_20N, DQ43R
17	FAHBP13	N8	IO, LVDS3F_20P, DQ43R
17	FALAN30	R10	IO, LVDS3F_21N, DQ43R
17	FALAP30	P9	IO, LVDS3F_21P, DQ43R
17	FALAN31	R8	IO, LVDS3F_22N, DQSN43R
17	FALAP31	P8	IO, LVDS3F_22P, DQS43R
17	FALAN33	R11	IO, LVDS3F_23N, DQ43R
17	FALAP33	P11	IO, LVDS3F_23P, DQ43R
17	FALAN32	L9	IO, LVDS3F_24N, DQ43R
17	FALAP32	L8	IO, LVDS3F_24P, DQ43R

IO BANK 3F, 1V8 BANK

A10SOC_1517

U23P

Ref	Pin	Signal
36	FPGAIO9_N	M2	IO, LVDS3E_1N, DQ44R
36	FPGAIO9_P	M1	IO, LVDS3E_1P, DQ44R
36	FPGAIO8_N	N4	IO, LVDS3E_2N, DQ44R
36	FPGAIO8_P	N3	IO, LVDS3E_2P, DQ44R
36	FPGAIO7_N	R3	IO, LVDS3E_3N, DQ44R
36	FPGAIO7_P	R2	IO, LVDS3E_3P, DQ44R
36	FPGAIO6_N	N2	IO, LVDS3E_4N, DQSN44R
36	FPGAIO6_P	N1	IO, LVDS3E_4P, DQS44R
36	FPGAIO5_N	R1	IO, LVDS3E_5N, DQ44R
36	FPGAIO5_P	P1	IO, LVDS3E_5P, DQ44R
36	FPGAIO4_N	P4	IO, LVDS3E_6N, DQ44R
36	FPGAIO4_P	P3	IO, LVDS3E_6P, DQ44R
36	FPGAIO3_N	P6	IO, LVDS3E_7N, DQ45R
36	FPGAIO3_P	P5	IO, LVDS3E_7P, DQ45R
36	FPGAIO2_N	T5	IO, LVDS3E_8N, DQ45R
36	FPGAIO2_P	R5	IO, LVDS3E_8P, DQ45R
43	FBHA_N6	U7	IO, LVDS3E_9N, DQ45R
43	FBHA_P6	T7	IO, LVDS3E_9P, DQ45R
43	FPGA_Refsys_3En	U6	IO, PLL_3E_CLKOUT1N, LVDS3E_10N, DQSN45R
43	FPGA_Refsys_3Ep	U5	IO, PLL_3E_CLKOUT1P, PLL_3E_CLKOUT1, PLL_3E_FB1, LVDS3E_10P, DQS45R
		V7	IO, LVDS3E_11N, DQ45R
		V6	IO, RZQ_3E, LVDS3E_11P, DQ45R
		W6	IO, CLK_3E_1N, LVDS3E_12N, DQ45R
		W5	IO, CLK_3E_1P, LVDS3E_12P, DQ45R
		U4	IO, CLK_3E_0N, LVDS3E_13N, DQ46R
18	FBLAN20	T4	IO, CLK_3E_0P, LVDS3E_13P, DQ46R
18	FBLAP20	T3	IO, LVDS3E_14N, DQ46R
18	FBLAN21	T2	IO, LVDS3E_14P, DQ46R
18	FBLAP21	U2	IO, PLL_3E_CLKOUT0N, LVDS3E_15N, DQ46R
18	FBLAN22	U1	IO, PLL_3E_CLKOUT0P, PLL_3E_CLKOUT0, PLL_3E_FB0, LVDS3E_15P, DQ46R
18	FBLAP22	V2	IO, LVDS3E_16N, DQSN46R
18	FBLAN23	V1	IO, LVDS3E_16P, DQS46R
18	FBLAP23	W4	IO, LVDS3E_17N, DQ46R
18	FBLAN24	W3	IO, LVDS3E_17P, DQ46R
18	FBLAP24	V4	IO, LVDS3E_18N, DQ46R
18	FBLAN25	V3	IO, LVDS3E_18P, DQ46R
18	FBLAP25	U10	IO, LVDS3E_19N, DQ47R
18	FBLAN26	U9	IO, LVDS3E_19P, DQ47R
18	FBLAP26	V9	IO, LVDS3E_20N, DQ47R
18	FBLAN27	V8	IO, LVDS3E_20P, DQ47R
18	FBLAP27	T9	IO, LVDS3E_21N, DQ47R
43	FBHA_N23	T8	IO, LVDS3E_21P, DQ47R
43	FBHA_P23	W10	IO, LVDS3E_22N, DQSN47R
18	FBHA_N20	W9	IO, LVDS3E_22P, DQS47R
18	FBHA_P20	V11	IO, LVDS3E_23N, DQ47R
43	FBHA_N21	U11	IO, LVDS3E_23P, DQ47R
43	FBHA_P21	R7	IO, LVDS3E_24N, DQ47R
18	FBHA_N22	R6	IO, LVDS3E_24P, DQ47R
18	FBHA_P22		

IO BANK 3E, 1V8 BANK

A10SOC_1517

43 FBHA_P17 — RZQ_3E
43 Refclk_3En
R609 100
43 Refclk_3Ep

17 FAHBP4 — 0 — R641 — RZQ_3F
R642 DNI

43 FBHA_N17 — 0 — R628
R629 DNI

Title: **Arria 10 SoC FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0321308 (6XX-44382R)	C

FPGA IOs for LVDS links of FMC B Port

U23V

A10SOC_1517

Net	Pin	Signal
18 FBLAN0	AU7	IO, LVDS3A_1N, DQ60R
18 FBLAP0	AV7	IO, LVDS3A_1P, DQ60R
43 FB_LA_DEVCLK_N	AT8	IO, LVDS3A_2N, DQ60R
43 FB_LA_DEVCLK_P	AT7	IO, LVDS3A_2P, DQ60R
18 FBLAN2	AT10	IO, LVDS3A_3N, DQ60R
18 FBLAP2	AT9	IO, LVDS3A_3P, DQ60R
18 FBLAN3	AV8	IO, LVDS3A_4N, DQSN60R
18 FBLAP3	AW8	IO, LVDS3A_4P, DQS60R
18 FBLAN4	AU9	IO, LVDS3A_5N, DQ60R
18 FBLAP4	AV9	IO, LVDS3A_5P, DQ60R
43 FB_LA_SYSREF_N	AW10	IO, LVDS3A_6N, DQ60R
43 FB_LA_SYSREF_P	AW9	IO, LVDS3A_6P, DQ60R
18 FBLAN6	AP8	IO, LVDS3A_7N, DQ61R
18 FBLAP6	AR8	IO, LVDS3A_7P, DQ61R
18 FBLAN7	AU11	IO, LVDS3A_8N, DQ61R
18 FBLAP7	AU10	IO, LVDS3A_8P, DQ61R
18 FBLAN8	AN9	IO, LVDS3A_9N, DQ61R
18 FBLAP8	AP9	IO, LVDS3A_9P, DQ61R
18 FBLAN9	AP10	IO, PLL_3A_CLKOUT1N, LVDS3A_10N, DQSN61R
18 FBLAP9	AR10	IO, PLL_3A_CLKOUT1P, PLL_3A_CLKOUT1, PLL_3A_FB1, LVDS3A_10P, DQS61R
18 FBLAN10	AR12	IO, LVDS3A_11N, DQ61R
	AT12	IO, RZQ_3A, LVDS3A_11P, DQ61R
	AP11	IO, CLK_3A_1N, LVDS3A_12N, DQ61R
	AR11	IO, CLK_3A_1P, LVDS3A_12P, DQ61R
	AL10	IO, CLK_3A_0N, LVDS3A_13N, DQ62R
	AM10	IO, CLK_3A_0P, LVDS3A_13P, DQ62R
18 FBLAN11	AK12	IO, LVDS3A_14N, DQ62R
18 FBLAP11	AK11	IO, LVDS3A_14P, DQ62R
18 FBLAN12	AL12	IO, PLL_3A_CLKOUT0N, LVDS3A_15N, DQ62R
18 FBLAP12	AM12	IO, PLL_3A_CLKOUT0P, PLL_3A_CLKOUT0, PLL_3A_FB0, LVDS3A_15P, DQ62R
18 FBLAN13	AM11	IO, LVDS3A_16N, DQSN62R
18 FBLAP13	AN11	IO, LVDS3A_16P, DQS62R
18 FBLAN14	AL14	IO, LVDS3A_17N, DQ62R
18 FBLAP14	AL13	IO, LVDS3A_17P, DQ62R
18 FBLAN15	AN13	IO, LVDS3A_18N, DQ62R
18 FBLAP15	AN12	IO, LVDS3A_18P, DQ62R
18 FBLAN16	AJ15	IO, LVDS3A_19N, DQ63R
18 FBLAP16	AK15	IO, LVDS3A_19P, DQ63R
18 FBLAN17	AH13	IO, LVDS3A_20N, DQ63R
18 FBLAP17	AH12	IO, LVDS3A_20P, DQ63R
18 FBLAN18	AJ13	IO, LVDS3A_21N, DQ63R
18 FBLAP18	AK13	IO, LVDS3A_21P, DQ63R
18 FBLAN19	AF14	IO, LVDS3A_22N, DQSN63R
18 FBLAP19	AG14	IO, LVDS3A_22P, DQS63R
18 FMB_SYNC_AB	AH14	IO, LVDS3A_23N, DQ63R
18 FMB_SYNC_CD	AJ14	IO, LVDS3A_23P, DQ63R
18 FMB_SYNCN	AF15	IO, LVDS3A_24N, DQ63R
18 FMB_SYNCP	AG15	IO, LVDS3A_24P, DQ63R

IO BANK 3A, 1V8 BANK

18 FBCLK0M2CN

18 FBCLK0M2CP

43 Refclk_3An

43 Refclk_3Ap

R569 100

R573 100

18 FBLAP10 — 0 — R533 — RZQ_3A

R570 DNI

Title: **Arria 10 SoC FPGA Development Kit Board**

Size B
Document Number 150-0321308 (6XX-44382R)
Rev C
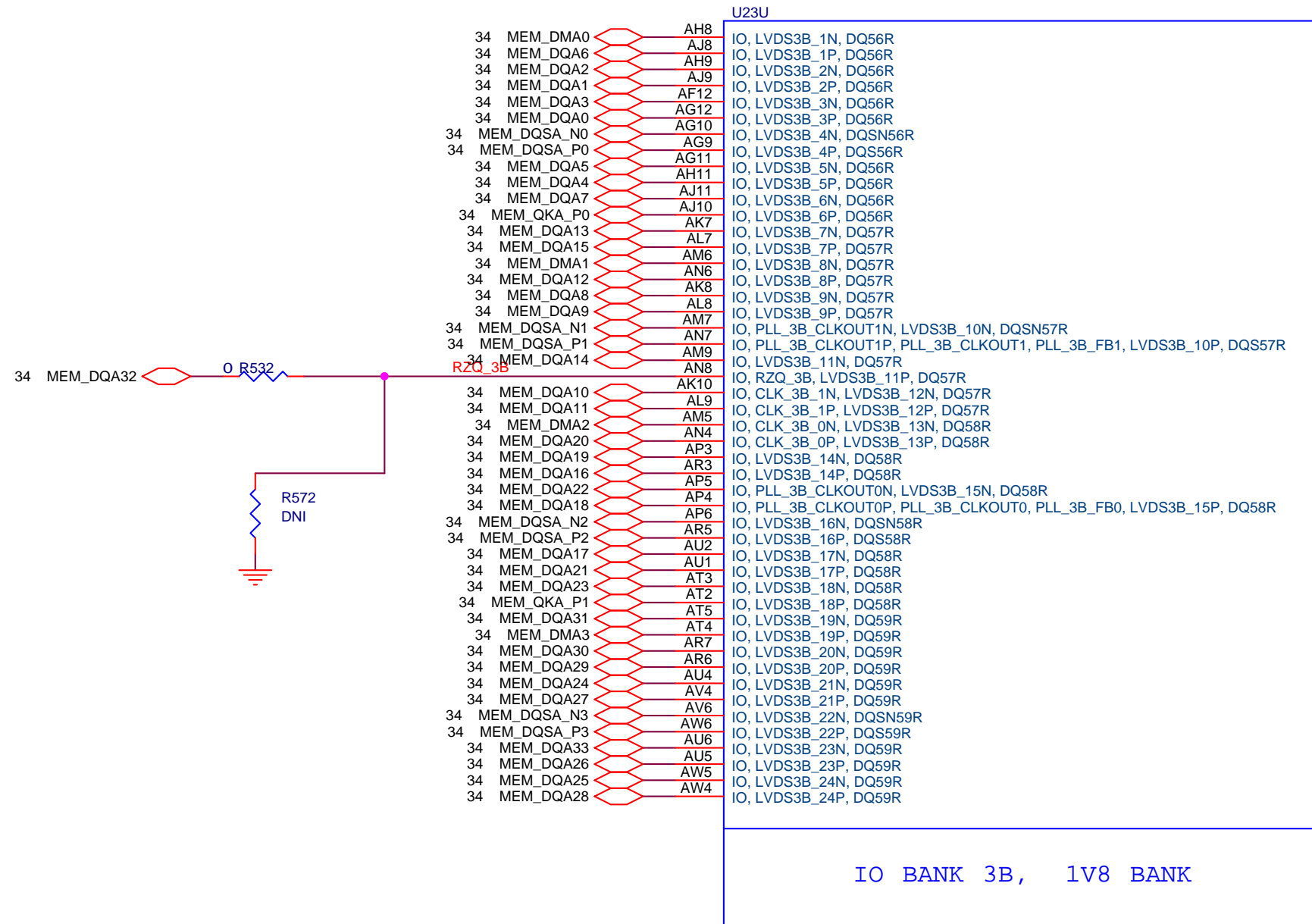Date: Thursday, March 31, 2016
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FPGA IOs for FPGA Memory Interface

U23R

Pin	Signal		IO
34	MEM_DQB4	W8	IO, LVDS3D_1N, DQ48R
34	MEM_DQB0	Y8	IO, LVDS3D_1P, DQ48R
34	MEM_DQB5	Y10	IO, LVDS3D_2N, DQ48R
34	MEM_DQB6	AA9	IO, LVDS3D_2P, DQ48R
34	MEM_DQB1	AB11	IO, LVDS3D_3N, DQ48R
34	MEM_DMB0	AA10	IO, LVDS3D_3P, DQ48R
34	MEM_DQSB_N0	AA8	IO, LVDS3D_4N, DQSN48R
34	MEM_DQSB_P0	AA7	IO, LVDS3D_4P, DQS48R
34	MEM_DQB2	AB10	IO, LVDS3D_5N, DQ48R
34	MEM_DQB3	AB9	IO, LVDS3D_5P, DQ48R
34	MEM_DQB7	AB7	IO, LVDS3D_6N, DQ48R
34	MEM_QKB_P0	AC7	IO, LVDS3D_6P, DQ48R
34	MEM_DQB9	Y7	IO, LVDS3D_7N, DQ49R
34	MEM_DQB8	Y6	IO, LVDS3D_7P, DQ49R
34	MEM_DQB11	Y5	IO, LVDS3D_8N, DQ49R
34	MEM_DQB10	AA5	IO, LVDS3D_8P, DQ49R
34	MEM_DQB14	AD5	IO, LVDS3D_9N, DQ49R
34	MEM_DQB12	AD4	IO, LVDS3D_9P, DQ49R
34	MEM_DQSB_N1	AE6	IO, PLL_3D_CLKOUT1N, LVDS3D_10N, DQSN49R
34	MEM_DQSB_P1	AE5	IO, PLL_3D_CLKOUT1P, PLL_3D_CLKOUT1, PLL_3D_FB1, LVDS3D_10P, DQS49R
34	MEM_DQB13	AC6	IO, LVDS3D_11N, DQ49R
34	MEM_RZQ	AD6	IO, RZQ_3D, LVDS3D_11P, DQ49R
34	MEM_DQB15	AB6	IO, CLK_3D_1N, LVDS3D_12N, DQ49R
34	MEM_DMB1	AB5	IO, CLK_3D_1P, LVDS3D_12P, DQ49R
34	MEM_DQB20	Y3	IO, CLK_3D_0N, LVDS3D_13N, DQ50R
34	MEM_DQB22	Y2	IO, CLK_3D_0P, LVDS3D_13P, DQ50R
34	MEM_DQB17	W1	IO, LVDS3D_14N, DQ50R
34	MEM_DQB18	Y1	IO, LVDS3D_14P, DQ50R
34	MEM_DQB19	AA4	IO, PLL_3D_CLKOUT0N, LVDS3D_15N, DQ50R
34	MEM_DQB16	AB4	IO, PLL_3D_CLKOUT0P, PLL_3D_CLKOUT0, PLL_3D_FB0, LVDS3D_15P, DQ50R
34	MEM_DQSB_N2	AA3	IO, LVDS3D_16N, DQSN50R
34	MEM_DQSB_P2	AA2	IO, LVDS3D_16P, DQS50R
34	MEM_DMB2	AB2	IO, LVDS3D_17N, DQ50R
34	MEM_DQB21	AB1	IO, LVDS3D_17P, DQ50R
34	MEM_DQB23	AC4	IO, LVDS3D_18N, DQ50R
34	MEM_QKB_P1	AC3	IO, LVDS3D_18P, DQ50R
34	MEM_DMB3	AC1	IO, LVDS3D_19N, DQ51R
34	MEM_DQB31	AD1	IO, LVDS3D_19P, DQ51R
34	MEM_DQB30	AD3	IO, LVDS3D_20N, DQ51R
34	MEM_DQB33	AC2	IO, LVDS3D_20P, DQ51R
34	MEM_DQB29	AF2	IO, LVDS3D_21N, DQ51R
34	MEM_DQB28	AG2	IO, LVDS3D_21P, DQ51R
34	MEM_DQSB_N3	AG1	IO, LVDS3D_22N, DQSN51R
34	MEM_DQSB_P3	AH1	IO, LVDS3D_22P, DQS51R
34	MEM_DQB25	AE2	IO, LVDS3D_23N, DQ51R
34	MEM_DQB26	AE1	IO, LVDS3D_23P, DQ51R
34	MEM_DQB24	AE3	IO, LVDS3D_24N, DQ51R
34	MEM_DQB27	AF3	IO, LVDS3D_24P, DQ51R

34 MEM_DQB32

O R589 RZQ_3D

R590 DNI

IO BANK 3D, 1V8 BANK

A10SOC_1517

U23S

Pin	Signal		IO
34	MEM_DQ_ADDR_CMD4	AC9	IO, LVDS3C_1N, DQ52R
34	MEM_DQ_ADDR_CMD3	AC8	IO, LVDS3C_1P, DQ52R
34	MEM_DQ_ADDR_CMD0	AE11	IO, LVDS3C_2N, DQ52R
34	MEM_DQ_ADDR_CMD2	AE10	IO, LVDS3C_2P, DQ52R
34	MEM_DQ_ADDR_CMD1	AD9	IO, LVDS3C_3N, DQ52R
34	MEM_DQ_ADDR_CMD5	AD8	IO, LVDS3C_3P, DQ52R
34	MEM_DQS_ADDR_CMD_N	AE8	IO, LVDS3C_4N, DQSN52R
34	MEM_DQS_ADDR_CMD_P	AF8	IO, LVDS3C_4P, DQS52R
34	MEM_DQ_ADDR_CMD6	AC11	IO, LVDS3C_5N, DQ52R
34	MEM_DQ_ADDR_CMD7	AD10	IO, LVDS3C_5P, DQ52R
34	MEM_DQ_ADDR_CMD8	AF10	IO, LVDS3C_6N, DQ52R
34	MEM_ADDR_CMD29	AF9	IO, LVDS3C_6P, DQ52R
34	MEM_ADDR_CMD18	AG4	IO, LVDS3C_7N, DQ53R
34	MEM_ADDR_CMD17	AH4	IO, LVDS3C_7P, DQ53R
34	MEM_ADDR_CMD16	AF5	IO, LVDS3C_8N, DQ53R
34	MEM_ADDR_CMD19	AF4	IO, LVDS3C_8P, DQ53R
34	MEM_ADDR_CMD26	AE7	IO, LVDS3C_9N, DQ53R
34	MEM_ADDR_CMD15	AF7	IO, LVDS3C_9P, DQ53R
34	MEM_ADDR_CMD14	AH3	IO, PLL_3C_CLKOUT1N, LVDS3C_10N, DQSN53R
34	MEM_ADDR_CMD13	AJ3	IO, PLL_3C_CLKOUT1P, PLL_3C_CLKOUT1, PLL_3C_FB1, LVDS3C_10P, DQS53R
34	MEM_ADDR_CMD12	AG7	IO, LVDS3C_11N, DQ53R
	RZQ_3C	AH7	IO, RZQ_3C, LVDS3C_11P, DQ53R
		AG6	IO, CLK_3C_1N, LVDS3C_12N, DQ53R
		AG5	IO, CLK_3C_1P, LVDS3C_12P, DQ53R
34	MEM_ADDR_CMD11	AH6	IO, CLK_3C_0N, LVDS3C_13N, DQ54R
34	MEM_ADDR_CMD10	AJ5	IO, CLK_3C_0P, LVDS3C_13P, DQ54R
34	MEM_ADDR_CMD9	AJ4	IO, LVDS3C_14N, DQ54R
34	MEM_ADDR_CMD8	AK3	IO, LVDS3C_14P, DQ54R
34	MEM_ADDR_CMD7	AJ6	IO, PLL_3C_CLKOUT0N, LVDS3C_15N, DQ54R
34	MEM_ADDR_CMD6	AK6	IO, PLL_3C_CLKOUT0P, PLL_3C_CLKOUT0, PLL_3C_FB0, LVDS3C_15P, DQ54R
34	MEM_ADDR_CMD5	AK5	IO, LVDS3C_16N, DQSN54R
34	MEM_ADDR_CMD4	AL5	IO, LVDS3C_16P, DQS54R
34	MEM_ADDR_CMD3	AL4	IO, LVDS3C_17N, DQ54R
34	MEM_ADDR_CMD2	AL3	IO, LVDS3C_17P, DQ54R
34	MEM_ADDR_CMD1	AM4	IO, LVDS3C_18N, DQ54R
34	MEM_ADDR_CMD0	AN3	IO, LVDS3C_18P, DQ54R
34	MEM_ADDR_CMD31	AH2	IO, LVDS3C_19N, DQ55R
34	MEM_ADDR_CMD30	AJ1	IO, LVDS3C_19P, DQ55R
34	MEM_CLK_N	AK2	IO, LVDS3C_20N, DQ55R
34	MEM_CLK_P	AK1	IO, LVDS3C_20P, DQ55R
34	MEM_ADDR_CMD21	AN1	IO, LVDS3C_21N, DQ55R
34	MEM_ADDR_CMD20	AM1	IO, LVDS3C_21P, DQ55R
34	MEM_ADDR_CMD25	AR2	IO, LVDS3C_22N, DQSN55R
34	MEM_ADDR_CMD24	AR1	IO, LVDS3C_22P, DQS55R
34	MEM_ADDR_CMD23	AL2	IO, LVDS3C_23N, DQ55R
34	MEM_ADDR_CMD22	AM2	IO, LVDS3C_23P, DQ55R
34	MEM_ADDR_CMD27	AN2	IO, LVDS3C_24N, DQ55R
34	MEM_ADDR_CMD28	AP1	IO, LVDS3C_24P, DQ55R

R583 240

IO BANK 3C, 1V8 BANK

A10SOC_1517

40CLK_EMI_N
40CLK_EMI_P

R582 100

Title: **Arria 10 SoC FPGA Development Kit Board**

Size B
Document Number 150-0321308 (6XX-44382R)
Rev C

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FPGA IOs for FPGA Memory Interface

U23U

Net	Pin	IO Function
34 MEM_DMA0	AH8	IO, LVDS3B_1N, DQ56R
34 MEM_DQA6	AJ8	IO, LVDS3B_1P, DQ56R
34 MEM_DQA2	AH9	IO, LVDS3B_2N, DQ56R
34 MEM_DQA1	AJ9	IO, LVDS3B_2P, DQ56R
34 MEM_DQA3	AF12	IO, LVDS3B_3N, DQ56R
34 MEM_DQA0	AG12	IO, LVDS3B_3P, DQ56R
34 MEM_DQSA_N0	AG10	IO, LVDS3B_4N, DQSN56R
34 MEM_DQSA_P0	AG9	IO, LVDS3B_4P, DQS56R
34 MEM_DQA5	AG11	IO, LVDS3B_5N, DQ56R
34 MEM_DQA4	AH11	IO, LVDS3B_5P, DQ56R
34 MEM_DQA7	AJ11	IO, LVDS3B_6N, DQ56R
34 MEM_QKA_P0	AJ10	IO, LVDS3B_6P, DQ56R
34 MEM_DQA13	AK7	IO, LVDS3B_7N, DQ57R
34 MEM_DQA15	AL7	IO, LVDS3B_7P, DQ57R
34 MEM_DMA1	AM6	IO, LVDS3B_8N, DQ57R
34 MEM_DQA12	AN6	IO, LVDS3B_8P, DQ57R
34 MEM_DQA8	AK8	IO, LVDS3B_9N, DQ57R
34 MEM_DQA9	AL8	IO, LVDS3B_9P, DQ57R
34 MEM_DQSA_N1	AM7	IO, PLL_3B_CLKOUT1N, LVDS3B_10N, DQSN57R
34 MEM_DQSA_P1	AN7	IO, PLL_3B_CLKOUT1P, PLL_3B_CLKOUT1, PLL_3B_FB1, LVDS3B_10P, DQS57R
34 MEM_DQA14	AM9	IO, LVDS3B_11N, DQ57R
RZQ_3B	AN8	IO, RZQ_3B, LVDS3B_11P, DQ57R
34 MEM_DQA10	AK10	IO, CLK_3B_1N, LVDS3B_12N, DQ57R
34 MEM_DQA11	AL9	IO, CLK_3B_1P, LVDS3B_12P, DQ57R
34 MEM_DMA2	AM5	IO, CLK_3B_0N, LVDS3B_13N, DQ58R
34 MEM_DQA20	AN4	IO, CLK_3B_0P, LVDS3B_13P, DQ58R
34 MEM_DQA19	AP3	IO, LVDS3B_14N, DQ58R
34 MEM_DQA16	AR3	IO, LVDS3B_14P, DQ58R
34 MEM_DQA22	AP5	IO, PLL_3B_CLKOUT0N, LVDS3B_15N, DQ58R
34 MEM_DQA18	AP4	IO, PLL_3B_CLKOUT0P, PLL_3B_CLKOUT0, PLL_3B_FB0, LVDS3B_15P, DQ58R
34 MEM_DQSA_N2	AP6	IO, LVDS3B_16N, DQSN58R
34 MEM_DQSA_P2	AR5	IO, LVDS3B_16P, DQS58R
34 MEM_DQA17	AU2	IO, LVDS3B_17N, DQ58R
34 MEM_DQA21	AU1	IO, LVDS3B_17P, DQ58R
34 MEM_DQA23	AT3	IO, LVDS3B_18N, DQ58R
34 MEM_QKA_P1	AT2	IO, LVDS3B_18P, DQ58R
34 MEM_DQA31	AT5	IO, LVDS3B_19N, DQ59R
34 MEM_DMA3	AT4	IO, LVDS3B_19P, DQ59R
34 MEM_DQA30	AR7	IO, LVDS3B_20N, DQ59R
34 MEM_DQA29	AR6	IO, LVDS3B_20P, DQ59R
34 MEM_DQA24	AU4	IO, LVDS3B_21N, DQ59R
34 MEM_DQA27	AV4	IO, LVDS3B_21P, DQ59R
34 MEM_DQSA_N3	AV6	IO, LVDS3B_22N, DQSN59R
34 MEM_DQSA_P3	AW6	IO, LVDS3B_22P, DQS59R
34 MEM_DQA33	AU6	IO, LVDS3B_23N, DQ59R
34 MEM_DQA26	AU5	IO, LVDS3B_23P, DQ59R
34 MEM_DQA25	AW5	IO, LVDS3B_24N, DQ59R
34 MEM_DQA28	AW4	IO, LVDS3B_24P, DQ59R

IO BANK 3B, 1V8 BANK

A10SOC_1517

34 MEM_DQA32 — O R532 — RZQ_3B

R572
DNI

Title: Arria 10 SoC FPGA Development Kit Board

Size B
Document Number 150-0321308 (6XX-44382R)
Rev C

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UART Port B

U61

Pin	Signal
1	EN_n
16	FORCEOFF_N
12	FORCEON
10	INVALID
9	ROUT
11	DIN
15	VCC
14	GND

Pin	Signal
2	C1+
4	C1-
5	C2+
6	C2-
3	V+
7	V-
8	RIN
13	DOUT

MAX3221

C635 0.1uF
C598 0.1uF
C597 0.1uF
C670 0.1uF

35 UART1_RX
35 UART1_TX
69 IO_3V3
IO_3V3

C669 0.1uF

DB9_TX
DB9_RX

J25
5
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11
61800925023

Title
Arria 10 SoC FPGA Development Kit Board

Size
B

Document Number
150-0321308   (6XX-44382R)

Rev
C

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External Memory Interface - HiLo connector

J27A — HiLo EMI - EMI SIGNALS

Net	Pin	Signal	Signal	Pin	Net
31 MEM_ADDR_CMD0	F1	MEM_ADDR_CMD0	MEM_DQ_ADDR_CMD0	R6	MEM_DQ_ADDR_CMD0 31
31 MEM_ADDR_CMD1	H1	MEM_ADDR_CMD1	MEM_DQ_ADDR_CMD1	T1	MEM_DQ_ADDR_CMD1 31
31 MEM_ADDR_CMD2	F2	MEM_ADDR_CMD2	MEM_DQ_ADDR_CMD2	R2	MEM_DQ_ADDR_CMD2 31
31 MEM_ADDR_CMD3	G2	MEM_ADDR_CMD3	MEM_DQ_ADDR_CMD3	T2	MEM_DQ_ADDR_CMD3 31
31 MEM_ADDR_CMD4	H2	MEM_ADDR_CMD4	MEM_DQ_ADDR_CMD4	U3	MEM_DQ_ADDR_CMD4 31
31 MEM_ADDR_CMD5	J2	MEM_ADDR_CMD5	MEM_DQ_ADDR_CMD5	T4	MEM_DQ_ADDR_CMD5 31
31 MEM_ADDR_CMD6	K2	MEM_ADDR_CMD6	MEM_DQ_ADDR_CMD6	U4	MEM_DQ_ADDR_CMD6 31
31 MEM_ADDR_CMD7	G3	MEM_ADDR_CMD7	MEM_DQ_ADDR_CMD7	T5	MEM_DQ_ADDR_CMD7 31
31 MEM_ADDR_CMD8	J3	MEM_ADDR_CMD8	MEM_DQ_ADDR_CMD8	T5	MEM_DQ_ADDR_CMD8 31
31 MEM_ADDR_CMD9	L3	MEM_ADDR_CMD9			
31 MEM_ADDR_CMD10	E4	MEM_ADDR_CMD10			
31 MEM_ADDR_CMD11	F4	MEM_ADDR_CMD11	MEM_DQS_ADDR_CMD_P	V4	MEM_DQS_ADDR_CMD_P 31
31 MEM_ADDR_CMD12	G4	MEM_ADDR_CMD12	MEM_DQS_ADDR_CMD_N	V5	MEM_DQS_ADDR_CMD_N 31
31 MEM_ADDR_CMD13	H4	MEM_ADDR_CMD13			
31 MEM_ADDR_CMD14	J4	MEM_ADDR_CMD14	MEM_CLK_P	V1	MEM_CLK_P 31
31 MEM_ADDR_CMD15	K4	MEM_ADDR_CMD15	MEM_CLK_N	V2	MEM_CLK_N 31
31 MEM_ADDR_CMD16	M1	MEM_ADDR_CMD16			
31 MEM_ADDR_CMD17	M2	MEM_ADDR_CMD17			
31 MEM_ADDR_CMD18	N2	MEM_ADDR_CMD18	CONFIG0	L6	
31 MEM_ADDR_CMD19	L4	MEM_ADDR_CMD19	CONFIG1	M6	
31 MEM_ADDR_CMD20	P5	MEM_ADDR_CMD20			
31 MEM_ADDR_CMD21	M5	MEM_ADDR_CMD21			
31 MEM_ADDR_CMD22	P1	MEM_ADDR_CMD22			
31 MEM_ADDR_CMD23	R4	MEM_ADDR_CMD23	RFU2	H5	
31 MEM_ADDR_CMD24	M4	MEM_ADDR_CMD24	RFU3	K5	
31 MEM_ADDR_CMD25	R3	MEM_ADDR_CMD25	RFU4	N6	
31 MEM_ADDR_CMD26	L2	MEM_ADDR_CMD26	RFU5	R7	
31 MEM_ADDR_CMD27	K1	MEM_ADDR_CMD27	RFU6	R8	
31 MEM_ADDR_CMD28	P2	MEM_ADDR_CMD28			
31 MEM_ADDR_CMD29	N4	MEM_ADDR_CMD29			
31 MEM_ADDR_CMD30	P4	MEM_ADDR_CMD30			
31 MEM_ADDR_CMD31	N3	MEM_ADDR_CMD31			

Net	Pin	Signal	Signal	Pin	Net
32 MEM_DMA0	B10	MEM_DMA0	MEM_DMB0	M16	MEM_DMB0 31
32 MEM_DMA1	C4	MEM_DMA1	MEM_DMB1	U16	MEM_DMB1 31
32 MEM_DMA2	B17	MEM_DMA2	MEM_DMB2	U11	MEM_DMB2 31
32 MEM_DMA3	F17	MEM_DMA3	MEM_DMB3	U6	MEM_DMB3 31

Net	Pin	Signal	Signal	Pin	Net
32 MEM_DQA0	A4	MEM_DQA0	MEM_DQB0	H16	MEM_DQB0 31
32 MEM_DQA1	B4	MEM_DQA1	MEM_DQB1	J16	MEM_DQB1 31
32 MEM_DQA2	B5	MEM_DQA2	MEM_DQB2	K16	MEM_DQB2 3164
32 MEM_DQA3	B6	MEM_DQA3	MEM_DQB3	L16	MEM_DQB3 3164
32 MEM_DQA4	A8	MEM_DQA4	MEM_DQB4	H17	MEM_DQB4 3164
32 MEM_DQA5	B8	MEM_DQA5	MEM_DQB5	K17	MEM_DQB5 3164
32 MEM_DQA6	B9	MEM_DQA6	MEM_DQB6	K18	MEM_DQB6 3164
32 MEM_DQA7	A10	MEM_DQA7	MEM_DQB7	L18	MEM_DQB7 3164
32 MEM_DQA8	B1	MEM_DQA8	MEM_DQB8	M17	MEM_DQB8 31
32 MEM_DQA9	B2	MEM_DQA9	MEM_DQB9	N18	MEM_DQB9 31
32 MEM_DQA10	C2	MEM_DQA10	MEM_DQB10	P17	MEM_DQB10 31
32 MEM_DQA11	C3	MEM_DQA11	MEM_DQB11	P18	MEM_DQB11 31
32 MEM_DQA12	E3	MEM_DQA12	MEM_DQB12	R18	MEM_DQB12 31
32 MEM_DQA13	D4	MEM_DQA13	MEM_DQB13	T16	MEM_DQB13 31
32 MEM_DQA14	D1	MEM_DQA14	MEM_DQB14	T17	MEM_DQB14 31
32 MEM_DQA15	D2	MEM_DQA15	MEM_DQB15	T18	MEM_DQB15 31
32 MEM_DQA16	A12	MEM_DQA16	MEM_DQB16	U15	MEM_DQB16 31
32 MEM_DQA17	B12	MEM_DQA17	MEM_DQB17	T14	MEM_DQB17 31
32 MEM_DQA18	B13	MEM_DQA18	MEM_DQB18	U14	MEM_DQB18 31
32 MEM_DQA19	B14	MEM_DQA19	MEM_DQB19	V14	MEM_DQB19 31
32 MEM_DQA20	C15	MEM_DQA20	MEM_DQB20	T13	MEM_DQB20 31
32 MEM_DQA21	A16	MEM_DQA21	MEM_DQB21	T12	MEM_DQB21 31
32 MEM_DQA22	B16	MEM_DQA22	MEM_DQB22	U12	MEM_DQB22 31
32 MEM_DQA23	A18	MEM_DQA23	MEM_DQB23	V12	MEM_DQB23 31
32 MEM_DQA24	C16	MEM_DQA24	MEM_DQB24	T10	MEM_DQB24 31
32 MEM_DQA25	D16	MEM_DQA25	MEM_DQB25	U10	MEM_DQB25 31
32 MEM_DQA26	E16	MEM_DQA26	MEM_DQB26	V10	MEM_DQB26 31
32 MEM_DQA27	F16	MEM_DQA27	MEM_DQB27	T9	MEM_DQB27 31
32 MEM_DQA28	D17	MEM_DQA28	MEM_DQB28	T8	MEM_DQB28 31
32 MEM_DQA29	C18	MEM_DQA29	MEM_DQB29	U7	MEM_DQB29 31
32 MEM_DQA30	D18	MEM_DQA30	MEM_DQB30	V6	MEM_DQB30 31
32 MEM_DQA31	E18	MEM_DQA31	MEM_DQB31	U8	MEM_DQB31 31
32 MEM_DQA32	E2	MEM_DQA32	MEM_DQB32	R16	MEM_DQB32 31
32 MEM_DQA33	G16	MEM_DQA33	MEM_DQB33	T6	MEM_DQB33 31

Net	Pin	Signal	Signal	Pin	Net
32 MEM_DQSA_P0	A6	MEM_DQSA_P0	MEM_DQSB_P0	H18	MEM_DQSB_P0 31
32 MEM_DQSA_N0	A7	MEM_DQSA_N0	MEM_DQSB_N0	J18	MEM_DQSB_N0 31
32 MEM_DQSA_P1	A2	MEM_DQSA_P1	MEM_DQSB_P1	U18	MEM_DQSB_P1 31
32 MEM_DQSA_N1	A3	MEM_DQSA_N1	MEM_DQSB_N1	V18	MEM_DQSB_N1 31
32 MEM_DQSA_P2	A14	MEM_DQSA_P2	MEM_DQSB_P2	V16	MEM_DQSB_P2 31
32 MEM_DQSA_N2	A15	MEM_DQSA_N2	MEM_DQSB_N2	V17	MEM_DQSB_N2 31
32 MEM_DQSA_P3	F18	MEM_DQSA_P3	MEM_DQSB_P3	V8	MEM_DQSB_P3 31
32 MEM_DQSA_N3	G18	MEM_DQSA_N3	MEM_DQSB_N3	V9	MEM_DQSB_N3 31

Net	Pin	Signal	Signal	Pin	Net
32 MEM_QKA_P0	A11	MEM_QKA_N0	MEM_QKB_N0	M18	MEM_QKB_P0 31
32 MEM_QKA_P1	B18	MEM_QKA_N1	MEM_QKB_N1	V13	MEM_QKB_P1 31

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J27B — HiLo EMI - POWER

HILO_VDD

63 HILO_VDD

VEXT = 2.5V

Pin	Signal	Signal	Pin
C7	VDD	VEXT	L11
C9	VDD	VEXT	L13
C11	VDD	VEXT	M8
C13	VDD	VEXT	M10
D6	VDD	VEXT	M12
D8	VDD	VEXT	M14
D10	VDD	VEXT	N7
D12	VDD	VEXT	N9
D14	VDD	VEXT	N11
E7	VDD	VEXT	N13
E9	VDD	VEXT	P8
E11	VDD	VEXT	P10
E13	VDD	VEXT	P12
F6	VDD	VEXT	P14
F8	VDD		
F10	VDD		

VDD = 1.1(DEFAULT)

Net	Pin	Signal
63 HILO_1V2_SETn	G15	VDD_1.2V_SET
63 HILO_1V25_SETn	D5	VDD_1.25V_SET
63 HILO_1V30_SETn	E15	VDD_1.30V_SET
63 HILO_1V35_SETn	J15	VDD_1.35V_SET
63 HILO_1V5_SETn	L15	VDD_1.5V_SET
63 HILO_1V8_SETn	N16	VDD_1.8V_SET

HILO_VDDQ

64 HILO_VDDQ

Pin	Signal	Signal	Pin
F12	VDDQ	2.5V/3.3V (VTT)	J7
F14	VDDQ	2.5V/3.3V (VTT)	J9
G7	VDDQ	2.5V/3.3V (VTT)	K6
G9	VDDQ	2.5V/3.3V (VTT)	K8
G11	VDDQ	2.5V/3.3V (VTT)	K10
G13	VDDQ	2.5V/3.3V (VTT)	K12
H6	VDDQ	2.5V/3.3V (VTT)	J11
H8	VDDQ	2.5V/3.3V (VTT)	L7
H10	VDDQ	2.5V/3.3V (VTT)	L9
H12	VDDQ		

VDDQ = 1.1(DEFAULT)

Pin	Signal
N15	VDDQ_1.1V_SET
P16	VDDQ_1.2V_SET
F5	VDDQ_1.25V_SET
R15	VDDQ_1.30V_SET
R14	VDDQ_1.35V_SET
R12	VDDQ_1.5V_SET
R11	VDDQ_1.8V_SET

Net	Pin	Signal
HILOQ_1V2_SETn		
HILOQ_1V25_SETn		
HILOQ_1V30_SETn		
HILOQ_1V35_SETn		
HILOQ_1V5_SETn		
HILOQ_1V8_SETn		

Pin	Signal
H14	VREF
J13	VREF
K14	VREF

IO_2V5   L11   IO_2V5

IO_3V3   J7   IO_3V3

HILO_VDDQ

R5495   240

R5494   240

C1557   0.1uF

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J27C — HiLo EMI - GND

Pin	Signal	Signal	Pin
A1	GND	GND	J10
A5	GND	GND	J12
A9	GND	GND	J14
A13	GND	GND	J17
A17	GND	GND	K3
B3	GND	GND	K7
B7	GND	GND	K9
B11	GND	GND	K11
B15	GND	GND	K13
C1	GND	GND	K15
C5	GND	GND	L1
C6	GND	GND	L5
C8	GND	GND	L8
C10	GND	GND	L10
C12	GND	GND	L12
C14	GND	GND	L14
C17	GND	GND	L17
D3	GND	GND	M3
D7	GND	GND	M7
D9	GND	GND	M9
D11	GND	GND	M11
D13	GND	GND	M13
D15	GND	GND	M15
E1	GND	GND	N1
E5	GND	GND	N5
E6	GND	GND	N8
E8	GND	GND	N10
E10	GND	GND	N12
E12	GND	GND	N14
E14	GND	GND	N17
E17	GND	GND	P3
F3	GND	GND	P6
F7	GND	GND	P7
F9	GND	GND	P9
F11	GND	GND	P11
F13	GND	GND	P13
F15	GND	GND	P15
G1	GND	GND	R1
G5	GND	GND	R5
G6	GND	GND	R9
G8	GND	GND	R10
G10	GND	GND	R13
G12	GND	GND	R17
G14	GND	GND	T3
G17	GND	GND	T7
H3	GND	GND	T11
H5	GND	GND	T15
H7	GND	GND	U1
H9	GND	GND	U5
H11	GND	GND	U9
H13	GND	GND	U13
H15	GND	GND	U17
J1	GND	GND	V3
J5	GND	GND	V7
J6	GND	GND	V11
J8	GND	GND	V15

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HILO_VDD

C639	C532	C601
10uF	1uF	0.1uF

Place near HILO connector J14 VDD pins

HILO_VDDQ

C600	C531	C640
10uF	1uF	0.1uF

Place near HILO connector J14 VDDQ pins

5M2210 System Controller

U16A — MAX V BANK1 (5M2210ZF256)

Pin	Left signal		Right signal	Pin
D3	DIFFIO_L1P	DIFFIO_L13P	J4	
C2	DIFFIO_L1N	DIFFIO_L13N	K1	PS_D0 27
C3	DIFFIO_L2P	DIFFIO_L14P	J3	NCONFIG 21 MDCLKR R446 10
E3	DIFFIO_L2N	DIFFIO_L14N	K2	DCLK 21
D2	DIFFIO_L3P	DIFFIO_L15P	K5	CVP_CONFDONE 27 UART_TX
E4	DIFFIO_L3N	DIFFIO_L15N	L1	NSTATUS 21
D1	DIFFIO_L4P	DIFFIO_L16P	L2	CONF_DONE 21
E5	DIFFIO_L4N	DIFFIO_L16N	K3	DEV_CLRN 27
				CRCERROR 27 UART_RX
F3	DIFFIO_L5P	DIFFIO_L17P	M1	dedicated_TX 23
E1	DIFFIO_L5N	DIFFIO_L17N	M2	dedicated_RX 23
F4	DIFFIO_L6P	DIFFIO_L18P	L4	
F2	DIFFIO_L6N	DIFFIO_L18N	L3	FPGA_IO5 27
F1	DIFFIO_L7P	DIFFIO_L19P	N1	FPGA_IO4 27
F6	DIFFIO_L7N	DIFFIO_L19N	M4	ENET_DISABLE_N 27
G2	DIFFIO_L8P	DIFFIO_L20P	N2	RESERVE1 21
G3	DIFFIO_L8N	DIFFIO_L20N	M3	
G1	DIFFIO_L9P	DIFFIO_L21P	N3	PCIE1V8_PERSTn 27
G4	DIFFIO_L9N	DIFFIO_L21N	P2	PCIE1V8_PERST1n 27
H2	DIFFIO_L10P			
G5	DIFFIO_L10N	IOB1_1	E2	BQSPI_RESETn 23
H3	DIFFIO_L11P	IOB1_2	F5	HPS_NPOR 21
J1	DIFFIO_L11N	IOB1_3	H1	HPS_NRST 21
H4	DIFFIO_L12P	IOB1_4	K4	FILE_RESETN 23
J2	DIFFIO_L12N	IOB1_5	L5	dedicated_OE 23
H5	IOB1/CLK0		P3	M5A_JTAG_TCK 38
J5	IOB1/CLK1		L6	M5A_JTAG_TDI 38
		TCK	M5	M5A_JTAG_TDO 38
		TDI	N4	M5A_JTAG_TMS 38
		TDO		
		TMS		

Left pin labels: 21 MSEL0, 21 MSEL1, 21 MSEL2, 23 MFD0, 23 MFD1, 23 MFD2, 23 MFD3, 27 CLK_50M_FPGA, 23 MFCSN, 23 MFCLK, 20 HPSUARTA_TX, 20 HPSUARTA_RX, 20 SPIM1_MOSI, 20 SPIM1_SS0_N, 20 SPIM1_SS1_N, 20 SPIM1_MISO, 36 MAXVtoMAXV0, 36 MAXVtoMAXV1, 36 MAXVtoMAXV2, 36 MAX_IO_CLK, 20 A10SH_GPIO0, 20 A10SH_GPIO1, 20 A10SH_GPIO2, 20 A10SH_GPIO3, 39 CLK_50M_MAX, 20 SPIM1_CLK

U16B — MAX V BANK2 (5M2210ZF256)

Pin	Left signal		Right signal	Pin
D4	DIFFIO_T1P	DIFFIO_T13P	E10	HPS_warm_RESET1n 37
B1	DIFFIO_T1N	DIFFIO_T13N	A11	HPS_warm_RESETn 44
C5	DIFFIO_T2P	DIFFIO_T14P	B11	HPS_cold_RESETn 44
C4	DIFFIO_T2N	DIFFIO_T14N	A12	DC_POWER_CTRL 44
B4	DIFFIO_T3P	DIFFIO_T15P	E11	I2C_flag 42
D6	DIFFIO_T3N	DIFFIO_T15N	B12	PGM_CONFIG 42
E6	DIFFIO_T4P	DIFFIO_T16P	C11	SECURITY_MODE 42
B5	DIFFIO_T4N	DIFFIO_T16N	B13	PGM_LED1 42
A5	DIFFIO_T5P	DIFFIO_T17P	D12	
D7	DIFFIO_T5N	DIFFIO_T17N	B14	MAXVtoMAXV4 36
B6	DIFFIO_T6P	DIFFIO_T18P	C13	MAXVtoMAXV5 36
E7	DIFFIO_T6N	DIFFIO_T18N	B16	MAXVtoMAXV6 36
C8	DIFFIO_T7P			MAXVtoMAXV7 36
B7	DIFFIO_T7N			
D8	DIFFIO_T8P	IOB2_6	A13	MAXVtoMAXV8 36
A7	DIFFIO_T8N	IOB2_7	A15	MAXVtoMAXV9 36
B8	DIFFIO_T9P	IOB2_8	A2	USER_PB_HPS0 42
A8	DIFFIO_T9N	IOB2_9	A6	USER_PB_HPS1 42
A9	DIFFIO_T10P	IOB2_10	A4	USER_PB_HPS2 42
E9	DIFFIO_T10N	IOB2_11	B10	USER_PB_HPS3 42
B9	DIFFIO_T11P	IOB2_12	B3	USER_PB_FPGA0 42
D9	DIFFIO_T11N	IOB2_13	C10	USER_PB_FPGA1 42
A10	DIFFIO_T12P	IOB2_14	C12	USER_PB_FPGA2 42
C9	DIFFIO_T12N	IOB2_15	C6	USER_PB_FPGA3 42
		IOB2_16	C7	MAXVtoMAXV3 36
		IOB2_17	D10	MAXVtoMAXV10 36
		IOB2_18	D11	MAXVtoMAXV11 36
		IOB2_19	D5	MAXVtoMAXV12 36
		IOB2_20	E8	MAXVtoMAXV13 36

Left pin labels: 42 USER_LED_FPGA0, 42 USER_LED_FPGA1, 42 USER_LED_FPGA2, 42 USER_LED_FPGA3, 42 USER_LED_HPS0, 42 USER_LED_HPS1, 42 USER_LED_HPS2, 42 USER_LED_HPS3, 42 MAX_ERROR, 42 MAX_LOAD, 42 MAX_CONF_DONE, 23 File_Presentn, 42 FACTORY_LOAD, 42 PGM_LED0, 42 PGM_SEL, 23 BF_Presentn, 42 USER_DIPSW_HPS0, 42 USER_DIPSW_HPS1, 42 USER_DIPSW_HPS2, 42 USER_DIPSW_HPS3, 42 USER_DIPSW_FPGA0, 42 USER_DIPSW_FPGA1, 42 USER_DIPSW_FPGA2, 42 USER_DIPSW_FPGA3

Q45 DMG2305UX

3V3 — S ... D — MV_3V3, G
C1559 1uF, R5499 10, R5498 4.7K
1V8 23,38,39,55
3V3 37,38,44,53,54,55,65,69,71
2V5 38,68,71

U16C — MAX V BANK3 (5M2210ZF256)

Pin	Left signal		Right signal	Pin
E14	DIFFIO_R1P	DIFFIO_R13P	J14	
C14	DIFFIO_R1N	DIFFIO_R13N	J15	EN0 R481 49.9
C15	DIFFIO_R2P	DIFFIO_R14P	K16	EN8 R453 49.9 A10_EN 55
E13	DIFFIO_R2N	DIFFIO_R14N	K13	A10_0V9_EN 56
E12	DIFFIO_R3P	DIFFIO_R15P	K15	A10_0V95_EN 58,59
D15	DIFFIO_R3N	DIFFIO_R15N	K14	A10_1V0_EN 60
F14	DIFFIO_R4P	DIFFIO_R16P	L16	EN1 R479 49.9 A10_1V8_EN 68
D16	DIFFIO_R4N	DIFFIO_R16N	L11	EN2 R487 49.9 IO_EN 62,63,64,68,69
				PCIE_auxEN 69
F13	DIFFIO_R5P	DIFFIO_R17P	L15	EN3 R483 49.9 PCIE_EN 49,69
E15	DIFFIO_R5N	DIFFIO_R17N	L12	EN4 R486 49.9 FMCA_AUXEN 65
E16	DIFFIO_R6P	DIFFIO_R18P	M16	EN5 R480 49.9 FMCA_EN 49,65,66
F15	DIFFIO_R6N	DIFFIO_R18N	L13	EN6 R485 49.9 FMCB_AUXEN 65
G14	DIFFIO_R7P	DIFFIO_R19P	M15	EN7 R482 49.9 FMCB_EN 49,65,67
F16	DIFFIO_R7N	DIFFIO_R19N	L14	
G13	DIFFIO_R8P	DIFFIO_R20P	N16	IO3V3_Discharge 70
G15	DIFFIO_R8N	DIFFIO_R20N	M13	PLL1V8_discharge 70
G12	DIFFIO_R9P	DIFFIO_R21P	N15	
G16	DIFFIO_R9N	DIFFIO_R21N	N14	LTCNTRL0 73
H14	DIFFIO_R10P	DIFFIO_R22P	P15	LTCNTRL1 73
H15	DIFFIO_R10N	DIFFIO_R22N	P14	LTWDI_RESETN 73
H13	DIFFIO_R11P		D13	FAPRSNT_N 17
H16	DIFFIO_R11N	IOB3_21	D14	FBPRSNT_N 18
J13	DIFFIO_R12P	IOB3_22	F11	USB_VFlagn 25
J16	DIFFIO_R12N	IOB3_23	F12	
		IOB3_24	K12	
		IOB3_25	M14	
		IOB3_26	N13	
		IOB3_27		
J12	IOB3/CLK2			
H12	IOB3/CLK3			

Left pin labels: 56 P0V9Pgood, 59 HPS_Pgood, 58 P0V95Pgood, 60 1V0_Pgood, 54 1V8_Pgood, 53 2V5_Pgood, 51 3V3_Pgood, 42 PGM_LED2, 50 5V0_Pgood, 62 HILOHPS_VDDPGood, 63 HILO_VDDPGood, 64 HILO_VDDQPGood, 66 FMCAVADJPGood, 67 FMCBVADJPGood, 55 10V_Fail_n, 55 10V_good, 73 LTFAUL0, 73 LTPWRGD, 17 FAC2MPgood, 18 FBC2MPgood, 17 FAM2CPgood, 45 TSENSE_ALERTn, 45 OVERTEMPn, 27 FAN_EN, 37 MAXV_USB_CLK

R492 10K

U16D — MAX V BANK4 (5M2210ZF256)

Pin	Left signal		Right signal	Pin
R1	DIFFIO_B1P	DIFFIO_B14P	M10	UART1_RX 33
P4	DIFFIO_B1N	DIFFIO_B14N	R10	UART1_TX 33
T2	DIFFIO_B2P	DIFFIO_B15P	N10	
P5	DIFFIO_B2N	DIFFIO_B15N	T11	LMK_RESET 41
R3	DIFFIO_B3P	DIFFIO_B16P	P10	
N5	DIFFIO_B3N	DIFFIO_B16N	R11	ENET_HPS_RESETn 22
P6	DIFFIO_B4P	DIFFIO_B17P	T12	USB_RESET 25
N6	DIFFIO_B4N	DIFFIO_B17N	N11	
R5	DIFFIO_B5P	DIFFIO_B19P	T13	PCIE_PERSTn 10
M6	DIFFIO_B5N	DIFFIO_B19N	R13	RESET_HPS_UARTA_N 26
T5	DIFFIO_B6P	DIFFIO_B18P	R12	MAX2toMAXV0 37
P7	DIFFIO_B6N	DIFFIO_B18N	P11	MAX2toMAXV1 37
R6	DIFFIO_B7P	DIFFIO_B20P	N12	MAX2toMAXV2 37
N7	DIFFIO_B7N	DIFFIO_B20N	R14	MAX2toMAXV3 37
M7	DIFFIO_B8P	DIFFIO_B21P	P12	MAX2toMAXV4 37
R7	DIFFIO_B8N	DIFFIO_B21N	T15	MAX2toMAXV5 37
P8	DIFFIO_B9P	DIFFIO_B22P	R16	MAX2toMAXV6 37
T7	DIFFIO_B9N	DIFFIO_B22N	P13	MAX2toMAXV7 37
N8	DIFFIO_B10P	IOB4_28	M11	MAX2toMAXV8 37
R8	DIFFIO_B10N	IOB4_29	M12	MAX2toMAXV9 37
T8	DIFFIO_B11P	IOB4_30	N9	MAX2toMAXV10 37
T9	DIFFIO_B11N	IOB4_31	R4	MAX2toMAXV11 37
R9	DIFFIO_B12P	IOB4_32	T10	MAX2toMAXV12 37
P9	DIFFIO_B12N	IOB4_33	T4	MAX2toMAXV13 37
M9	DIFFIO_B13N/DEV_CLRn			
M8	DIFFIO_B13P/DEV_OE			

Left pin labels: 20,45 A10_2L_SDA, 20,45 A10_2L_SCL, 20 A10I2CEN, 27 A10PMBUSEN, 45 A10_PMBUSDIS_N, 26 UARTA_RX, 26 UARTA_TX, 10 PCIE_PRSNT2n, 13 SFPA_LOS, 13 SFPA_TXFAULT, 13 SFPA_TXDISABLE, 13 SFPA_RATESEL0, 13 SFPA_RATESEL1, 14 SFPB_TXDISABLE, 14 SFPB_RATESEL0, 14 SFPB_RATESEL1, 14 SFPB_LOS, 14 SFPB_TXFAULT, 13 SFPA_MOD0_PRSNTn, 14 SFPB_MOD0_PRSNTn, 22 ENET_HPS_INTn, 42 Logic_RESETn, 42 EXT_INTn

U16E — MAX V Power (5M2210ZF256)

Pin	Left		Right	Pin
F7	GNDINT	VCCINT	F10	
G6	GNDINT	VCCINT	G11	
H7	GNDINT	VCCINT	H10	
H9	GNDINT	VCCINT	H8	
J10	GNDINT	VCCINT	J7	
J8	GNDINT	VCCINT	J9	
K11	GNDINT	VCCINT	K6	
L10	GNDINT	VCCINT	L7	
A1	GNDIO	VCCIO1	C1	
A16	GNDIO	VCCIO1	H6	
B2	GNDIO	VCCIO1	J6	
G10	GNDIO	VCCIO1	P1	
G7	GNDIO	VCCIO2	A14	
G8	GNDIO	VCCIO2	A3	
G9	GNDIO	VCCIO2	F8	
K10	GNDIO	VCCIO2	F9	
K7	GNDIO	VCCIO3	C16	
K8	GNDIO	VCCIO3	H11	
K9	GNDIO	VCCIO3	J11	
R15	GNDIO	VCCIO3	P16	
R2	GNDIO	VCCIO4	L8	
T1	GNDIO	VCCIO4	L9	
T16	GNDIO	VCCIO4	T14	
T6	GNDIO	VCCIO4	T3	

1V8, 2V5, MV_3V3

R484 10K MV_3V3
PMbus_ALERTn 45,51,56,73

Decoupling capacitors

VCCINT (1V8): C385, C383, C399, C363, C388, C401, C387, C438 — 0.1uF each
3V3 VCCIO (MV_3V3): C362, C417, C400, C398, C384, C411 — 0.1uF each
1V8 VCCIO: C402, C412, C389 — 0.1uF each
2V5 VCCIO: C356, C355, C386 — 0.1uF each

FPGAIO for DP_IO, SDI_IO and FMC_3V3IO

U21A — MAX V BANK1 (5M2210ZF256)

25 USB_MAXV_D0	D3 DIFFIO_L1P	DIFFIO_L13P J4	FPGAIO7_P 29
25 USB_MAXV_D1	C2 DIFFIO_L1N	DIFFIO_L13N K1	FPGAIO7_N 29
25 USB_MAXV_D2	C3 DIFFIO_L2P	DIFFIO_L14P J3	FPGAIO6_P 29
25 USB_MAXV_D3	E3 DIFFIO_L2N	DIFFIO_L14N K2	FPGAIO6_N 29
25 USB_MAXV_D4	D2 DIFFIO_L3P	DIFFIO_L15P K5	FPGAIO5_P 29
25 USB_MAXV_D5	E4 DIFFIO_L3N	DIFFIO_L15N L1	FPGAIO5_N 29
25 USB_MAXV_D6	D1 DIFFIO_L4P	DIFFIO_L16P L2	FPGAIO4_P 29
25 USB_MAXV_D7	E5 DIFFIO_L4N	DIFFIO_L16N K3	FPGAIO4_N 29

FPGAIO_P / N section:
- 27 FPGAIO12_P F3 DIFFIO_L5P DIFFIO_L17P M1 FPGAIO3_P 29
- 27 FPGAIO12_N E1 DIFFIO_L5N DIFFIO_L17N M2 FPGAIO3_N 29
- 27 FPGAIO11_P F4 DIFFIO_L6P DIFFIO_L18P L4 FPGAIO2_P 29
- 27 FPGAIO11_N F2 DIFFIO_L6N DIFFIO_L18N L3 FPGAIO2_N 29
- 27 FPGAIO10_P F1 DIFFIO_L7P DIFFIO_L19P N1 FPGAIO1_P 27
- 27 FPGAIO10_N F6 DIFFIO_L7N DIFFIO_L19N M4 FPGAIO1_N 27
- 29 FPGAIO9_P   G2 DIFFIO_L8P DIFFIO_L20P N2 FPGAIO_P 27
- 29 FPGAIO9_N   G3 DIFFIO_L8N DIFFIO_L20N M3 FPGAIO_N 27

- 25 USB_MAXV_TXEn G1 DIFFIO_L9P   DIFFIO_L21P N3 MAXVtoMAXV1 35
- 25 USB_MAXV_RXFn G4 DIFFIO_L9N   DIFFIO_L21N P2 MAXVtoMAXV2 35
-                  H2 DIFFIO_L10P
-                  G5 DIFFIO_L10N   IOB1_1 E2
-                  H3 DIFFIO_L11P   IOB1_2 F5   PCIE1V8_PERSTn 27
-                  J1 DIFFIO_L11N   IOB1_3 H1   PCIE1V8_PERST1n 27
- 25 USB_MAXV_RESET H4 DIFFIO_L12P IOB1_4 K4   FPGAIO8_P 29
- 25 USB_MAXV_WR   J2 DIFFIO_L12N IOB1_5 L5   FPGAIO8_N 29
- 25 USB_MAXV_RDn

- 35 MAXVtoMAXV0 H5 IOB1/CLK0
- 35 MAX_IO_CLK   J5 IOB1/CLK1

- TCK P3 M5B_JTAG_TCK 38
- TDI L6 M5B_JTAG_TDI 38
- TDO M5 M5B_JTAG_TDO 38
- TMS N4 M5B_JTAG_TMS 38

U21B — MAX V BANK2 (5M2210ZF256)

- 16 SDI_MF1_SLEEP_MISO D4 DIFFIO_T1P DIFFIO_T13P E10 DP_AUX_DE 15
- 16 SDI_MF3_MOSI   B1 DIFFIO_T1N DIFFIO_T13N A11 DP_AUX_D 15
- 16 SDI_MF2_MUTE_SCLK   C5 DIFFIO_T2P DIFFIO_T14P B11 DP_AUX_REn 15
- 16 SDI_xCS_CS   C4 DIFFIO_T2N DIFFIO_T14N A12 DP_AUX_R 15
- 16 SDI_SPI_CS0   B4 DIFFIO_T3P DIFFIO_T15P E11 DP_CONFIG1 15
- 16 SDI_SPI_MOSI   D6 DIFFIO_T3N DIFFIO_T15N B12 DP_CONFIG2 15
- 16 SDI_SPI_M1SO   E6 DIFFIO_T4P DIFFIO_T16P C11 DP_OCn 15
- 16 SDI_SPI_CLK   B5 DIFFIO_T4N DIFFIO_T16N B13 DP_HOT_PLUG 15

- 39 SI516_FS   A5 DIFFIO_T5P DIFFIO_T17P D12 DP_ON 15
- 16 SDI_TX_SD_HDn   D7 DIFFIO_T5N DIFFIO_T17N B14 MAXVtoMAXV8 35
- 39 SDI_CLK148_DOWN   B6 DIFFIO_T6P DIFFIO_T18P C13 MAXVtoMAXV9 35
- 39 SDI_CLK148_UP   E7 DIFFIO_T6N DIFFIO_T18N B16 MAXVtoMAXV10 35
- 16 SDI_XHD_RATE   C8 DIFFIO_T7P
- 16 SDI_MF4_status   B7 DIFFIO_T7N
- 16 SDI_MF0_BYPASS_present D8 DIFFIO_T8P
-                        A7 DIFFIO_T8N IOB2_6 A13 PCIE_PRSNT2n 10
-                                       IOB2_7 A15 PCIE_WAKE_N 10

- B8 DIFFIO_T9P   IOB2_8 A2   MAXVtoMAXV11 35
- A8 DIFFIO_T9N   IOB2_9 A6   MAXVtoMAXV12 35
- 11 ENETA_INTn A9 DIFFIO_T10P IOB2_10 B10 MAXVtoMAXV13 35
- 11 ENETA_RESETn E9 DIFFIO_T10N IOB2_11 B3   MAXVtoMAXV4 35
- B9 DIFFIO_T11P IOB2_12 C10 MAXVtoMAXV5 35
- D9 DIFFIO_T11N IOB2_13 C12 MAXVtoMAXV6 35
- 12 ENETB_INTn A10 DIFFIO_T12P IOB2_14 C6   MAXVtoMAXV7 35
- 12 ENETB_RESETn C9 DIFFIO_T12N IOB2_15

- IOB2_16 C7   MAXVtoMAXV3 35
- IOB2_17 D10 LMK_RESET 41
- IOB2_18 D11 SPI_CLK 41
- IOB2_19 D5   SPI_SDIO 41
- IOB2_20 E8   SPI_CSn 41

U21C — MAX V BANK3 (5M2210ZF256)

- 17 FAHBP18 E14 DIFFIO_R1P   DIFFIO_R13P J14
- 17 FAHBN18 C14 DIFFIO_R1N   DIFFIO_R13N J15 FAPRSNT_N 17
- 17 FAHBP19 C15 DIFFIO_R2P   DIFFIO_R14P K16
- 17 FAHBN19 E13 DIFFIO_R2N   DIFFIO_R14N K13
- 17 FAHBP20 E12 DIFFIO_R3P   DIFFIO_R15P K15
- 17 FAHBN20 D15 DIFFIO_R3N   DIFFIO_R15N K14
- 17 FAHBP21 F14 DIFFIO_R4P   DIFFIO_R16P L6
- 17 FAHBN21 D16 DIFFIO_R4N   DIFFIO_R16N L11

- F13 DIFFIO_R5P DIFFIO_R17P L15
- E15 DIFFIO_R5N DIFFIO_R17N L12
- E16 DIFFIO_R6P DIFFIO_R18P M16
- F15 DIFFIO_R6N DIFFIO_R18N L13
- 17 FAHBP11 G14 DIFFIO_R7P DIFFIO_R19P M15
- 17 FAHBN11 F16 DIFFIO_R7N DIFFIO_R19N L14
- 17 FAHBP12 G13 DIFFIO_R8P DIFFIO_R20P M16
- 17 FAHBN12 G15 DIFFIO_R8N DIFFIO_R20N M13

- 17 FAHBP14 G12 DIFFIO_R9P   DIFFIO_R21P N15
- 17 FAHBN14 G16 DIFFIO_R9N   DIFFIO_R21N N14
- 17 FAHBP15 H14 DIFFIO_R10P DIFFIO_R22P P15
- 17 FAHBN15 H15 DIFFIO_R10N DIFFIO_R22N P14
- 17 FAHBP17 H13 DIFFIO_R11P
- 17 FAHBN17 H16 DIFFIO_R11N IOB3_21 D13
- 17 FAHBP16 J13 DIFFIO_R12P IOB3_22 D14
- 17 FAHBN16 J16 DIFFIO_R12N IOB3_23 F11

- IOB3_24 F12 FACLKDIR 17
- IOB3_25 K12
- J12 IOB3/CLK2 IOB3_26 M14
- H12 IOB3/CLK3 IOB3_27 N13

U21D — MAX V BANK4 (5M2210ZF256)

- 18 FBHBP18 R1 DIFFIO_B1P DIFFIO_B14P M10 FBPRSNT_N 18
- 18 FBHBN18 P4 DIFFIO_B1N DIFFIO_B14N R10
- 18 FBHBP19 T2 DIFFIO_B2P DIFFIO_B15P N10
- 18 FBHBN19 P5 DIFFIO_B2N DIFFIO_B15N T11
- 18 FBHBP20 R3 DIFFIO_B3P DIFFIO_B16P P10
- 18 FBHBN20 N5 DIFFIO_B3N DIFFIO_B16N R11
- 18 FBHBP21 P6 DIFFIO_B4P DIFFIO_B17P T12 FBLAN28 18
- 18 FBHBN21 N6 DIFFIO_B4N DIFFIO_B17N N11 FBLAP28 18

- R5 DIFFIO_B5P DIFFIO_B19P T13 FBLAP29 18
- M6 DIFFIO_B5N DIFFIO_B19N R13 FBLAN29 18
- T5 DIFFIO_B6P DIFFIO_B18P R12 FBLAP30 18
- P7 DIFFIO_B6N DIFFIO_B18N P11 FBLAN30 18
- R6 DIFFIO_B7P DIFFIO_B20P N12 FBLAP31 18
- N7 DIFFIO_B7N DIFFIO_B20N R14 FBLAN31 18
- M7 DIFFIO_B8P DIFFIO_B21P P12 FBLAP32 18
- R7 DIFFIO_B8N DIFFIO_B21N T15 FBLAN32 18

- P8 DIFFIO_B9P   DIFFIO_B22P R16 FBLAP33 18
- T7 DIFFIO_B9N   DIFFIO_B22N P13 FBLAN33 18
- N8 DIFFIO_B10P IOB4_28 M11
- R8 DIFFIO_B10N IOB4_29 M12
- T8 DIFFIO_B11P IOB4_30 N9
- T9 DIFFIO_B11N IOB4_31 R4
- R9 DIFFIO_B12P IOB4_32 T10
- P9 DIFFIO_B12N IOB4_33 T4

- M9 DIFFIO_B13N/DEV_CLRn
- M8 DIFFIO_B13P/DEV_OE

R5522 0

U21E — MAX V Power (5M2210ZF256)

F7 GNDINT	F10 VCCINT
G6 GNDINT	G11 VCCINT
H7 GNDINT	H10 VCCINT
H9 GNDINT	H8 VCCINT
J10 GNDINT	J7 VCCINT
J8 GNDINT	J9 VCCINT
K11 GNDINT	K6 VCCINT
L10 GNDINT	L7 VCCINT
A1 GNDIO	C1 VCCIO1
A16 GNDIO	H6 VCCIO1
B15 GNDIO	J6 VCCIO1
B2 GNDIO	P1 VCCIO1
G10 GNDIO	A14 VCCIO2
G7 GNDIO	A3 VCCIO2
G8 GNDIO	F8 VCCIO2
G9 GNDIO	F9 VCCIO2
K10 GNDIO	
K7 GNDIO	C16 VCCIO3
K8 GNDIO	H11 VCCIO3
K9 GNDIO	J11 VCCIO3
R15 GNDIO	P16 VCCIO3
R2 GNDIO	
T1 GNDIO	L8 VCCIO4
T16 GNDIO	L9 VCCIO4
T6 GNDIO	T14 VCCIO4
	T3 VCCIO4

Right side connections
- FMCAVADJ 66
- FAM2CVIO
- FMCBVADJ 67
- FBM2CVIO 18
- FMCB_DC_3V3 72
- R522 / R540 0.001 DNI
- R444 / R443 DNI DNI
- R5521
- 0.001
- Vbank3, Vbank4
- IO_1V8
- IO_2V5
- IO_1V8 15,20,21,22,23,25,27,39,40,42,74,77
- IO_2V5 11,12,16,22,24,27,34,39,41,45
- IO_1V8, IO_2V5, Vbank3, Vbank4

Decoupling Capacitors

IO_1V8 VCCINT
C440	C443	C403	C404	C430	C420	C431	C444
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

Vbank3 3V3 VCCIO Vbank4
C464	C490	C465	C433	C415	C445
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

IO_1V8 1V8 VCCIO / IO_2V5 2V5 VCCIO
C442	C432	C421	C429	C441	C478
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

On-Board USB Blaster II - Part 1

U17A — MAX II BANK1 — EPM1270_M256FBGA

U17D — MAX II BANK4 — EPM1270_M256FBGA

U18 — CY7C68013A_QFN

J22 MICRO_USB_CONN

U53 TPD2EUSB30
U20 MAX811
U73 SN74LVC1G17

VBUS_5V R93 10K FX2_WAKEUP
R438 20K   C57 0.1uF
3V3

Y3 24.00MHz IFCLK = 48MHz
C59 12pF   C60 12pF

1M R412
4.7nF C347
100K R97 FX2_RESETn
C425 0.1uF
35 HPS_warm_RESET1n

FX2_SCL R5459 2.00K
FX2_SDA R5460 2.00K

R452 0
R5500 10

PLACE NEAR CY7C68013A
3V3
C396 C369 C407 C361 C377 C368 C360 C408
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF
C1563 0.1uF

IO_1V8 15,20,21,22,23,25,27,33,40,42,74,77
USB_FPGA_CLK 27

FX2_FLAGB
PCIE_TRSTN 10
PCIE_TCK 10
PCIE_TMS 10
FX2_PA1
FX2_PA4
FX2_PA2
FATRST 17
FX2_PA3
PCIE_TDI 10
PCIE_TDO 10
FX2_PA6
FX2_PA5
FB1RST 18
PCIE_PRSNT2n 10

1V8 35,54
3V3 35,42,51
1V8 3V3

FX2_FLAGC
FX2_FLAGA

DNI R474 R467 R475 R477
R434 R428 R472 R468 0
EBLST_JTAG_TCK 38
EBLST_JTAG_TDI 38
EBLST_JTAG_TDO 38
EBLST_JTAG_TMS 38

C_USB_MAX_TCK
C_USB_MAX_TDI
C_USB_MAX_TDO
C_USB_MAX_TMS

R473 R459 R476 R478 0
FX2_PD0 FX2_PD2 FX2_PD3 FX2_PD1

RJTAG_TCK RJTAG_TDI RJTAG_TDO RJTAG_TMS

38 EBLST_ENABLEN
38 EBLST_PROC_RSTn
38 EBLAST_RESERVE0
38 EBLAST_RESERVE1
35 MAXV_USB_CLK

35 MAX2toMAXV0 ... MAX2toMAXV13

FX2_PA7
FX2_SLWRn
FX2_SLRDn
FATMS 17
FATDI 17
FATCK 17
FATDO 17
FBTMS 18
FBTDI 18
FBTCK 18

FX2_PB4 FX2_PB3 FX2_PB2 FX2_PD5 FX2_PD4
FX2_PD7 FX2_PD6
MAX_SDA
18 FBTDO
FX2_RESETn

FX2_PB[0:7]
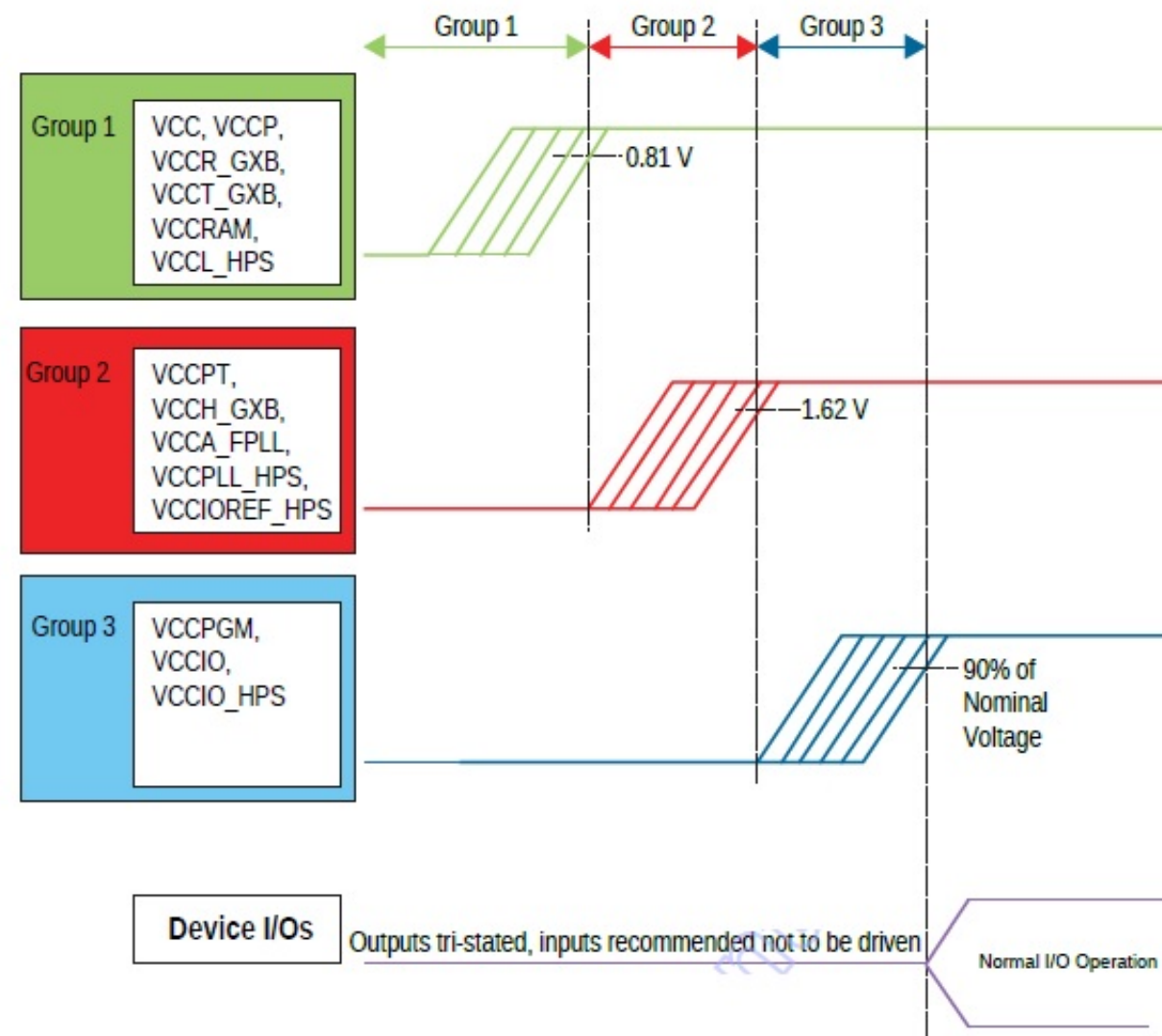FX2_PA[0:7]
FX2_PD[0:7]
MAX_SDA

Title Block

Altera Corporation, 101 innovation Dr, San Jose, CA 95134

Title: **Arria 10 SoC FPGA Development Kit Board**

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On-Board USB Blaster II - Part 2

Logic 0 = Device JTAG Bypass
Logic 1 = Device JTAG Enable

SW3 TDA08H0SB1

16	1	A10_BYPASS
15	2	M5B_BYPASS
14	3	FMCA_BYPASS
13	4	FMCB_BYPASS
12	5	PCIE_BYPASS
11	6	MSTR0
10	7	MSTR1
9	8	MSTR2

U17B — MAX II BANK2 — EPM1270_M256FBGA

A1 IOB2_1 / A10 IOB2_2 / A11 IOB2_3 / A12 IOB2_4 / A13 IOB2_5 / A14 IOB2_6 / A15 IOB2_7 / A16 IOB2_8
B14 IOB2_25 / B15 IOB2_26 / B16 IOB2_27 / B17 IOB2_28 / B18 IOB2_29 / B19 IOB2_30 / B2 IOB2_31 / B3 IOB2_32
A17 IOB2_9 / A18 IOB2_10 / A19 IOB2_11 / A2 IOB2_12 / A20 IOB2_13 / A3 IOB2_14 / A4 IOB2_15 / A5 IOB2_16
B4 IOB2_33 / B5 IOB2_34 / B6 IOB2_35 / B7 IOB2_36 / B8 IOB2_37 / B9 IOB2_38 / C14 IOB2_39 / C15 IOB2_40
A6 IOB2_17 / A7 IOB2_18 / A8 IOB2_19 / A9 IOB2_20 / B10 IOB2_21 / B11 IOB2_22 / B12 IOB2_23 / B13 IOB2_24
C16 IOB2_41 / C5 IOB2_42 / C6 IOB2_43 / C7 IOB2_44 / D13 IOB2_45 / D14 IOB2_46 / D15 IOB2_47 / IOB2_48
D16 IOB2_49 / D5 IOB2_50 / D6 IOB2_51 / D7 IOB2_52 / D8 IOB2_53

JTAG_TX B2
FBPRSNT_N 18 → 1V8
D13 GREEN_LED R409 22.0

MICTOR_JTAG_TRSTn 23
MICTOR_JTAG_TCK 23
MICTOR_JTAG_TMS 23
MICTOR_JTAG_TDI 23
MICTOR_JTAG_TDO 23
MICTOR_PROC_RESETn 23

M5B_JTAG_TDI 36
M5B_JTAG_TDO 36
M5B_JTAG_TMS 36
M5B_JTAG_TCK 36

FTRACE_PROC_RESETN 23
FAPRSNT_N 17
23,27 FTRACE_CLK

D14 GREEN_LED SC_RX
D15 GREEN_LED JTAG_RX / SC_RX
D16 GREEN_LED SC_TX

35 M5A_JTAG_TDI
35 M5A_JTAG_TDO
35 M5A_JTAG_TMS
35 M5A_JTAG_TCK
R407 22.0 / R406 22.0 / R408 22.0 / 1V8
23 FTRACE_JTAG_TDO
23 FTRACE_JTAG_TDI
23 FTRACE_JTAG_TRSTn
23 FTRACE_JTAG_TCK
23 FTRACE_JTAG_TMS

Mode table

MSTR2	MSTR1	MSTR0	Mode
ON	ON	ON	BOOT
OFF	ON	ON	FMCA Master
ON	OFF	ON	FMCB Master
OFF	OFF	ON	Reserved
ON	ON	OFF	FTRACE Master
OFF	ON	OFF	GUI Test
ON	OFF	OFF	SystemMAXV Progrm Mode
OFF	OFF	OFF	ON-board UBII

U17C — MAX II BANK3 — EPM1270_M256FBGA

B20 IOB3_1 / C18 IOB3_2 / C19 IOB3_3 / C20 IOB3_4 / D17 IOB3_5 / D18 IOB3_6 / D19 IOB3_7 / D20 IOB3_8
J20 IOB3_25 / K19 IOB3_26 / K20 IOB3_27 / L19 IOB3_28 / M19 IOB3_29 / N17 IOB3_30 / N19 IOB3_31 / N20 IOB3_32
E17 IOB3_9 / E18 IOB3_10 / E19 IOB3_11 / E20 IOB3_12 / F17 IOB3_13 / F18 IOB3_14 / F19 IOB3_15 / F20 IOB3_16
P17 IOB3_33 / P18 IOB3_34 / P19 IOB3_35 / P20 IOB3_36 / R17 IOB3_37 / R18 IOB3_38 / R19 IOB3_39 / R20 IOB3_40
G17 IOB3_17 / G18 IOB3_18 / G19 IOB3_19 / G20 IOB3_20 / H17 IOB3_21 / H19 IOB3_22 / H20 IOB3_23 / J19 IOB3_24
T17 IOB3_41 / T18 IOB3_42 / T19 IOB3_43 / T20 IOB3_44 / U17 IOB3_45 / U18 IOB3_46 / U19 IOB3_47 / U20 IOB3_48
V19 IOB3_49 / V20 IOB3_50 / W19 IOB3_51 / W20 IOB3_52 / Y20 IOB3_53
M20 IOB3/GCLK2 / L20 IOB3/GCLK3

1V8 R424 DNI R423 DNI R421 DNI R422 DNI

FTRACE_D8 23,27 Direct USB_RDn
FTRACE_D9 23,27 Direct USB_Wrn
FTRACE_D10 23,27 Direct USB_OEn
FTRACE_D11 23,27 Direct USB_RESETn
FTRACE_D12 23,27 Direct USB_EMPTY
FTRACE_D13 23,27 Direct USB_FULL
FTRACE_D14 23,27 Direct USB_SDA
FTRACE_D15 23,27 Direct USB_SCL

FTRACE_D0 23,27
FTRACE_D1 23,27
FTRACE_D2 23,27 Direct USB D[7:0]
FTRACE_D3 23,27
FTRACE_D4 23,27
FTRACE_D5 23,27
FTRACE_D6 23,27
FTRACE_D7 23,27

A10_JTAG_TRST 21
A10_JTAG_TDI 21
A10_JTAG_TCK 21
A10_JTAG_TMS 21
A10_JTAG_TDO 21

U17E — MAX II Power — EPM1270_M256FBGA

J4 / U12 / M17 / D12 GNDINT
K4 / U11 / L17 / D11 VCCINT 2V5

H3 / J3 / M4 / N3 / U9 / V8 / V9 / V13 / H18 / J17 / N18 / C8 / D9 / C12 / C13 / M18 GNDIO

K3 / L3 / L4 / M3 VCCIO1 3V3
C9 / C10 / D10 / C11 VCCIO2 1V8
J18 / K17 / K18 / L18 VCCIO3 3V3
U10 / V10 / V11 / V12 VCCIO4 3V3

USB Blaster Programming Header

(uses JTAG mode only)

R458 DNI C2490 DNI
R5476 1.00k

J24 2X5_100mil

2	1
4	3
6	5
8	7
10	9

R5477 1.00k / 3V3 / 3V3
R5474 1.00k 3V3
R5473 1.00k
R5528 1.00k / 3V3

37 EBLST_PROC_RSTn
37 EBLAST_RESERVE0
EBLAST_RESERVE1 37
37 EBLST_ENABLEN
37 EBLST_JTAG_TCK
37 EBLST_JTAG_TDO
37 EBLST_JTAG_TMS
37 EBLST_JTAG_TDI
R465 0
R466 DNI

PLACE NEAR MAX II (U25)

2V5 / 3V3 / 3V3
C382 / C379 / C397 / C409 / C378 / C410 0.1uF each
1V8 / 1V8
C371 / C381 / C370 / C380 0.1uF each

1V8 35,54
3V3 35,42,51
2V5 35,53

PLL

PCIE reference clock

U11 Si52112

Pin	Signal
1	VDD
10	VDD2
2	XOUT
3	XIN/CLKIN
4	VSS
5	VSS2

DIFF1 6 → CLK_DIFF1_P → R66 0 → PCIE_REFCLK_QR0_P 8 (100MHz)
DIFF1 7 → CLK_DIFF1_N → R65 0 → PCIE_REFCLK_QR0_N 8
DIFF2 8 → CLK_DIFF2_P → R60 0 → PCIE_REFCLK_SYN_P 10 (100MHz)
DIFF2 9 → CLK_DIFF2_N → R58 0 → PCIE_REFCLK_SYN_N 10

Y2 25.00MHz

C271 0.1uF   C253 2.2uF
C254 DNI   C272 DNI

69 IO_3V3
IO_3V3

36,68 IO_2V5
IO_2V5

L3 742792780

C278 0.1uF C260 0.1uF C279 0.1uF C277 0.1uF C302 0.1uF

C259 DNI
Y6 25.00MHz
C258 DNI

R349 DNI
R350 DNI

36,37,68 IO_1V8

1V8_PLL   L21   IO_1V8
C287 0.1uF C303 0.1uF 742792780 C304 0.1uF C40 0.1uF

OSC1_CLK_SEL = HIGH selects (OSC1_CLK_SMA) SMA input
OSC1_CLK_SEL = LOW selects (OSC1_CLK_SYN) Si5356A input

2.5V_CLK_MUX L22 742792780
C311 0.1uF C322 0.1uF
IO_1V8

U42 Si5338A-CUSTOM

Pin	Signal		Pin	Signal
1	CLKIN_P		7	VDD1
2	CLKIN_N		24	VDD2
3	CLKIN		11	VDDO3
4	I2C_LSB		15	VDDO2
5	FDBK_P		16	VDDO1
6	FDBK_N		20	VDDO0
12	SCL		8	INTR
19	SDA		9	CLK3B
			10	CLK3A
			13	CLK2B
			14	CLK2A
			17	CLK1B
			18	CLK1A
			21	CLK0B
			22	CLK0A
23	RSVD_GND		25	EPAD

R149 1.00K

40,45 CLOCK_I2C_SCL
40,45 CLOCK_I2C_SDA

Si5358 Programmable Oscillator Use Clock Control GUI (Defaults 156.25MHz, 156.25MHz,25MHz,25MHz, 25MHz, 25MHz,100MHz, 100MHz)
I2C Address 70 HEX

CLK_3An 43 CLK_3Ap 43 (100MHz)
25Mhz
CLKUSR 27
100Mhz
CLK_3En 43 CLK_3Ep 43
156.25MHz
CMOS

I2C Address = b'1110000'

J15 SMA
R370 DNI R84 DNI

OSC2_CLK_SYN
OSC2_CLK_SMA
OSC2_HPS_CLK

C339 0.01uF
IO_2V5

Y7
OSC_33MHZ
VDD OUT
EN GND

U47 ICS83054I

Pin	Signal		Pin	Signal
14	CLK0		12	VDD
10	CLK1		16	VDDQ
8	CLK2		1	Q
4	CLK3		2	NC1
3	OE		11	NC2
7	SEL1		13	NC3
9	SEL0		5	NC4
			15	NC5
	GND			

R390 22.0 → HPS_CLK1 21

IO_2V5

J16 CON2 1.00K R293
J17 CON2 OSC2_CLK_SEL0 1.00K R292
OSC2_CLK_SEL1

Si5358 Programmable...

2.5V_Si516 IO_2V5
L25
C463 0.1uF C439 10uF BLM15AG221SN1

U54 Si516_148.5M_148.35M

Pin	Signal		Pin	Signal
2	FS(OE)		6	VDD
7	NC(SDA)		4	CLK+
8	NC(SCL)		5	CLK-
3	GND		1	VC

36 SI516_FS

35,54 1V8
REFCLK_SDI_CP C461 0.1uF → REFCLK_SDI_P 9
REFCLK_SDI_CN C462 0.1uF → REFCLK_SDI_N 9
SI571_VCONTROL
148.5MHz

From FPGA
36 SDI_CLK148_UP R490 180K
36 SDI_CLK148_DOWN R491 180K
C419 1.0nF
R469 4.99K
C428 0.1uF

Populated with Si516.
FS Control on DIPSWITCH
FS=0: 148.35MHz
FS=1: 148.50MHz
I2C only available if Si571 is populated.

1V8
R429 10K

IO_1V8
C41 0.1uF C305 0.1uF

U51 50MHz
Pin	Signal	Pin	Signal
1	EN	4	VCC
2	GND	3	OUT

1V8
CLKIN_50
R447 22.0 → CLK_50M_MAX 35
C373 2.2uF C372 0.1uF

41 CP1

IO_3V3
L28 3A, 30 Ohm FB 3.3V_VCXO
C783 0.1uF C782 2.2uF

Y5 122.88 MHz
Pin	Signal	Pin	Signal
1	VC	4	VDD
2	GND	3	OUT

VCXO 41

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IO_1V8

IO_1V8   IO_1V8   36,37,68

U50 — Si5338B-CUSTOM

C345 DNI
Y9 25.00MHz
C344 DNI

1.8V_PLLA   IO_1V8

Pin	Signal
1	CLKIN_P
2	CLKIN_N
3	CLKIN
4	I2C_LSB
5	FDBK_P
6	FDBK_N
7	VDD1
24	VDD2
11	VDDO3
15	VDDO2
16	VDDO1
20	VDDO0
8	INTR

C44 C45 C51 C49 C50 C48
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

L24 BLM15AG221SN1

R85 4.7K

CLOCK_I2C_SCL   39,45
CLOCK_I2C_SDA   39,45

12 SCL
19 SDA

Pin	Signal	Net	Cap	Output
9	CLK3B	REFCLK1_FMCB_CP	C326 0.1uF	REFCLK1_FMCB_P 8
10	CLK3A	REFCLK1_FMCB_CN	C325 0.1uF	REFCLK1_FMCB_N 8
13	CLK2B	REFCLK0_FMCB_CP	C332 0.1uF	REFCLK0_FMCB_P 7
14	CLK2A	REFCLK0_FMCB_CN	C333 0.1uF	REFCLK0_FMCB_N 7
17	CLK1B	REFCLK_DP_CP	C342 0.1uF	REFCLK_DP_P 9
18	CLK1A	REFCLK_DP_CN	C343 0.1uF	REFCLK_DP_N 9
21	CLK0B	ENET_REFCLK_CP	C348 0.1uF	CLK_ENET_FPGA_P 8
22	CLK0A	ENET_REFCLK_CN	C349 0.1uF	CLK_ENET_FPGA_N 8

100MHz
100MHz
270MHz
125MHz

23 RSVD_GND
25 EPAD

LVDS

Si5338B-CUSTOM

I2C Address = b'1110001'

J13
C38 0.1uF EXTSMACLKP   1
J14
C39 0.1uF EXTSMACLKN   1

U49 — Si5338B-CUSTOM

C341 DNI
Y8 25.00MHz
C340 DNI

1.8V_PLLB   IO_1V8

Pin	Signal
1	CLKIN_P
2	CLKIN_N
3	CLKIN
4	I2C_LSB
5	FDBK_P
6	FDBK_N
7	VDD1
24	VDD2
11	VDDO3
15	VDDO2
16	VDDO1
20	VDDO0
8	INTR

C55 C54 C47 C52 C53 C46
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

L23 BLM15AG221SN1

R86 4.7K

12 SCL
19 SDA

Pin	Signal	Net	Cap	Output
9	CLK3B	REFCLK_SMA_CP	C324 DNI	REFCLK_SMA_P 9
10	CLK3A	REFCLK_SMA_CN	C323 DNI	REFCLK_SMA_N 9
13	CLK2B			CLK_FAEMI_P 43
14	CLK2A			CLK_FAEMI_N 43
17	CLK1B			CLK_HPSEMI_P 19
18	CLK1A			CLK_HPSEMI_N 19
21	CLK0B			CLK_EMI_P 31
22	CLK0A			CLK_EMI_N 31

133.33MHz
133.33MHz
133.33MHz
133.33MHz

23 RSVD_GND
25 EPAD

LVDS

Si5338B-CUSTOM

I2C Address = b'1110011'

ALTERA ®

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Clock Cleaner

U26
LMK04828

Pin	Signal	Pin	Signal
10	VCC1_VCO	32	CPOUT1
17	VCC2_GC1	46	CPOUT2
21	VCC3_SYSREF	40	OSCOUTp
26	VCC4_CG2	41	OSCOUTn
33	VCC5_DIG	1	DCLKOUT0p
36	VCC6_PLL1	2	DCLKOUT0n
39	VCC7_OSCout	3	SDCLKOUT1p
42	VCC8_OSCin	4	SDCLKOUT1n
45	VCC9_CP2	15	DCLKOUT2p
47	VCC10_PLL2	16	DCLKOUT2n
53	VCC11_CG3	13	SDCLKOUT3p
64	VCC12_CG0	14	SDCLKOUT3n
18	CS	24	DCLKOUT4p
37	CLKIN0p	25	DCLKOUT4n
38	CLKIN0n	22	SDCLKOUT5p
34	CLKIN1p/FBCLKINp/FINp	23	SDCLKOUT5n
35	CLKIN1n/FBCLKINn/FINn	27	DCLKOUT6p
43	OSCINp	28	DCLKOUT6n
44	OSCINn	29	SDCLKOUT7p
58	CLKin_SEL0	30	SDCLKOUT7n
59	CLKin_SEL1	51	DCLKOUT8p
31	STATUS_LD1	52	DCLKOUT8n
48	STATUS_LD2	49	SDCLKOUT9p
5	RESET	50	SDCLKOUT9n
6	SYNC	54	DCLKOUT10p
19	SCK	55	DCLKOUT10n
20	SDIO	56	SDCLKOUT11p
11	LDObyp1	57	SDCLKOUT11n
12	LDObyp2	62	DCLKOUT12p
65	DAP	63	DCLKOUT12n
		60	SDCLKOUT13p
		61	SDCLKOUT13n

U25
NB6L72MNG

CMOS INPUT -> LVPECL OUTPUT

Pin	Signal	Pin	Signal
13	VCC	4	VTD0
12	VCC	5	VTD1
2	D0p	15	Q0p
3	D0n	14	Q0n
6	D1p	11	Q1p
7	D1n	10	Q1n
1	SEL0	9	GND
8	SEL1	16	GND
		17	GND_PAD

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User I/O

35 MAX_ERROR — MAX_ERROR — D17 Red_LED — R113 100 — 3V3

35 MAX_LOAD — MAX_LOAD — D19 Green_LED — R598 100

35 MAX_CONF_DONE — MAX_CONF_DONE — D18 Green_LED — R115 100

35 PGM_LED0 — PGM_LED0 — D20 Green_LED — R588 100

35 PGM_LED1 — PGM_LED1 — D21 Green_LED — R116 100

35 PGM_LED2 — PGM_LED2 — D22 Green_LED — R117 100

17 FAPRSNT_N — D23 Green_LED — R122 100 — 3V3

18 FBPRSNT_N — D24 Green_LED — R123 100

D42 Green_LED — R5501 100 — 3V3
3V3 Power on LED

35 PGM_CONFIG
35 PGM_SEL
35 Logic_RESETn
35 EXT_INTn

S7 PB Switch
S8 PB Switch
S10 PB Switch
S9 PB Switch

35 USER_PB_HPS0
35 USER_PB_HPS1
35 USER_PB_HPS2
20,35 USER_PB_HPS3

IO_1V8 R5529 10K

S14 PB Switch
S13 PB Switch
S11 PB Switch
S12 PB Switch

35 USER_PB_FPGA0
35 USER_PB_FPGA1
35 USER_PB_FPGA2
35 USER_PB_FPGA3

S3 PB Switch
S5 PB Switch
S6 PB Switch
S4 PB Switch

35 USER_LED_HPS0 — USER_LED_HPS0 — D29 Green_LED — R136 100 — 3V3

35 USER_LED_HPS1 — USER_LED_HPS1 — D32 Green_LED — R139 100

35 USER_LED_HPS2 — USER_LED_HPS2 — D31 Green_LED — R138 100 — IO_3V3

20,35 USER_LED_HPS3 — USER_LED_HPS3 — D30 Green_LED — R137 100

35 USER_LED_FPGA0 — USER_LED_FPGA0 — D26 Green_LED — R126 100 — 3V3

35 USER_LED_FPGA1 — USER_LED_FPGA1 — D25 Green_LED — R125 100

35 USER_LED_FPGA2 — USER_LED_FPGA2 — D28 Green_LED — R128 100

35 USER_LED_FPGA3 — USER_LED_FPGA3 — D27 Green_LED — R127 100

USER_DIPSW_HPS0 35
USER_DIPSW_HPS1 35
USER_DIPSW_HPS2 20,35
USER_DIPSW_HPS3 20,35

R5531 10K — IO_1V8
R5530 10K
R5532 10K

SW2 TDA08H0SB1
16 1
15 2
14 3
13 4
12 5
11 6
10 7
9 8

1V8 23,38,39,55
3V3 37,38,44,53,54,55,65,69,71
2V5 38,68,71

USER_DIPSW_FPGA0 35
USER_DIPSW_FPGA1 35
USER_DIPSW_FPGA2 35
USER_DIPSW_FPGA3 35

SW1 TDA04H0SB1
8 1
7 2
6 3
5 4

I2C_flag 35
DC_POWER_CTRL 35
FACTORY_LOAD 35
SECURITY_MODE 35

IO_3V3 — IO_3V3 69
IO_1V8 — IO_1V8 36,37,68

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Clock Resistor Mux

FMC A Clock MUX for FMC card

17 FALAP1	O R612	LMK_CLK_FMC_P 41
17 FALAN1	O R613	LMK_CLK_FMC_N 41
	DNI R610	FA_LA_DEVCLK_P 28
	DNI R611	FA_LA_DEVCLK_N 28
17 FALAP5	O R621	LMK_SYSREF_FMC_P 41
17 FALAN5	O R633	LMK_SYSREF_FMC_N 41
	DNI R620	FA_LA_SYSREF_P 28
	DNI R632	FA_LA_SYSREF_N 28

FMC B Clock MUX for FMC card

18 FBLAP1	O R361	LMK_CLK_FMCB_P 41
18 FBLAN1	O R365	LMK_CLK_FMCB_N 41
	DNI R360	FB_LA_DEVCLK_P 30
	DNI R364	FB_LA_DEVCLK_N 30
18 FBLAP5	O R373	LMK_SYSREF_FMCB_P 41
18 FBLAN5	O R383	LMK_SYSREF_FMCB_N 41
	DNI R372	FB_LA_SYSREF_P 30
	DNI R382	FB_LA_SYSREF_N 30

Clock MUX for 3A Bank reference clock

30 Refclk_3An	O R354	CLK_3An 39
30 Refclk_3Ap	O R347	CLK_3Ap 39
	DNI R355	FBCLK1M2CN 18
	DNI R348	FBCLK1M2CP 18
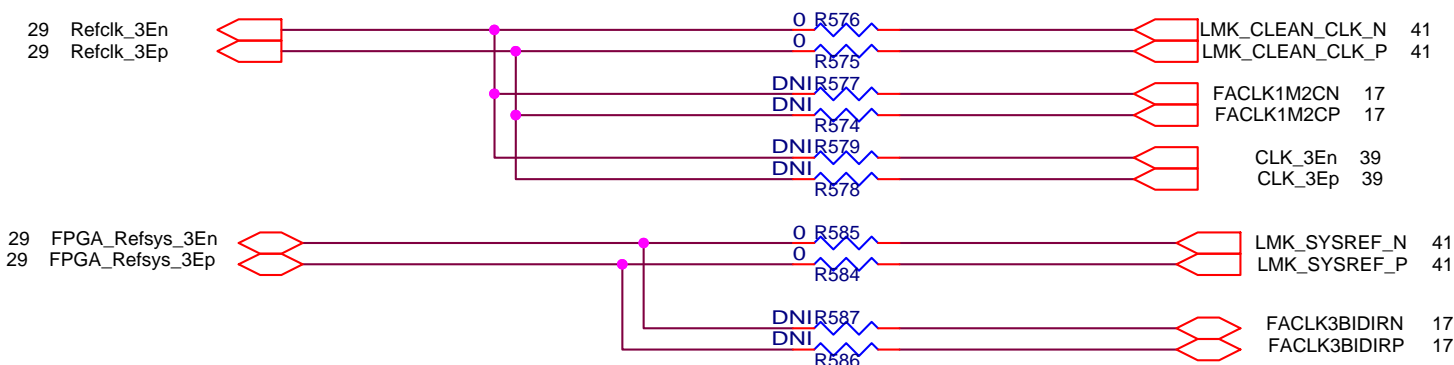
Clock MUX for 3E Bank reference clock

29 Refclk_3En	O R576	LMK_CLEAN_CLK_N 41
29 Refclk_3Ep	O R575	LMK_CLEAN_CLK_P 41
	DNI R577	FACLK1M2CN 17
	DNI R574	FACLK1M2CP 17
	DNI R579	CLK_3En 39
	DNI R578	CLK_3Ep 39
29 FPGA_Refsys_3En	O R585	LMK_SYSREF_N 41
29 FPGA_Refsys_3Ep	O R584	LMK_SYSREF_P 41
	DNI R587	FACLK3BIDIRN 17
	DNI R586	FACLK3BIDIRP 17
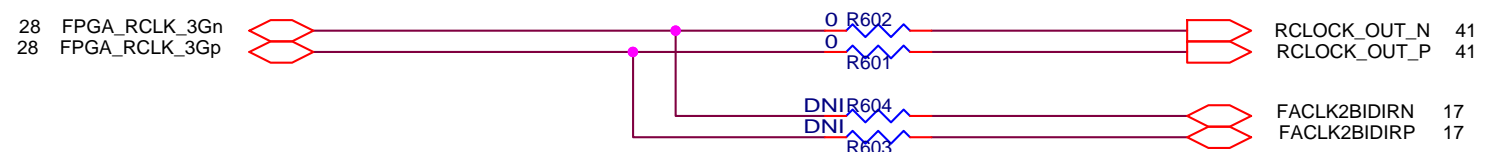
Clock MUX for 3G Bank reference clock

28 FPGA_RCLK_3Gn	O R602	RCLOCK_OUT_N 41
28 FPGA_RCLK_3Gp	O R601	RCLOCK_OUT_P 41
	DNI R604	FACLK2BIDIRN 17
	DNI R603	FACLK2BIDIRP 17
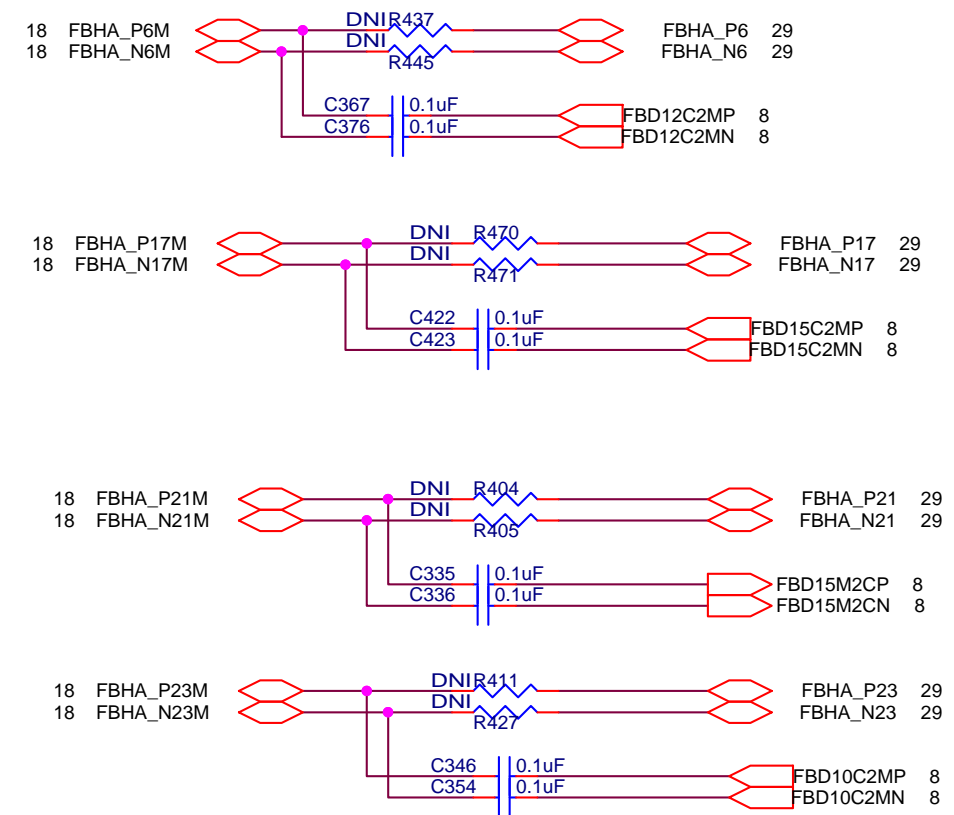
MUX for supporting Altera FMC spec

18 FBHA_P6M	DNI R437	FBHA_P6 29
18 FBHA_N6M	DNI R445	FBHA_N6 29
	C367 0.1uF	FBD12C2MP 8
	C376 0.1uF	FBD12C2MN 8
18 FBHA_P17M	DNI R470	FBHA_P17 29
18 FBHA_N17M	DNI R471	FBHA_N17 29
	C422 0.1uF	FBD15C2MP 8
	C423 0.1uF	FBD15C2MN 8
18 FBHA_P21M	DNI R404	FBHA_P21 29
18 FBHA_N21M	DNI R405	FBHA_N21 29
	C335 0.1uF	FBD15M2CP 8
	C336 0.1uF	FBD15M2CN 8
18 FBHA_P23M	DNI R411	FBHA_P23 29
18 FBHA_N23M	DNI R427	FBHA_N23 29
	C346 0.1uF	FBD10C2MP 8
	C354 0.1uF	FBD10C2MN 8

28 FA_EMI_CLKN	DNI R594	CLK_FAEMI_N 40
28 FA_EMI_CLKP	DNI R593	CLK_FAEMI_P 40
	O R596	FACLK0M2CN 17
	O R595	FACLK0M2CP 17

RESET CIRUIT

3V3

3V3

0.1uF   C357

R430
20K

U14

4 VCC   GND 1

1 S2 2
PB Switch

PB_COLD_RESETn

3 MR   RESET 2

COLD_RESETn R92   100K

MAX811

R440
0

35,42,51   3V3

3V3

HPS_cold_RESETn   35

3V3

3V3

0.1uF   C173

R16
20K

U1

4 VCC   GND 1

1 S1 2
PB Switch

PB_WARM_RESETn

3 MR   RESET 2

WARM_RESETn R294   100K

MAX811

R289
0

HPS_warm_RESETn   35

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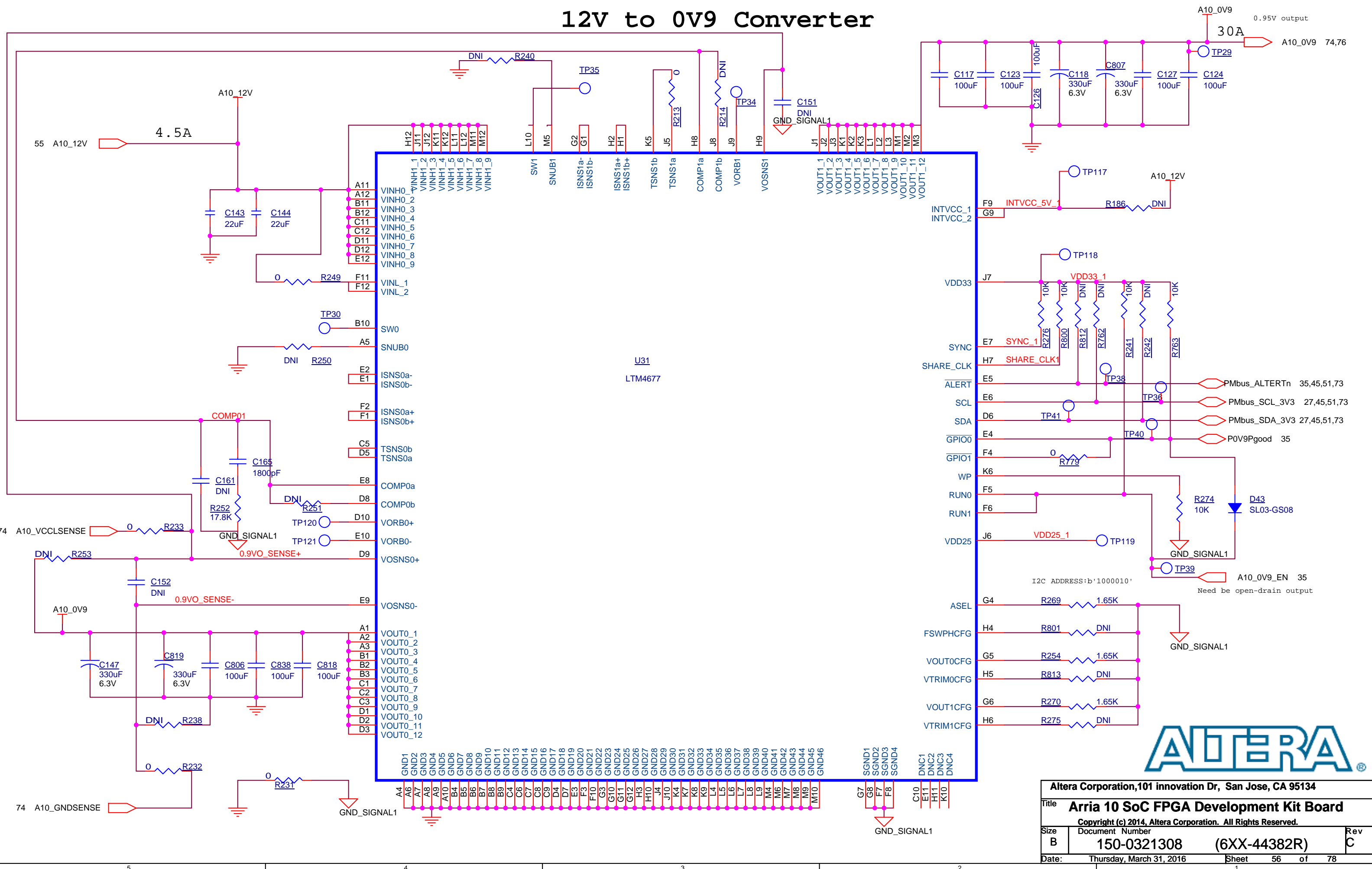Date: Thursday, March 31, 2016   Sheet   44   of   78

I2C MUX

IO_3V3

IO_3V3

I2C ADDRESS:b'1001100'

21 TEMPDIODE_P

C1562 2200pf

U46 MAX1619

6	ADD1	OVERTn 9
10	ADD0	ALERTn 11
3	DXP	SMBCLK 14
4	DXN	SMBDATA 12
15	STBYn	GND1 2
1	VCC	GND2 7
		GND3 8
5	NC1	
13	NC2	
16	NC3	

21 TEMPDIODE_N

IO_3V3

R399 200

C321 0.1uF

R380 R379
4.7K 4.7K

OVERTEMPn 35
TSENSE_ALERTn 35

J28
2X6

R605 0
R614 0

PMbus_ALTERTn 35,51,56,73

IO_3V3

U48 FXMA2102UMX

2	A0	B0 6
3	A1	B1 9
5	OE	
4	VCCA	VCCB 8
	GND	

IO_5V

LT_3V3 69

IO_2V5
IO_3V3

IO_3V3 69

IO_2V5

IO_2V5 36,68

IO_3V3

R376 R410
4.7K 4.7K

R387 R396 R374 R386
DNI DNI 4.7K 4.7K

IO_5V 50

20,35 A10_2L_SDA
20,35 A10_2L_SCL

R389 0
R397 0

LTSDA 71
LTSCL 71

Bus1_SDA
Bus1_SCL

R375 0
R385 0

CLOCK_I2C_SDA 39,40
CLOCK_I2C_SCL 39,40

R377 0
R402 0

EXTA_SDA 10,13,17
EXTA_SCL 10,13,17

R388 0
R398 0

EXTB_SDA 14,18
EXTB_SCL 14,18

IO_5V IO_3V3 IO_2V5

C2350 C338
0.1uF 0.1uF

C310 C331 C330 C314
0.1uF 0.1uF 0.1uF 0.1uF

C315 C309
0.1uF 0.1uF

IO_3V3

U43 FXMA2102UMX

2	A0	B0 7
3	A1	B1 6
5	OE	
1	VCCA	VCCB 8
4	GND	

IO_2V5

PMBus

PMbus_SDA_3V3 27,51,56,73
PMbus_SCL_3V3 27,51,56,73

J35

B1
2x16 LCD BOM I2C

LCD_SCL
LCD_SDA

I2C ADDRESS: 0x28

35 A10_PMBUSDIS_N

U44 FXMA2102UMX

2	A0	B0 7
3	A1	B1 6
5	OE	
1	VCCA	VCCB 8
4	GND	

IO_3V3

R395 R394
DNI DNI

R757 R776
4.7K 4.7K

LCD_HEADER

C873 0.04A

IO_5V

C873 0.1uF

IO_3V3

R401 4.7K

Note to assembler: Use this resistor to attach to LCD Header (follow assembly instructions).

IO_3V3 IO_3V3

U45 24LC32A

1	A0	VCC 8
2	A1	WP 7
3	A2	SCL 6
4	GND	SDA 5

C320 0.1uF

I2C ADDRESS:b'1010001'

I2C ADDRESS:b'1101000'

IO_3V3

C18 0.1uF

R29 0
R50 0

U5 DS1339C

3	VCC	VBACKUP 14
16	SDA	SQW/INT 2
1	SCL	NC5 4
15	GND	NC6 5
13	NC1	NC7 6
12	NC2	NC8 7
11	NC3	NC9 8
10	NC4	NC10 9

VBAT

R51 4.7K IO_3V3

BT1

Title **Arria 10 SoC FPGA Development Kit Board**

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A10 SOC DEV KIT PDN Diagram

Slew rate < 3V/ms

PCIE_12V

FMCA_12V

MAX V
Power Squencer

Slew rate < 3V/ms

FMCB_12V

12V_Power_Adapter
Input

Main_12V

A10_12V

Slew rate < 1V/ms

PO5V0
2A
EN2342QI

LTM4676
26A

10V
threshold

LTM4677
36A

PCIE_3V3

3V3

PD2.5V
3A
EN6337QI

PC1.8V
12A
EN63A0QI

HILO VDD
8A
EN6360QI

Slew rate < 1V/ms

LT_3V3

0V9

FMB_3V3

FMCA_3V3

HILO_VDD

FMB_3V3

FMA_3V3

IO_2V5

1V8

A10_main_
1V8

3.3V_IO
_Dicharge

IO_3V3

A10_Main_3V3

FMCB Vadj
8A
EN6360QI

FMCA Vadj
8A
EN6360QI

HILO VDDQ
8A
EN6360QI

PGHILO-HPS
VDD
8A
EN6360QI

Slew rate < 1V/ms

PF1V
12A
EN63A0QI

PN0.95V
3A
EN6337QI

PE0.95V
8A
EN6360QI

PLL1V8
Discharge

PMCBVADJ

FMCAVADJ

HILO_VDDQ

HILOHPS_VDD

IO_1V8

PLL_1V8

0V95

0V9/0V95

A10SOC

VCCIO3A | VCCIO3H | VCCIO3G | VCCIO3F | VCCIO3D | VCCIO3C | VCCIO3B | VCCIO2I | VCCIO2K | VCCIO2L | VCCIO3E | VCCIO2I | VCCIO2A | VCCPGM | VCCIOHPS | VCCBAT | VCCIOREF_HPS | VCCPLL_HPS | VCCA_PLL | VCCH_GXBL | VCCPT | VCCR_GXBL | VCCT_GXBL | VCCERAM | VCCL_HPS | VCC | VCCP

A10 SOC Power Sequence

Figure 1: Power-Up Sequence for Arria 10 Devices

Group	Rails
Group 1	VCC, VCCP, VCCR_GXB, VCCT_GXB, VCCRAM, VCCL_HPS
Group 2	VCCPT, VCCH_GXB, VCCA_FPLL, VCCPLL_HPS, VCCIOREF_HPS
Group 3	VCCPGM, VCCIO, VCCIO_HPS

Group 1 — 0.81 V
Group 2 — 1.62 V
Group 3 — 90% of Nominal Voltage

Device I/Os: Outputs tri-stated, inputs recommended not to be driven — Normal I/O Operation

1. If the VCC voltage level is different from
VCCT_GXB, VCCR_GXB, and orVCCRAM,
then ramp VCC first followed by VCCT_GXB,
VCCR_GXB, and VCCRAM (In any order) within group 1
2. All Power rails must ramp completely to
full rail voltage within the Tramp (0.2ms to 4ms)
3.VCCBAT (1.2-1.8V) can be powered up/down
at any time and is not shown in the power sequence
4.The Power down sequence is the reverse of
the power up sequence

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12V Power PMOS Switches

Input connector for
200 Watt AC/DC Adapter

J36
VOUT 1
VOUT 2
GND 3
GND 4
SGND 5
SGND 6
SGND 7
SGND 8
SGND 9
PD-40S

Adapter_DC_12V

16A

Q12 Si7635DP

R756 10

C872 1uF

R755 49.9K

D41 B530C

Q35 DMP3098L

1A

FMCB_12V 18

TP114
TP113

C64 330uF 25V
C67 330uF 25V
C63 330uF 25V
C65 330uF 25V

R773 49.9K
R810 49.9K
R785 49.9K

R786 10
C879 1uF
R774 10

Q36 DMP3098L

R196 10

3v/ms

R735 10

4 1
5 2
6 3
SW5 SW_SLIDE_DPDT

MAIN_GATE

J31
SENSE0 12V
SENSE1 12V
GND 12V
GND
GND
PCIe 2x4 ATX

12V ATX INPUT (12.5A)

R187 100K

3v/ms

R5353 1.00k
R775 100K

R5354 1.00k

C899 0.1uF

R803 10K

Q42 MMBT2222A-7-F

Q39 MMBT2222A-7-F

TP24
TP26

35 FMCB_EN

Q34 DMP3098L

S D
G

Q8 Si7635DP

10A

MAIN_12V 27,50,51,55,68

4A

PCIE_12V 10

R780 10
C882 1uF
R781 10

R686 10
C102 1uF
R171 10

TP90
TP84

3v/ms

R795 49.9K
R807 49.9K
R794 49.9K

Q38 DMP3098L

R5208 49.9K
R162 49.9K
R687 49.9K

Q9 DMP3098L

3v/ms

35 FMCA_EN

R796 100K

R172 100K

1A

FMCA_12V 17

TP103
TP104

R5374 1.00k

R5375 1.00k

C898 0.1uF

R808 10K

Q41 MMBT2222A-7-F

Q37 MMBT2222A-7-F

R5213 1.00k

R5214 1.00k

C777 0.1uF

R685 10K

Q30 MMBT2222A-7-F

Q31 MMBT2222A-7-F

35 PCIE_EN

ALTERA®

12V to 5V Converter

Rclx and Rfs chosen
for 12Vin/1.2Vout

VOUT = 5V

11,12,22,25,45,71 IO_5V

PVIN = 12V

Output capacitors chosen for
smallest footprint. For lower
Vout ripple option, use
two 47uF/1206/X5R capacitors.

Connect input and output caps
to GND plane through mulitple
vias. (See the Gerber files.)

A single through-hole via connects
these AGND pins to the GND plane.

C787 47nF
0402 X7R
TP92

C788
1uF
0402/X7R

PO_EN
TP93

5V0_Pgood 35

R707
68.1K
0402
R706
30.1K
0402

R709 0402
100k

680PF
C786

R692
4.7

U66
EN2342QI

R705
0

C785
56pf

R5030
80.6k
0402

R691
10K

R695
14.3K
0402

TP102

TP100

U66 pin labels (left side):
1 NC1
2 NC2
3 NC3
4 NC4
5 NC5
6 NC6
7 NC7
8 NC8
9 NC9
10 NC10
11 NC11
12 NC12
13 NC13
14 NC14

Top pins:
69 GND_PAD
68 NC68
67 NC67
66 NC66
65 NC65
64 NC64
63 NC(SW)63
62 NC(SW)62
61 NC(SW)61
60 AGND
59 NC59
58 FQADJ
57 RCLX
56 SS
55 EAOUT
54 VFB
53 AGND
52 AGND
51 AVIN
50 ENABLE
49 POK

Bottom pins:
15 NC15
16 VOUT
17 VOUT
18 VOUT
19 VOUT
20 VOUT
21 VOUT
22 VOUT
23 VOUT
24 VOUT
25 NC25
26 NC26
27 NC(SW)27
28 NC(SW)28
29 PGND
30 PGND
31 PGND
32 PGND
33 PGND
34 PGND

Right side pins:
48 S_OUT
47 S_IN
46 BGND
45 VDDB
44 BTMP
43 PG
42 AVINO
41 PVIN
40 PVIN
39 PVIN
38 PVIN
37 PVIN
36 PVIN
35 PVIN

C795 0402
0.22uF X7R

R5508
DNI

C796 22nF
0402
X7R

R710
4.75k

0402

C805
1uF
0402
X7R

R696
49.9K

R708
10K

R728
560
0402
or
0201

C834
C840

C835

Cin: 22u
1206
25V
X5R

F1 1A TP105
1.5A
MAIN_12V 49

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12V to 3V3 Converter

3V3

37,38,44,53,54,55,65,69,71

TP23 3V3

20A

C73 100uF C74 100uF C76 100uF C80 330uF 6.3V C69 100uF

DNI R509

TP62

R498 0

R499 DNI

TP130

C84 DNI

GND_SIGNAL2

MAIN_12V

6A TP25

49 MAIN_12V

C91 22uF C92 22uF

TP131 MAIN_12V

INTVCC_5V_2 R497 DNI

U24
LTM4676

Pin	Signal
H12	SW1
L10 M5	SNUB1
G2 G1	ISNS1a- ISNS1b-
H2 H1	ISNS1a+ ISNS1b+
K5 J5	TSNS1b TSNS1a
H8 J8	COMP1a COMP1b
J9	VORB1
H9	VOSNS1

VINH1_1 ... VINH1_9 (J11 J12 K11 K12 L11 L12 M11 M12)

A11 A12 VINH0_1 VINH0_2
B11 B12 VINH0_3 VINH0_4
C11 C12 VINH0_5 VINH0_6
D11 D12 VINH0_7 VINH0_8
E12 VINH0_9

F11 F12 0 R571 VINL_1 VINL_2

TP66 B10 SW0
DNI R157 A5 SNUB0
E2 E1 ISNS0a- ISNS0b-
F2 F1 ISNS0a+ ISNS0b+
C5 D5 TSNS0b TSNS0a
E8 COMP0a
D8 COMP0b DNI R156 R542 4.75K
D10 VORB0+ TP83
E10 VORB0- TP72

COMP02

C95 2200pF
C96 68pF

3V3_SENSE+ GND_SIGNAL2 D9 VOSNS0+

0 R120

C83 DNI

3V3_SENSE- E9 VOSNS0-

3V3

VOUT0_1 ... VOUT0_12 (A1 A2 A3 B1 B2 B3 C1 C2 C3 D1 D2 D3)

C82 330uF 6.3V C75 100uF C71 100uF C72 100uF

0 R121

VOUT1_1 ... VOUT1_12 (J1 J2 J3 K1 K2 K3 L1 L2 L3 M1 M2 M3)

INTVCC_1 F9
INTVCC_2 G9

VDD33 J7 TP61 VDD33_2
R148 R546 R545 R541 R549 R548 R547 (10K each)

SYNC E7 SYNC_2
SHARE_CLK H7 SHARE_CLK2
ALERT E5 PMbus_ALTERTn 35,45,56,73
SCL E6 PMbus_SCL_3V3 27,45,56,73
SDA D6 PMbus_SDA_3V3 27,45,56,73
GPIO0 E4 TP65
GPIO1 F4 0 R151 3V3_Pgood 35
WP K6
RUN0 F5
RUN1 F6 R160 10K

VDD25 J6 VDD25_2 TP73

GND_SIGNAL2

I2C ADDRESS:b'1001110'

ASEL G4 R132 22.6K
FSWPHCFG H4 R146 DNI
VOUT0CFG G5 R147 22.6K
VTRIM0CFG H5 R152 DNI
VOUT1CFG G6 R158 22.6K
VTRIM1CFG H6 R159 DNI

GND_SIGNAL2

GND1...GND46 (A4 A6 A7 A8 A9 A10 B4 B5 B6 B7 B8 B9 C4 C6 C7 C8 C9 C10 D4 D6 D7 E3 F3 G3 G10 G11 G12 H3 H10 J4 J10 K4 K7 K8 K9 K10 L4 L5 L6 L7 L8 L9 M4 M6 M7 M8 M9 M10)

SGND1 SGND2 SGND3 SGND4 (G7 G8 F7 F8)

DNC1 DNC2 DNC3 DNC4 (C10 E11 H11 K10)

0 R131

GND_SIGNAL2

GND_SIGNAL2

GND_SIGNAL2

Altera Corporation,101 innovation Dr, San Jose, CA 95134

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3V3 to 2V5 Converter

C826 15nF
0402

R737 100k

2V5_Pgood   35

PDEN

TP101

0
R736

U68
EN6337QI

Pin	Name		Name	Pin
1	NC(SW)7		NC25	25
2	NC(SW)6		NC24	24
3	NC3		NC23	23
4	NC4		NC22	22
5	VOUT		PVIN	21
6	VOUT		PVIN	20

Top pins (39–26): GND_PAD, NC(SW)1, NC(SW)2, NC(SW)3, NC(SW)4, NC(SW)5, AVIN, AGND, VFB, SS, RLLM, POK, ENABLE, LLM/SYNC

Bottom pins (7–19): VOUT, VOUT, VOUT, VOUT, VOUT, NC(SW), PGND, PGND, PGND, PGND, PGND, PGND, PVIN

R738 86.6k
0402

R744 200k
0402

C827 15pF
0402

DNI
R732

VIN = 2.4 - 6.6 VDC

3V3

2A

3V3   35,42,51

71   2V5I_P

R195   10K

C125 1uF

71   2V5I_N

R201   10K

2V5

R202

38,68,71   2V5

2A

2V5out

0.001

0
R745

TP96

C111   47uF
1206 X5R

C798   47uF

Connect the output cap to the GND plane through multiple vias

C797   22uF
1206 X5R

Connect the input cap to the GND plane through multiple vias. (see the Gerber files)

TP95

A single through-hole test point connects the AGND pin to the GND plane.

3.3V to 1.8V Converter

3V3

R713
5.49k

R712 10K
C789 15nF
0402

1V8_Pgood 35

TP97

R723 0402
100k

O
R714
DNI

R711

TP160

O
R715

U67
EN63A0QI

Pin	Signal		Pin	Signal
77	GND_PAD			
76	NC76			
75	NC75			
74	NC74			
73	NC73			
72	NC72			
71	NC(SW)71			
70	NC(SW)70			
69	EN_PB			
68	FQADJ			
67	NC(XREF)			
66	VSENSE			
65	SS			
64	EAOUT			
63	VFB			
62	IVS			
61	AGND			
60	AVIN			
59	ENABLE			
58	POK			
57	S_OUT			

1	NC1		56	S_IN
2	NC2		55	BGND
3	NC3		54	VDDB
4	NC4		53	NC53
5	NC5		52	NC52
6	NC6		51	PVIN
7	NC7		50	PVIN
8	NC8		49	PVIN
9	NC9		48	PVIN
10	NC10		47	PVIN
11	NC11		46	PVIN
12	NC12		45	PVIN
13	NC13		44	PVIN
14	NC14		43	PVIN
15	NC15		42	PVIN
16	NC16		41	PVIN
17	NC17		40	PVIN
18	NC18		39	PVIN

C799
0.22uF
0201
X5R

73 1V8SENSP
100 R758
0.22uF
C874

73 1V8SENSN
100 R759

TP109

1V8
R258
8A

1V8 23,38,39,55
0.00025

10A
1V8_OUT

3V3

3V3 35,42,51
5A

71 A10_1V8I_N
R271 10K

71 A10_1V8I_P
R272 10K

C172
1uF

O
R697

R698 160k
C780 27pF
0402   0402

R699
15k
0201

Connect the input and output caps
to the GND plane through mulitple vias.
(Please see the Gerber files.)

Pin	Signal
19	NC19
20	VOUT
21	VOUT
22	VOUT
23	VOUT
24	VOUT
25	VOUT
26	VOUT
27	VOUT
28	VOUT
29	NC29
30	NC(SW)30
31	NC(SW)31
32	PGND
33	PGND
34	PGND
35	PGND
36	PGND
37	PGND
38	PGND

C841 47uF
1206   X5R

C849 47uF
1206   X5R

C862 47uF
1206   X5R

C842 47uF
1206   X5R

C850 47uF
1206   X5R

A single through-hole via
connects the AGND
pin to the GND plane.

TP33

0.999V

R700
1V8DAC_P 73
DNI

R701
1V8DAC_N 73
DNI

R522
80.6k
0402

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MAIN_12V

Q10
Si7635DP

A10_12V

9A

49 MAIN_12V

3.5A

A10_12V 56,73

35,42,51 3V3

3V3

Q27

10A

A10_main_3V3 58,59,60,62,63,64,66,67

TP87

TP89

TP68

TP69

MAIN_12V

R608
100K

SiRA00DP

R681
49.9K

C774
1uF

R682
10

R53
25.5K

R597
1.00k

C599
0.01uF

R680
100K

Q28
MMBT2222A-7-F

R54
49.9

35 A10_EN

R694

Q29
MMBT2222A-7-F

10K

C779
0.1uF

R693
10K

R5491
1.00k

3V3

R55
10K

R52
10K

J58

1

2

CON2

TP88

J58 need be shorted if MAXV is not programmed

Typical 12V good threshold voltage is 10.62V.
Typcial 12V bad threshold voltage is 10.11V

U39

3 INA+   OUTA 1

4 INB-   OUTB 6

10V_Fail_n 35

10V_good 35

TP45

TP44

3V3

Q44

1V8

35,54 1V8

SiRA00DP

2 GND   VDD 5

TPS3700

C20
0.1uF

MAIN_12V

R277
100K

R273
100K

R278
1.00k

10A

A10_main_1V8 68

R607
10K

C894
0.01uF

Q40
MMBT2222A-7-F

TP42

TP37

Q46
MMBT2222A-7-F

C1560

C1561

100uF
6.3V

100uF
6.3V

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12V to 0V9 Converter

U31
LTM4677

0.95V output

A10_0V9   30A   A10_0V9 74,76

C117 100uF   C123 100uF   C126 100uF   C118 330uF 6.3V   C807 330uF   C127 100uF   C124 100uF

A10_12V

C143 22uF   C144 22uF

55 A10_12V   4.5A

I2C ADDRESS:b'1000010'

Need be open-drain output

PMbus_ALTERTn 35,45,51,73
PMbus_SCL_3V3 27,45,51,73
PMbus_SDA_3V3 27,45,51,73
P0V9Pgood 35
A10_0V9_EN 35

VDD33_1   10K 10K DNI DNI 10K DNI 10K
R276 R800 R812 R762 R241 R242 R763

SYNC_1
SHARE_CLK1

R274 10K   D43 SL03-GS08

R269 1.65K
R801 DNI
R254 1.65K
R813 DNI
R270 1.65K
R275 DNI

74 A10_VCCLSENSE   0   R233
DNI R253
COMP01
C165 1800pF
C161 DNI
R252 17.8K
R251 DNI
A10_0V9
C152 DNI
0.9VO_SENSE-
C147 330uF 6.3V   C819 330uF 6.3V   C806 100uF   C838 100uF   C818 100uF
DNI R238
0 R232
0 R231
74 A10_GNDSENSE

GND_SIGNAL1

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3.3V to 0.9V Converter

For a PWM application RLLM pin can float,
and LLM/SYNC has to be tied to GND.

P0V95Pgood   35

R657
100k   TP86

PPEN   49.9   A10_0V95_EN 35,73
              R669
              TP85

C760
15nF
0402

R655
1.00M

0402

Change Votlage to 0.9V for production FPGA

U64

EN6337QI

GND_PAD (39)
NC(SW)1 (38)
NC(SW)2 (37)
NC(SW)3 (36)
NC(SW)4 (35)
NC(SW)5 (34)
AVIN (33)
AGND (32)
VFB (31)
SS (30)
RLLM (29)
POK (28)
ENABLE (27)
LLM/SYNC (26)

1 NC(SW)7
2 NC(SW)6
3 NC3
4 NC4
5 VOUT
6 VOUT

NC25 25
NC24 24
NC23 23
NC22 22
PVIN 21
PVIN 20

DNI
R668

VIN = 2.4 - 6.6 VDC

VOUT (7)
VOUT (8)
VOUT (9)
VOUT (10)
VOUT (11)
NC(SW) (12)
PGND (13)
PGND (14)
PGND (15)
PGND (16)
PGND (17)
PGND (18)
PVIN (19)

C740
15pF
0402

R652
200k
0402

A10_Main_3V3

1A

A10_Main_3V3 55

0V95

TP74

R135

0V95out

0
R650

2A

74,76 0V95

C739 47uF
1206 X5R

C78   47uF

C767 22uF
1206 X5R

Connect the output
cap to the GND plane
through multiple vias

Connect the input
cap to the GND plane
through multiple vias.
(see the Gerber files)

TP81

A single through-hole test
point connects the AGND
pin to the GND plane.

71 A10_0V95I_N   R133   10K

C77
1uF

71 A10_0V95I_P   R134   10K

3.3V to 0.9V converter (HPS Core)

Optional EAOUT test point
is used for monitoring
purposes only.

A10_Main_3V3

R683 DNI
R688 10K

R684
0402
3.57k

C775 15nF
0402

TP77

R666 49.9
A10_0V95_EN 35,73

J30
1
2
CON2

R677
0 0

R656
0402
100k

HPS_Pgood 35

TP79

TP80

R665

1.78M

R140
10K

U65
EN6360QI

Pin	Name		Pin	Name
1	NC1		48	S_IN
2	NC2		47	BGND
3	NC3		46	VDDB
4	NC4		45	NC45
5	NC5		44	NC44
6	NC6		43	PVIN
7	NC7		42	PVIN
8	NC8		41	PVIN
9	NC9		40	PVIN
10	NC10		39	PVIN
11	NC11		38	PVIN
12	NC12		37	PVIN
13	NC13		36	PVIN
14	NC14		35	PVIN

Top pins: 69 GND_PAD, 68 NC68, 67 NC67, 66 NC66, 65 NC65, 64 NC64, 63 NC(SW)63, 62 NC(SW)62, 61 EN_PB, 60 FQADJ, 59 NC59, 58 VSENSE, 57 SS, 56 EAOUT, 55 VFB, 54 M/S, 53 AGND, 52 AVIN, 51 ENABLE, 50 POK, 49 S_OUT

Bottom pins: 15 NC15, 16 VOUT, 17 VOUT, 18 VOUT, 19 VOUT, 20 VOUT, 21 VOUT, 22 VOUT, 23 VOUT, 24 VOUT, 25 NC25, 26 NC(SW)26, 27 NC(SW)27, 28 PGND, 29 PGND, 30 PGND, 31 PGND, 32 PGND, 33 PGND, 34 PGND

73 A10_0V95SENSP

R141 100

C85 0.22uF

73 A10_0V95SENSN

R142 100

C757
0.22uF
0201
X5R

A single through-hole
via/test point connects
AGND pin to the GND plane.

TP78

HPS_0V95

74,76 HPS_0V95

R169
0.001

TP94
HPS_0V95out

3A

R703 0

R702
160k
0402

C781
22pF
0402

C772 47uF
1206 X5R

C773 47uF
1206 X5R

C758 22uF
1206 X5R

A10_Main_3V3

C759 22uF
1206 X5R

1.5A

A10_Main_3V3 55

VIN = 2.5 - 6.6VDC

71 A10_HPS0V95I_N

R170 10K

C99
1uF

71 A10_HPS0V95I_P

R161 10K

R689
15k
0201

0.896V

Connect the input and output caps
to the GND plane through mulitple vias.

R153

A10_0V95DAC_P 73

DNI

R667
324K
0402

R143

A10_0V95DAC_N 73

DNI

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3.3V to 1.0V Converter

A single through-hole via connects the AGND pin to the GND plane.

A10_Main_3V3

R505 3.57k
C453 15nF 0402
TP58
R511 10K
R504 0
R512 DNI
TP60
1V0_Pgood 35
R460 0402 100k
PFEN
49.9 R489 A10_1V0_EN 35,73
TP59
C418 0.22uF 0201 X5R
R488 10K

U56 EN63A0QI

Pin	Name		Pin	Name
1	NC1		56	S_IN
2	NC2		55	BGND
3	NC3		54	VDDB
4	NC4		53	NC53
5	NC5		52	NC52
6	NC6		51	PVIN
7	NC7		50	PVIN
8	NC8		49	PVIN
9	NC9		48	PVIN
10	NC10		47	PVIN
11	NC11		46	PVIN
12	NC12		45	PVIN
13	NC13		44	PVIN
14	NC14		43	PVIN
15	NC15		42	PVIN
16	NC16		41	PVIN
17	NC17		40	PVIN
18	NC18		39	PVIN

Top pins (77–57): GND_PAD, NC76, NC75, NC74, NC73, NC72, NC(SW)71, NC(SW)70, EN_PB, FQADJ, NC(XREF), VSENSE, SS, EAOUT, VFB, IVS, AGND, AVIN, ENABLE, POK, S_OUT

Bottom pins (19–38): NC19, VOUT, VOUT, VOUT, VOUT, VOUT, VOUT, VOUT, VOUT, VOUT, NC29, NC(SW)30, NC(SW)31, PGND, PGND, PGND, PGND, PGND, PGND, PGND

73 A10_1V0SENSP
100 R506
0.22uF C457
73 A10_1V0SENSN
100 R496

A10_1V0
1.03V output
74,77 A10_1V0
10A
R4252
TP19 A10_1V0OUT
0.00025
71 A10_1V0I_N
R109 10K
R510 0
C66 1uF
R110 10K
71 A10_1V0I_P

R502 160k 0402
C452 27pF 0402
R503 12k 0201

C454 47uF 1206 X5R
C456 47uF 1206 X5R
C455 47uF 1206 X5R

A10_Main_3V3
4A
A10_Main_3V3 55
C426 47uF 1206 X5R
C427 47uF 1206 X5R

Connect the input and output caps to the GND plane through mulitple vias. (Please see the Gerber files.)

Feedback network configured for 3.3Vin /1.0Vout

TP15

R494
0.999V
A10_1V0DAC_P 73
R495 226K 0402
619K
Update the value to 226K from 240K for 1.03V output
+-15% range
0 R493
A10_1V0DAC_N 73

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3.3V to HPS HILO VDD converter

A10_Main_3V3

TP54

PIEN   0   IO_EN   35,73
          R433

R451   10K
R450   DNI

C375 15nF
0402

R442
0402
5.49k

TP55

TP51
R5131
0402
HILOHPS_VDDPGood   35

100k

TP50

24   HILOHPS_1V2_SETn
R431
976K   1V2SET

24   HILOHPS_1V35_SETn
R426
390K   1V35SET

24   HILOHPS_1V5_SETn
R425
240K   1V5SET

0
R441

U52
EN6360QI

Pin	Signal	Pin	Signal
69	GND_PAD		
68	NC68		
67	NC67		
66	NC66		
65	NC65		
64	NC64		
63	NC(SW)63		
62	NC(SW)62		
61	EN_PB		
60	FQADJ		
59	NC59		
58	VSENSE		
57	SS		
56	EAOUT		
55	VFB		
54	M/S		
53	AGND		
52	AVIN		
51	ENABLE		
50	POK		
49	S_OUT		

1   NC1   S_IN   48
2   NC2   BGND   47   C351
3   NC3   VDDB   46   0.22uF
4   NC4   NC45   45   0201
5   NC5   NC44   44   X5R
6   NC6   PVIN   43
7   NC7   PVIN   42
8   NC8   PVIN   41
9   NC9   PVIN   40
10 NC10   PVIN   39
11 NC11   PVIN   38
12 NC12   PVIN   37
13 NC13   PVIN   36
14 NC14   PVIN   35

15 NC15
16 VOUT
17 VOUT
18 VOUT
19 VOUT
20 VOUT
21 VOUT
22 VOUT
23 VOUT
24 VOUT
25 NC25
26 NC(SW)26
27 NC(SW)27
28 PGND
29 PGND
30 PGND
31 PGND
32 PGND
33 PGND
34 PGND

A10_Main_3V3

1.5A

A10_Main_3V3   55

71   A10_HPSVDDI_P
R95   10K
C58
1uF
71   A10_HPSVDDI_N
R96   10K

HILOHPS_VDD
TP57

3A
R94
0.001

HILOHPS_VDDOUT

24,74,77   HILOHPS_VDD

73   HILOHPSSENSP
100   R91
0
R463

R462   C414
160k   22pF
0402   0402

0.22uF
C56

73   HILOHPSSENSN
100   R87

R456
15k
0201

C366   47uF
1206   X5R

C365   47uF
1206   X5R

C352   22uF
1206   X5R

C353   22uF
1206   X5R

VIN = 2.5 - 6.6VDC

Connect the input and output caps
to the GND plane through mulitple vias.

1.102V

R89
HILOHPSDAC_P   73
DNI

R436
191K
0402

R88
HILOHPSDAC_N   73
DNI

TP56

A single through-hole
via/test point connects
AGND pin to the GND plane.

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Arria 10 SoC FPGA Development Kit Board

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3.3V to HILO VDD converter

34 HILO_1V2_SETn R626 976K 1V2SET

A10_Main_3V3

R635 10K
R636 DNI

C709 15nF 0402

TP70

PGEN R639 O IO_EN 35,73

34 HILO_1V25_SETn R627 649K 1V25SET

R637 O

R648 0402 5.49k

TP75

34 HILO_1V30_SETn R5160 487K 1V3SET

TP71

R5169 0402 100k

HILO_VDDPGood 35

34 HILO_1V35_SETn R624 390K 1V35SET

U63
EN6360QI

Pin	Signal		Pin	Signal
69	GND_PAD			
68	NC68			
67	NC67			
66	NC66			
65	NC65			
64	NC64			
63	NC(SW)63			
62	NC(SW)62			
61	EN_PB			
60	FQADJ			
59	NC59			
58	VSENSE			
57	SS			
56	EAOUT			
55	VFB			
54	M/S			
53	AGND			
52	AVIN			
51	ENABLE			
50	POK			
49	S_OUT			

34 HILO_1V5_SETn R623 240K 1V5SET

34 HILO_1V8_SETn R622 137K 1V8SET

1	NC1
2	NC2
3	NC3
4	NC4
5	NC5
6	NC6
7	NC7
8	NC8
9	NC9
10	NC10
11	NC11
12	NC12
13	NC13
14	NC14

48	S_IN
47	BGND
46	VDDB
45	NC45
44	NC44
43	PVIN
42	PVIN
41	PVIN
40	PVIN
39	PVIN
38	PVIN
37	PVIN
36	PVIN
35	PVIN

C732 0.22uF 0201 X5R

71A10_HLVDDI_P R144 10K

C86 1uF R145 10K

HILO_VDD

4A

34 HILO_VDD R155

TP82 HILO_VDDOUT

15	NC15
16	VOUT
17	VOUT
18	VOUT
19	VOUT
20	VOUT
21	VOUT
22	VOUT
23	VOUT
24	VOUT
25	NC25
26	NC(SW)26
27	NC(SW)27
28	PGND
29	PGND
30	PGND
31	PGND
32	PGND
33	PGND
34	PGND

73 HILOVDDSENSP 0.001 R163 100

0.22uF C97

73 HILOVDDSENSN 100 R154

R649 O

C725 22pF 0402

R647 160k 0402

R634 15k 0201

C765 47uF 1206 X5R

C755 47uF 1206 X5R

C766 22uF 1206 X5R

C756 22uF 1206 X5R

A10_Main_3V3

1.7A

A10_Main_3V3 55

Connect the input and output caps
to the GND plane through mulitple vias.

1.102V R130 HILOVDDDAC_P 73 DNI

R638 191K 0402

TP76

A single through-hole
via/test point connects
AGND pin to the GND plane.

R129 HILOVDDDAC_N 73 DNI

71A10_HLVDDI_N

Title **Arria 10 SoC FPGA Development Kit Board**

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3.3V to HILO VDDQ converter

34 HILOQ_1V2_SETn
R527
976K 1V2SET

34 HILOQ_1V25_SETn
R526
649K 1V25SET

34 HILOQ_1V30_SETn
R529
487K 1V3SET

34 HILOQ_1V35_SETn
R528
390K 1V35SET

34 HILOQ_1V5_SETn
R530
240K 1V5SET

34 HILOQ_1V8_SETn
R531
137K 1V8SET

A10_Main_3V3
R553 10K
R554 DNI
R556 0

R555 0402 5.49k
C492 0402 15nF
TP18
TP17
TP16

R558 0 IO_EN 35,73
R559 0402 100k HILO_VDDQPGood 35
TP20

U59
EN6360QI

Pin	Name
1	NC1
2	NC2
3	NC3
4	NC4
5	NC5
6	NC6
7	NC7
8	NC8
9	NC9
10	NC10
11	NC11
12	NC12
13	NC13
14	NC14

Top pins: 69 GND_PAD, 68 NC68, 67 NC67, 66 NC66, 65 NC65, 64 NC64, 63 NC(SW)63, 62 NC(SW)62, 61 EN_PB, 60 FQADJ, 59 NC59, 58 VSENSE, 57 SS, 56 EAOUT, 55 VFB, 54 M/S, 53 AGND, 52 AVIN, 51 ENABLE, 50 POK, 49 S_OUT

Right pins:
48 S_IN
47 BGND
46 VDDB
45 NC45
44 NC44
43 PVIN
42 PVIN
41 PVIN
40 PVIN
39 PVIN
38 PVIN
37 PVIN
36 PVIN
35 PVIN

C495 0.22uF 0201 X5R

Bottom pins: 15 NC15, 16 VOUT, 17 VOUT, 18 VOUT, 19 VOUT, 20 VOUT, 21 VOUT, 22 VOUT, 23 VOUT, 24 VOUT, 25 NC25, 26 NC(SW)26, 27 NC(SW)27, 28 PGND, 29 PGND, 30 PGND, 31 PGND, 32 PGND, 33 PGND, 34 PGND

71A10_HLVDDQI_P
R111 10K
C68 1uF
71A10_HLVDDQI_N
R112 10K

HILO_VDDQ
34,74,77 HILO_VDDQ
3A
R114
HILO_VDDQOUT
TP21

73 HILOVDDQSENSP
R119 0.001 100
R568 0
C70 0.22uF

73 HILOVDDQSENSN
R118 100

R551 160k 0402
C494 22pF 0402
R552 15k 0201

C529 1206 47uF X5R
C564 1206 47uF X5R

C530 1206 22uF X5R
C565 1206 22uF X5R

A10_Main_3V3
VIN = 2.5 - 6.6VDC
1.5A
A10_Main_3V3 55

Connect the input and output caps
to the GND plane through mulitple vias.

1.102V
R108
DNI
HILOVDDQDAC_P 73

A single through-hole
via/test point connects
AGND pin to the GND plane.
TP22

R557 191K 0402
R107
DNI
HILOVDDQDAC_N 73

FMC 3.3V PMOS Switches

35,42,51 3V3

3V3

Q4
SiSS23DN
3A FMCB_3V3 72

R14 10
C186 1uF
R19 10
R25 100K

Q16
DMG2305UX

35 FMCB_EN

TP8
TP6

3V3

Q2
SiSS23DN
3A FMCA_3V3 72

R6 10
C177 1uF
R4 10
R5 100K

Q13
DMG2305UX

35 FMCA_EN

TP4
TP3

3V3

Q3
SiSS23DN
0.02A FMCB_aux3V3 18

R18 10
C187 1uF
R23 10
R24 100K

Q17
DMG2305UX

35 FMCB_AUXEN

TP10
TP5

3V3

Q1
SiSS23DN
0.02A FMCA_aux3V3 17

R3 10
C178 1uF
R1 10
R2 100K

Q14
DMG2305UX

35 FMCA_AUXEN

TP2
TP1

3.3V to FMC A VADJ converter

J42

1	1	2	2
3	3	4	4
5	5	6	6
7	7	8	8
9	9	10	10

2X5_100mil

R788 1V2SET 976K
R789 1V25SET 649K
R799 1V35SET 390K
R805 1V5SET 240K
R811 1V8SET 137K

A10_main_3V3
R761 10K
R778 DNI
R777 0402 5.49k
R787 0

C880 15nF 0402
TP112
TP116

PJEN
R798 0
TP111
FMCA_EN 35
R804 0402 100k
FMCAVADJPGood 35
TP115

U70
EN6360QI

Pin labels left side:
1 NC1
2 NC2
3 NC3
4 NC4
5 NC5
6 NC6
7 NC7
8 NC8
9 NC9
10 NC10
11 NC11
12 NC12
13 NC13
14 NC14

Top pins:
69 GND_PAD
68 NC68
67 NC67
66 NC66
65 NC65
64 NC64
63 NC(SW)63
62 NC(SW)62
61 EN_PB
60 FQADJ
59 NC59
58 VSENSE
57 SS
56 EAOUT
55 VFB
54 M/S
53 AGND
52 AVIN
51 ENABLE
50 POK
49 S_OUT

PJEA

Right pins:
48 S_IN
47 BGND
46 VDDB
45 NC45
44 NC44
43 PVIN
42 PVIN
41 PVIN
40 PVIN
39 PVIN
38 PVIN
37 PVIN
36 PVIN
35 PVIN

C900 0.22uF 0201 X5R

Bottom pins:
15 NC15
16 VOUT
17 VOUT
18 VOUT
19 VOUT
20 VOUT
21 VOUT
22 VOUT
23 VOUT
24 VOUT
25 NC25
26 NC(SW)26
27 NC(SW)27
28 PGND
29 PGND
30 PGND
31 PGND
32 PGND
33 PGND
34 PGND

71FMAVADJI_P
R243 10K
C164 1uF
71FMAVADJI_N
R234 10K

TP110

FMCAVADJ
6A
17,36,74,77 FMCAVADJ
R244 0.001
FMCAVADJOUT
R751 0

73 FMASENSP
100 R256
0.22uF C167
73 FMASENSN
100 R257

R752 160k 0402
C863 22pF 0402
R760 15k 0201

C884 47uF 1206 X5R
C883 47uF 1206 X5R

A10_main_3V3
3A
A10_main_3V3 55

C896 22uF 1206 X5R
C895 22uF 1206 X5R

VIN = 2.5 - 6.6VDC

Connect the input and output caps
to the GND plane through mulitple vias.

1.102V
R260 DNI
FMADAC_P 73
R797 191K 0402
R261 DNI
FMADAC_N 73

TP108
A single through-hole
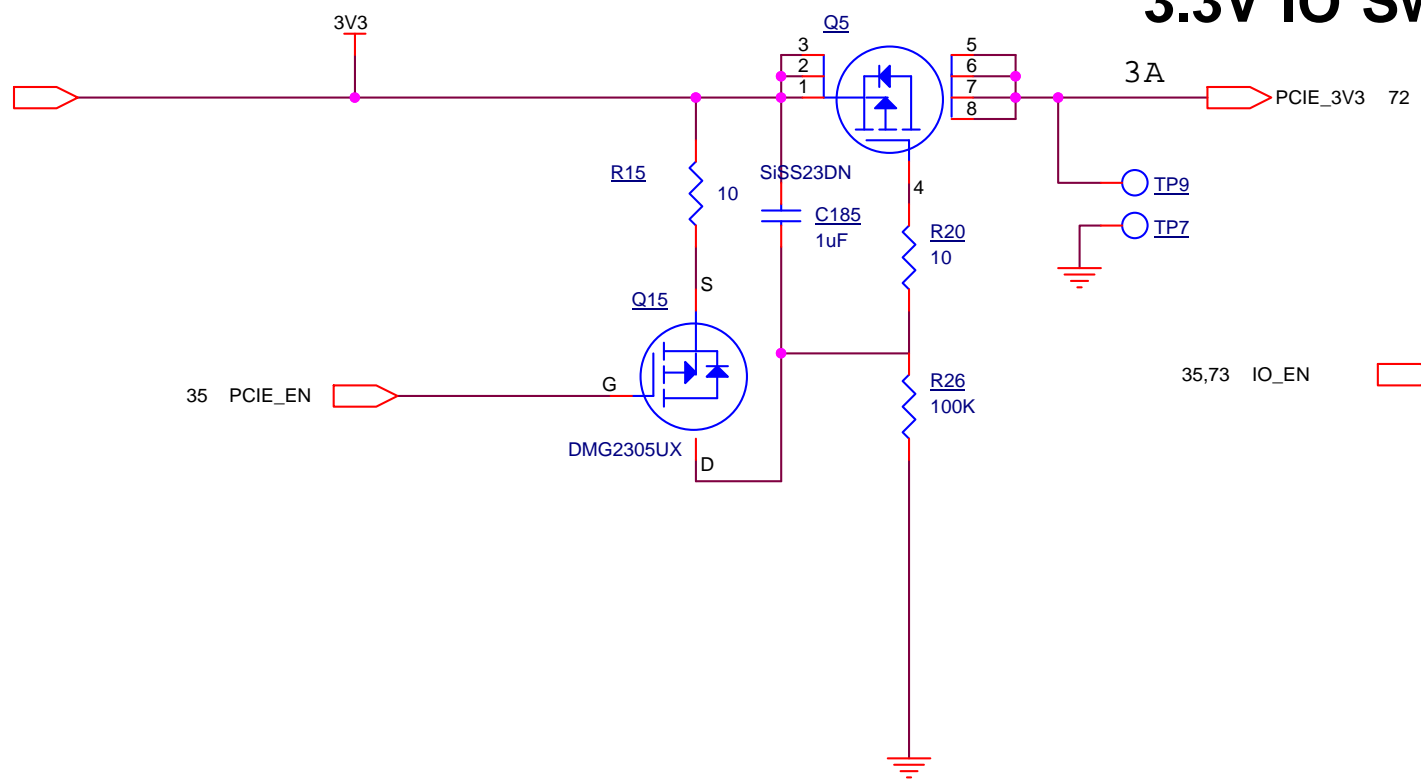via/test point connects
AGND pin to the GND plane.

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3.3V to FMC B VADJ converter

R716 1V2SET
976K
R717 1V25SET
649K
R718 1V35SET
390K
R719 1V5SET
240K
R720 1V8SET
137K

J32
2X5_100mil

A10_main_3V3
R729 10K
R730 DNI
R733 0402 5.49k
TP31

PKEN
R746 0 → FMCB_EN 35
TP107

C817 15nF 0402

O R740

FMCBVADJPGood 35
R747 0402 100k
TP106

U69
EN6360QI

Pin	Name
69	GND_PAD
68	NC68
67	NC67
66	NC66
65	NC65
64	NC64
63	NC(SW)63
62	NC(SW)62
61	EN_PB
60	FQADJ
59	NC59
58	VSENSE
57	SS
56	EAOUT
55	VFB
54	M/S
53	AGND
52	AVIN
51	ENABLE
50	POK
49	S_OUT

1 NC1
2 NC2
3 NC3
4 NC4
5 NC5
6 NC6
7 NC7
8 NC8
9 NC9
10 NC10
11 NC11
12 NC12
13 NC13
14 NC14

S_IN 48
BGND 47
VDDB 46
NC45 45
NC44 44
PVIN 43
PVIN 42
PVIN 41
PVIN 40
PVIN 39
PVIN 38
PVIN 37
PVIN 36
PVIN 35

C845 0.22uF 0201 X5R

15 NC15
16 VOUT
17 VOUT
18 VOUT
19 VOUT
20 VOUT
21 VOUT
22 VOUT
23 VOUT
24 VOUT
25 NC25
26 NC(SW)26
27 NC(SW)27
28 PGND
29 PGND
30 PGND
31 PGND
32 PGND
33 PGND
34 PGND

71FMBVADJI_P
R193 10K
C119 1uF
R192 10K
71FMBVADJI_N

TP99

FMCBVADJ

18,36,74,77 FMCBVADJ
4A
R194 0.001

O R724

FMCBVADJOUT

73 FMBSENSP
R200 100
0.22uF
C128
73 FMBSENSN
R206 100

R726 160k 0402
C800 22pF 0402

R725 15k

1.102V
R739 191K 0402

A single through-hole
via/test point connects
AGND pin to the GND plane.

TP98

C829 47uF 1206 X5R
C828 47uF 1206 X5R

C844 22uF 1206 X5R
C843 22uF 1206 X5R

A10_main_3V3
2A
VIN = 2.5 - 6.6VDC
A10_main_3V3 55

Connect the input and output caps
to the GND plane through mulitple vias.

R205
FMBDAC_P 73
DNI

R215
FMBDAC_N 73
DNI

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2.5V and 1.8V IO Switches

2V5

1A

35,53 2V5

Q20
SiSS23DN

1A

IO_2V5   11,12,16,22,24,27,34,39,41,45

TP46

R381   10

C306
1uF

R371
10

TP47

Q19

S

35,73 IO_EN

G

R362
49.9K

DMG2305UX   D

A10_main_1V8

Q24
SiRA00DP

5A

5A

IO_1V8

MAIN_12V

15,20,21,22,23,25,27,39,40,42,74,77

TP53

R455
100K

10K
R454

TP52

R181
1.00k

C105
0.01uF

A10_main_1V8

Q7
SiRA00DP

PLL_1V8

R449
10K

B   C

Q25
MMBT2222A-7-F

E

4A

4A

PLL_1V8   70,74,77

B   C   Q26
MMBT2222A-7-F

55A10_main_1V8

TP27

E

MAIN_12V

4

R5315
10K

TP28

49   MAIN_12V

R179
100K

10K
R5510

35,73 A10_1V8_EN

R184
1.00k

R185
10K

B   C   Q33
MMBT2222A-7-F

B   C   Q11
MMBT2222A-7-F

C790
0.01uF

E

E

R5509
10K

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3.3V IO Switches

3V3

Q5
SiSS23DN
3 A PCIE_3V3 72
35,42,51 3V3

R15 10
C185 1uF
R20 10
TP9
TP7

Q15
DMG2305UX
35 PCIE_EN
R26 100K

3V3
Q23
SiSS23DN
3 A IO_3V3
13,14,15,20,22,23,24,25,26,27,33,34,39,41,42,45,70

3 A
3V3

R403 10
C327 1uF
R400 10
TP49
TP48

Q22
DMG2305UX
35,73 IO_EN
R393 49.9K

Q6
SiSS23DN
0.375A PCIE_aux3V3 10
3V3

R46 10
C216 1uF
R31 10
TP13
TP14

Q18
DMG2305UX
35 PCIE_auxEN
R30 100K

LT_3V3
3V3
R317
0.3A LT_3V3 45,71,73
0.01
TP11
TP12

3.3V and 1.8V Discharge Load

69   IO_3V3

68   PLL_1V8

RJK0301DPB

35   IO3V3_discharge

R391
10

Q21
drain-tab

DS3v3Current

R392
10K

R363
0.5

RJK0301DPB

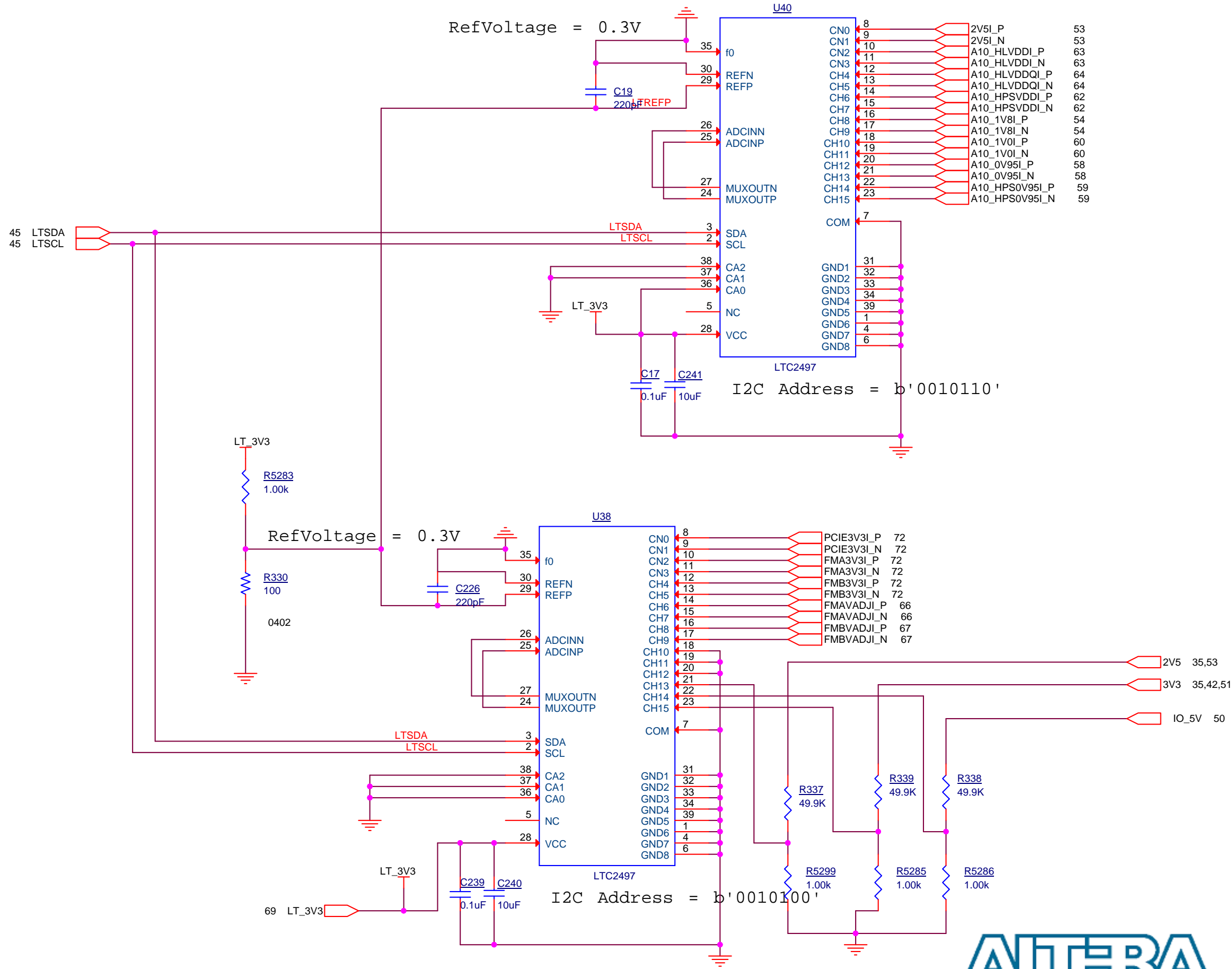35   PLL1V8_discharge

R727
10

Q32
drain-tab

DS1V8Current

R731
10K

R734
0.5
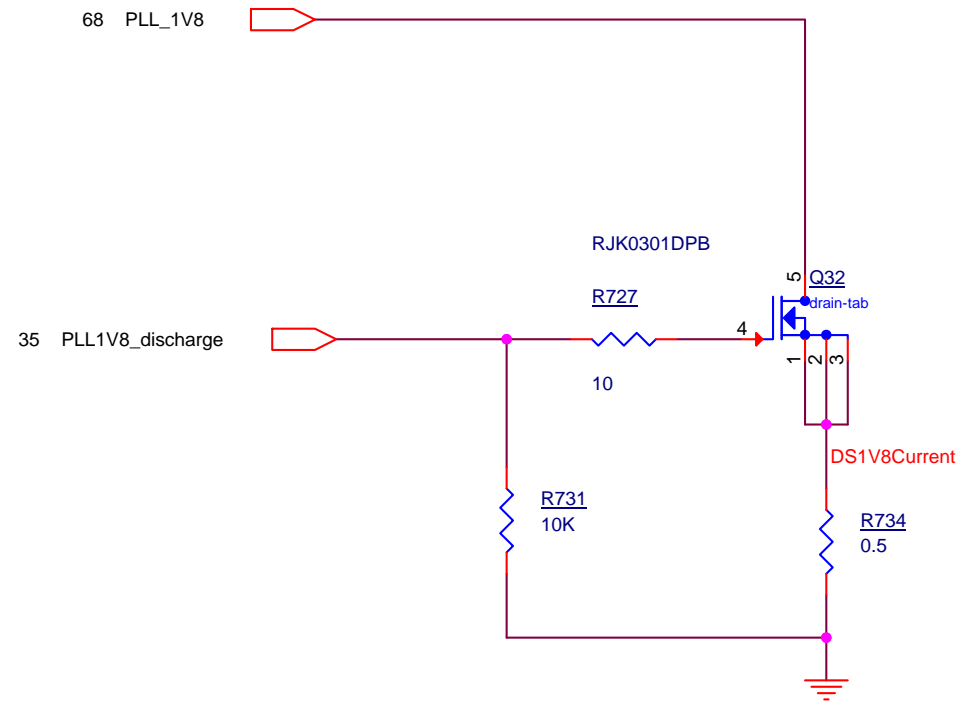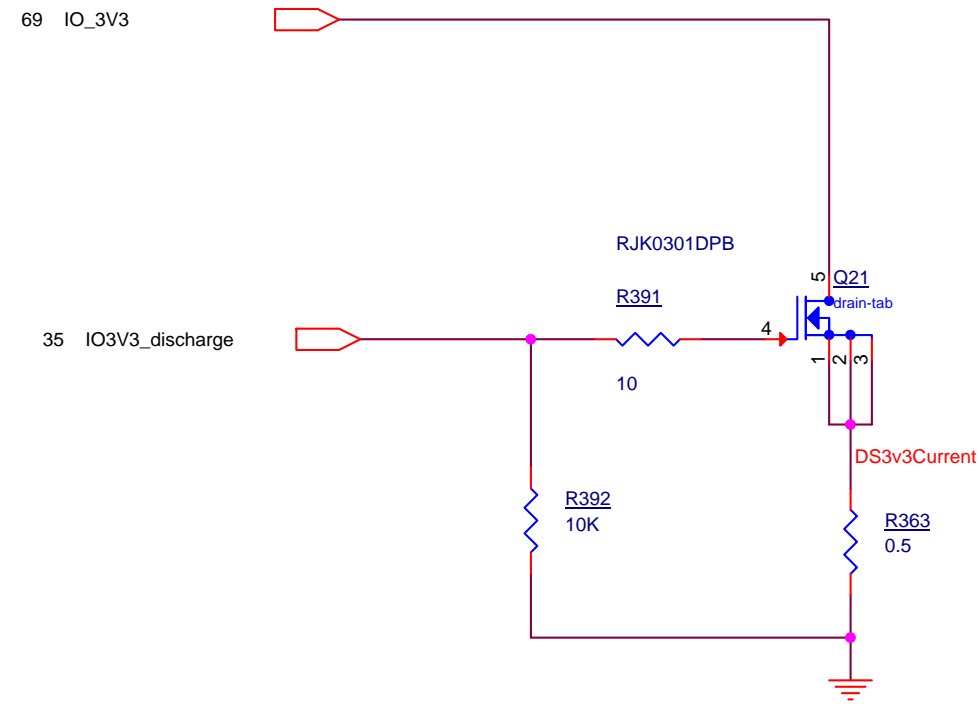
50us Discharge time

Altera Corporation,101 innovation Dr, San Jose, CA 95134

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I2C Current ADC (A)

RefVoltage = 0.3V

U40 — LTC2497

Pin	Signal		Signal	Pin
35	f0	CN0	8	2V5I_P	53
		CN1	9	2V5I_N	53
30	REFN	CN2	10	A10_HLVDDI_P	63
29	REFP	CN3	11	A10_HLVDDI_N	63
		CH4	12	A10_HLVDDQI_P	64
		CH5	13	A10_HLVDDQI_N	64
		CH6	14	A10_HPSVDDI_P	62
		CH7	15	A10_HPSVDDI_N	62
		CH8	16	A10_1V8I_P	54
26	ADCINN	CH9	17	A10_1V8I_N	54
25	ADCINP	CH10	18	A10_1V0I_P	60
		CH11	19	A10_1V0I_N	60
		CH12	20	A10_0V95I_P	58
27	MUXOUTN	CH13	21	A10_0V95I_N	58
24	MUXOUTP	CH14	22	A10_HPS0V95I_P	59
		CH15	23	A10_HPS0V95I_N	59

C19 220pF REFP

		COM	7
3	SDA	LTSDA
2	SCL	LTSCL
38	CA2	GND1	31
37	CA1	GND2	32
36	CA0	GND3	33
		GND4	34
5	NC	GND5	39
		GND6	1
28	VCC	GND7	4
		GND8	6

LT_3V3

C17 0.1uF   C241 10uF

I2C Address = b'0010110'

RefVoltage = 0.3V

R5283 1.00k
R330 100   0402

U38 — LTC2497

Pin	Signal		Signal	Pin
35	f0	CN0	8	PCIE3V3I_P	72
		CN1	9	PCIE3V3I_N	72
30	REFN	CN2	10	FMA3V3I_P	72
29	REFP	CN3	11	FMA3V3I_N	72
		CH4	12	FMB3V3I_P	72
		CH5	13	FMB3V3I_N	72
		CH6	14	FMAVADJI_P	66
		CH7	15	FMAVADJI_N	66
		CH8	16	FMBVADJI_P	67
26	ADCINN	CH9	17	FMBVADJI_N	67
25	ADCINP	CH10	18
		CH11	19
		CH12	20
27	MUXOUTN	CH13	21
24	MUXOUTP	CH14	22
		CH15	23

C226 220pF

2V5   35,53
3V3   35,42,51
IO_5V   50

		COM	7
3	SDA	LTSDA
2	SCL	LTSCL
38	CA2	GND1	31
37	CA1	GND2	32
36	CA0	GND3	33
		GND4	34
5	NC	GND5	39
		GND6	1
28	VCC	GND7	4
		GND8	6

R337 49.9K   R339 49.9K   R338 49.9K
R5299 1.00k   R5285 1.00k   R5286 1.00k

LT_3V3

C239 0.1uF   C240 10uF

I2C Address = b'0010100'

69 LT_3V3

45 LTSDA
45 LTSCL

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User DC card 3.3V Current Sensors

71 PCIE3V3I_P
71 PCIE3V3I_N

R32 10K

PCIE_3V3 69

C11
1uF

R316
0.01

R47 10K

PCIE_DC_3V3 10

71 FMA3V3I_P
71 FMA3V3I_N

R742 10K

FMCA_3V3 65

C833
1uF

R743
0.01

R741 10K

FMCA_DC_3V3 17

71 FMB3V3I_P
71 FMB3V3I_N

R523 10K

FMCB_3V3 65

C479
1uF

R524
0.01

R507 10K

FMCB_DC_3V3 18,36

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I2C Power ADC, DAC Controller

U35

LTC2977

Pin	Signal
14	VIN_SNS
12	VIN_EN

A10_12V

55 A10_12V

36	VSENSEP0
37	VSENSEM0
42	VSENSEP1
43	VSENSEM1
46	VSENSEP2
47	VSENSEM2
48	VSENSEP3
49	VSENSEM3
52	VSENSEP4
53	VSENSEM4
62	VSENSEP5
63	VSENSEM5
64	VSENSEP6
1	VSENSEM6
2	VSENSEP7
3	VSENSEM7

59 A10_0V95SENSP
59 A10_0V95SENSN
60 A10_1V0SENSP
60 A10_1V0SENSN
54 1V8SENSP
54 1V8SENSN
66 FMASENSP
66 FMASENSN
67 FMBSENSP
67 FMBSENSN
62 HILOHPSSENSP
62 HILOHPSSENSN
63 HILOVDDSENSP
63 HILOVDDSENSN
64 HILOVDDQSENSP
64 HILOVDDQSENSN

34 REFP
35 REFM
13 NC

C194
0.1uF

39	VDACP0
38	VDACM0
40	VDACP1
41	VDACM1
44	VDACP2
45	VDACM2
50	VDACP3
51	VDACM3
55	VDACP4
54	VDACM4
56	VDACP5
57	VDACM5
59	VDACP6
58	VDACM6
60	VDACP7
61	VDACM7

A10_0V95DAC_P 59
A10_0V95DAC_N 59
A10_1V0DAC_P 60
A10_1V0DAC_N 60
1V8DAC_P 54
1V8DAC_N 54
FMADAC_P 66
FMADAC_N 66
FMBDAC_P 67
FMBDAC_N 67
HILOHPSDAC_P 62
HILOHPSDAC_N 62
HILOVDDDAC_P 63
HILOVDDDAC_N 63
HILOVDDQDAC_P 64
HILOVDDQDAC_N 64

27,45,51,56 PMbus_SCL_3V3
27,45,51,56 PMbus_SDA_3V3

28	SCL
27	SDA
32	ASEL0
33	ASEL1
30	CONTROL0
31	CONTROL1
22	WDI/RESET

LT_3V3

R300 10K
R301 10K
R290 10K

4	VOUT_EN0
5	VOUT_EN1
6	VOUT_EN2
7	VOUT_EN3
8	VOUT_EN4
9	VOUT_EN5
10	VOUT_EN6
11	VOUT_EN7

R288 DNI
R287 DNI
R286 DNI
R285 DNI
R284 10K
R283 10K
R282 10K
R281 10K

R9 10K
R10 10K
R12 10K
R13 10K

A10_0V95_EN 58,59
A10_1V0_EN 60
A10_1V8_EN 68
IO_EN 62,63,64,68,69

R291 10K
R295 10K
R296 10K
R299 10K

23	FAULTB00
24	FAULTB01
25	FAULTB10
26	FAULTB11

R280 5.49K

| 21 | SHARE_CLK |

29	ALERTB
20	PWRGD
15	VPWR
18	VDD25

R279 10K

LTPWRGD 35
PMbus_ALERTn 35,45,51,56

35 LTCNTRL0
35 LTCNTRL1
35 LTWDI_RESETN
35 LTFAUL0

| 19 | WP |
| 65 | E-PAD |

LT_3V3

| 16 | VDD33_OUT |
| 17 | VDD33_IN |

LT_3V3 69

I2C Address = b'1011100'

C2
0.1uF

C3
0.1uF

C1
0.1uF

Arria 10 Power Inputs

U23Y — A10SOC_1517

PLL_1V8

77 A10_VCCAPLL
68 PLL_1V8

A10VCCPLLHPS 77
VCCIOREF_HPS 77
VCCIO_HPS 77
HPS_0V95 59
A10_VCCLSENSE 56
A10_GNDSENSE 56

VCCBAT — AE18
VCCA_PLL — W19
VCCA_PLL — W18

VCCP — T24, T23, T20, T19, T17, T15, T14, AD25, AD24, AD16, AD15, AD14

VCCPLL_HPS — N18
VCCIOREF_HPS — N16, M16
VCCIO_HPS — N17, P16, P18, R18
VCCLSENSE — AA19
GNDSENSE — AA18

PLL_1V8 1.8A

VCCH_GXBL — AD27, AH27, AM27, D27, H27, M27, T27, Y27

60 A10_1V0

VCCT_GXBL1J — D29, D28
VCCT_GXBL1I — H29, H28
VCCT_GXBL1H — M29, M28
VCCT_GXBL1G — T29, T28
VCCT_GXBL1F — Y29, Y28
VCCT_GXBL1E — AD29, AD28
VCCT_GXBL1D — AH29, AH28
VCCT_GXBL1C — AM29, AM28

VCCR_GXBL1C — AP28, AP29
VCCR_GXBL1D — AK28, AK29
VCCR_GXBL1E — AF28, AF29
VCCR_GXBL1F — AB28, AB29
VCCR_GXBL1G — V28, V29
VCCR_GXBL1H — P28, P29
VCCR_GXBL1I — K28, K29
VCCR_GXBL1J — F28, F29

VCCIO2A — AK19, AM18, AP17
VCCIO2I — AL21, AP22, AT21
VCCIO2J — AK24, AN25, AR24
VCCIO2K — E24, H25, K24
VCCIO2L — H20, J22, K19
VCCIO3A — AK14, AL11, AM13
VCCIO3B — AK9, AL6, AM8
VCCIO3C — AD7, AG8, AH5
VCCIO3D — AA6, AC5, Y4
VCCIO3E — R4, T6, V5
VCCIO3F — K4, L6, M8
VCCIO3G — G8, K9, L11
VCCIO3H — G13, J12, K14

IO_1V8 36,37,68
HILOHPS_VDD 62
IO_1V8
FMCBVADJ 67
HILO_VDDQ 64
IO_1V8
FMCAVADJ 66

VCCPT — U22, U21, U20, U17, T16, U15, U16, AC21, AC19, AC17, AC16, AC14, AB14
VCCPGM — AF19, AF18
VCCERAM — Y12, Y13, Y18, Y21, Y22, Y23
VREFP_ADC — D16
VREFN_ADC — D15
VREFB3HN0 — M15
VREFB3FN0 — P13
VREFB3EN0 — T10
VREFB3DN0 — W11
VREFB3CN0 — Y11
VREFB3BN0 — AD11
VREFB3AN0 — AF13
VREFB2LN0 — AH16
VREFB2KN0 — P22
VREFB2JN0 — P24
VREFB2IN0 — AF23
VREFB2AN0 — AE23, AG19

A10SOC_1517

PLL_1V8 2A
58 0V95
3A
IO_1V8

U23Q — A10SOC_1517

A10_0V9 56

VCC — AF21, AF22, P21, P23, R12, R13, R14, R15, R16, R17, R20, R21, R22, R23, R25, T12, T13, T18, T22, T25, U12, U14, U19, U24, U25, U26, V12, V13, V14, V16, V17, V18, V19, V21, V22, V23, V24, W13, W14, W20, W21, W23, W24, W25, Y14, Y16

VCC — AA12, AA13, AA14, AA15, AA16, AA20, AA22, AA23, AA24, AA25, AB12, AB15, AB16, AB17, AB19, AB20, AB22, AB24, AB25, AC12, AC13, AC18, AC23, AC24, AC26, AD13, AD17, AD18, AD19, AD21, AD22, AD23, AE12, AE13, AE14, AE15, AE16, AE17, AE21, AE22, AE25, Y17, Y20, Y25

Capacitors / Resistors

0.1uF C719 C524 C554 C523

IO_1V8   HILOHPS_VDD   IO_1V8   FMCBVADJ

R519 240
R521 240
R520 240
R645 240
R646 DNI
R518 240
HILO_VDDQ

VREFB2A
VREFB2I
VREFB2J
VREFB2K
VREFB2L
VREFB3A
VREFB3B   R580 240
VREFB3C   R591 240
VREFB3D   R599 240

IO_1V8   FMCAVADJ

R672 240
R631 240
R619 240
R618 240
R600 240
R592 240
R581 240
R535 240
R644 240
R643 240
R537 240
R538 DNI
R536 DNI

VREFB3E   R616 240
VREFB3F   R617 240
VREFB3G   R630 240
VREFB3H   R678 240

C720 C522 C521 C567 C566 C644 C675 C673 C711
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

Voltage reference (LT1389)

IO_1V8
R674 100K
D40 LT1389
GND VOUT
GND
NC1 NC7
NC2 NC8
NC3
C741 0.1uF

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Arria 10 Ground Connections

U23T

U23Z

A10SOC_1517

A10SOC_1517

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Core Power Decoupling

0.95V HPS is for boost mode

56 A10_0V9

0.9V Decoupling

C726	C594	C505	C474	C475	C769	C771	C668	C770	C768
100uF	100uF	100uF	100uF	100uF	100uF	100uF	100uF	100uF	100uF
6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V

C501	C528	C493	C747	C476	C477
100uF	100uF	100uF	100uF	100uF	100uF
6.3V	6.3V	6.3V	6.3V	6.3V	6.3V

C654	C646	C764	C652	C658	C590	C683	C574
0.1uF	0.1uF	1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C697	C681	C699	C684	C569	C687	C679	C698	C693
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C663	C629	C628	C613	C618	C540	C620	C553	C572
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C694	C576	C626	C541	C664	C570	C578	C547	C584
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C695	C585	C700	C692	C588	C582	C579	C551	C552
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C610	C535	C538	C631	C665	C623	C696	C549	C612
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C677	C586	C651	C583	C544	C609	C614	C691	C622
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C627	C539	C648	C542	C676	C701	C661	C580	C655
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C662	C688	C555	C630	C589	C587	C678	C556	C619
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C603	C536	C680	C686	C568	C682	C605	C575	C548
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C611	C537	C645	C660	C550	C607	C608	C647	C649
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C1591	C1592	C1593	C1594	C1595	C1596
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

U23. pin R23, R21, Ae14,Ae13,U19,AD16

---

59 HPS_0V95

DNI
R663
Only install for supporting NF5 FPGA

0.95V HPS VCCL

C778	C714	C689	C690	C685
100uF	0.1uF	0.1uF	0.1uF	0.1uF
6.3V				

58 0V95

3A

C641	C604	C625	C621	C615	C606	C624
100uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF
6.3V						

IO Power Decoupling

A10_1V0

60 A10_1V0

C510	C499	C516	C704	C557	C592	C666	C730	C743	C508	C526	C558	C633	C717	C737	C744	C703
330uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

C500	C509	C527	C559	C560	C634	C667	C705	C706	C718	C731	C738	C593	C517	C746	C745
4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF	4.7uF

PLL_1V8

68 PLL_1V8

C561	C656	C545	C571	C742	C736	C716	C591	C525	C507	C632	C702	C657	C581	C573	C577	C650	C659	C653	C1588	C1589	C1590
100uF 6.3V	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

PLL_1V8   L26   A10_VCCAPLL

0.1A   A10_VCCAPLL   74

3A, 30 Ohm FB

L27   A10VCCAPLLHPS

0.1A   A10VCCPLLHPS   74

3A, 30 Ohm FB

DNI
R664

Only install for supporting NF5 FPGA

A10_VCCAPLL

C617	C616
0.1uF	0.1uF

A10VCCAPLLHPS

C715
0.1uF

IO_1V8

36,37,68 IO_1V8

C497	C498	C515	C543	C674	C506	C496	C546	C642	C643	C761	C762	C1587
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

IO_1V8   0   R675   **0.1A**   VCCIO_HPS   74

DNI
R662   C713
0.1uF

Only install for supporting NF5 FPGA

67 FMCBVADJ

C486	C487	C1583
0.1uF	0.1uF	0.1uF

PLL_1V8   0   R673   **0.1A**   VCCIOREF_HPS   74

DNI
R660   C712
0.1uF

Only install for supporting NF5 FPGA

62 HILOHPS_VDD

C488	C489	C763	C735	C1578	C1579
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

64 HILO_VDDQ

C520	C534	C602	C533	C513	C519	C1580	C1581	C1582
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

4A

FMCAVADJ
66

C733	C727	C728	C710	C734	C729	C1584	C1585	C1586
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

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