system_pl_wrapper.v

AUTHORS

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DATES

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INFORMATION

Brief

System wrapper for pl only for zcu102 board.

License MIT

system_pl_wrapper

```
module system_pl_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
0,
parameter
FPGA_FAMILY
 =
0,
parameter
SPEED_GRADE
```

```
 =
0,
parameter
DEV_PACKAGE
 =
0,
parameter
ADC_INIT_DELAY
 =
23,
parameter
DAC_INIT_DELAY
 =
0,
parameter
DELAY_REFCLK_FREQUENCY
 =
200
) ( input axi_aclk, input axi_aresetn, input s_axi_awvalid, input [31:0] s_
```

System wrapper for pl only for zcu102 board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 1 is for 7 series.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 10 is for -1.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 14 is for cl.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

axi_aclk	AXI Lite control bus
axi_aresetn	AXI Lite control bus
s_axi_awvalid	AXI Lite control bus
s_axi_awaddr	AXI Lite control bus
s_axi_awready	AXI Lite control bus
s_axi_awprot	AXI Lite control bus
s_axi_wvalid	AXI Lite control bus
s_axi_wdata	AXI Lite control bus
s_axi_wstrb	AXI Lite control bus
s_axi_wready	AXI Lite control bus
s_axi_bvalid	AXI Lite control bus
s_axi_bresp	AXI Lite control bus
s_axi_bready	AXI Lite control bus

s_axi_arvalid	AXI Lite control bus
s_axi_araddr	AXI Lite control bus
s_axi_arready	AXI Lite control bus
s_axi_arprot	AXI Lite control bus
s_axi_rvalid	AXI Lite control bus
s_axi_rready	AXI Lite control bus
s_axi_rresp	AXI Lite control bus
s_axi_rdata	AXI Lite control bus
adc_dma_irq	fmcomms5 ADC irq
dac_dma_irq	fmcomms5 DAC irq
delay_clk	fmcomms5 delay clock
rx_clk_in_0_p	fmcomms5 0 rx clk
rx_clk_in_0_n	fmcomms5 0 rx clk
rx_frame_in_0_p	fmcomms5 0 rx frame
rx_frame_in_0_n	fmcomms5 0 rx frame
rx_data_in_0_p	fmcomms5 0 rx data
rx_data_in_0_n	fmcomms5 0 rx data
tx_clk_out_0_p	fmcomms5 0 tx clk
tx_clk_out_0_n	fmcomms5 0 tx clk
tx_frame_out_0_p	fmcomms5 0 tx frame
tx_frame_out_0_n	fmcomms5 0 tx frame
tx_data_out_0_p	fmcomms5 0 tx data
tx_data_out_0_n	fmcomms5 0 tx data
txnrx_0	fmcomms5 0 txnrx
enable_0	fmcomms5 0 enable
up_enable_0	fmcomms5 0 enable input
up_txnrx_0	fmcomms5 0 txnrx select input
tdd_sync_0_t	fmcomms5 0 TDD sync i/o
tdd_sync_0_i	fmcomms5 0 TDD sync i/o
tdd_sync_0_o	fmcomms5 0 TDD sync i/o
rx_clk_in_1_p	fmcomms5 1 rx clk
rx_clk_in_1_n	fmcomms5 1 rx clk
rx_frame_in_1_p	fmcomms5 1 rx frame
rx_frame_in_1_n	fmcomms5 1 rx frame
rx_data_in_1_p	fmcomms5 1 rx data
rx_data_in_1_n	fmcomms5 1 rx data
tx_clk_out_1_p	fmcomms5 1 tx clk
tx_clk_out_1_n	fmcomms5 1 tx clk
tx_frame_out_1_p	fmcomms5 1 tx frame
tx_frame_out_1_n	fmcomms5 1 tx frame
tx_data_out_1_p	fmcomms5 1 tx data

tx_data_out_1_n	fmcomms5 1 tx data
txnrx_1	fmcomms5 1 txnrx
enable_1	fmcomms5 1 enable
up_enable_1	fmcomms5 1 enable input
up_txnrx_1	fmcomms5 1 txnrx select input
tdd_sync_1_t	fmcomms5 1 TDD sync i/o
tdd_sync_1_i	fmcomms5 1 TDD sync i/o
tdd_sync_1_o	fmcomms5 1 TDD sync i/o
m_axi_aclk	DMA Clock
adc_m_dest_axi_awaddr	fmcomms5 ADC DMA
adc_m_dest_axi_awlen	fmcomms5 ADC DMA
adc_m_dest_axi_awsize	fmcomms5 ADC DMA
adc_m_dest_axi_awburst	fmcomms5 ADC DMA
adc_m_dest_axi_awprot	fmcomms5 ADC DMA
adc_m_dest_axi_awcache	fmcomms5 ADC DMA
adc_m_dest_axi_awvalid	fmcomms5 ADC DMA
adc_m_dest_axi_awready	fmcomms5 ADC DMA
adc_m_dest_axi_wdata	fmcomms5 ADC DMA
adc_m_dest_axi_wstrb	fmcomms5 ADC DMA
adc_m_dest_axi_wready	fmcomms5 ADC DMA
adc_m_dest_axi_wvalid	fmcomms5 ADC DMA
adc_m_dest_axi_wlast	fmcomms5 ADC DMA
adc_m_dest_axi_bvalid	fmcomms5 ADC DMA
adc_m_dest_axi_bresp	fmcomms5 ADC DMA
adc_m_dest_axi_bready	fmcomms5 ADC DMA
dac_m_src_axi_arready	fmcomms5 DAC DMA
dac_m_src_axi_arvalid	fmcomms5 DAC DMA
dac_m_src_axi_araddr	fmcomms5 DAC DMA
dac_m_src_axi_arlen	fmcomms5 DAC DMA
dac_m_src_axi_arsize	fmcomms5 DAC DMA
dac_m_src_axi_arburst	fmcomms5 DAC DMA
dac_m_src_axi_arprot	fmcomms5 DAC DMA
dac_m_src_axi_arcache	fmcomms5 DAC DMA
dac_m_src_axi_rdata	fmcomms5 DAC DMA
dac_m_src_axi_rready	fmcomms5 DAC DMA
dac_m_src_axi_rvalid	fmcomms5 DAC DMA
dac_m_src_axi_rresp	fmcomms5 DAC DMA
dac_m_src_axi_rlast	fmcomms5 DAC DMA

INSTANTIANTED MODULES

inst_dma_rstgen

```
dma_rstgen inst_dma_rstgen (
                                                                                .
slowest_sync_clk(m_axi_aclk),
                                                                                .
ext_reset_in(axi_aresetn),
                                                                                .
aux_reset_in(1'b1),
                                                                                .
mb_debug_sys_rst(1'b0),
                                                                                .
dcm_locked(1'b1),
                                                                                .
mb_reset(),
                                                                                .
bus_struct_reset(),
                                                                                .
peripheral_reset(),
                                                                                .
interconnect_aresetn(),
                                                                                .
peripheral_aresetn(m_axi_aresetn)
)
```

Generate a new DMA reset based on delay clock.