system_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2023/11/02

INFORMATION

Brief

System wrapper for pl and ps for zcu102 board.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
FPGA_TECHNOLOGY
 =
3,
parameter
FPGA_FAMILY
 =
4,
parameter
SPEED_GRADE
```

```
 =
20,
parameter
DEV_PACKAGE
 =
3,
parameter
DELAY_REFCLK_FREQUENCY
 =
500,
parameter
ADC_INIT_DELAY
 =
8,
parameter
DAC_INIT_DELAY
 =
0
) ( input [12:0] gpio_bd_i, output [ 7:0] gpio_bd_o, input rx_clk_in_0_p, in
```

System wrapper for pl and ps for zcu102 board.

Parameters

FPGA_TECHNOLOGY parameter	Type of FPGA, such as Ultrascale, Arria 10. 3 is for ultrascale+.
FPGA_FAMILY parameter	Sub type of fpga, such as GX, SX, etc. 4 is for zynq.
SPEED_GRADE parameter	Number that corresponds to the ships recommeneded speed. 20 is for -2.
DEV_PACKAGE parameter	Specify a number that is equal to the manufactures package. 3 is for ff.
DELAY_REFCLK_FREQUENCY parameter	Reference clock frequency used for ad_data_in instances
ADC_INIT_DELAY parameter	Initial Delay for the ADC
DAC_INIT_DELAY parameter	Initial Delay for the DAC

Ports

gpio_bd_i	gpio
gpio_bd_o	gpio
rx_clk_in_0_p	fmcomms5 0 rx clk
rx_clk_in_0_n	fmcomms5 0 rx clk
rx_frame_in_0_p	fmcomms5 0 rx frame
rx_frame_in_0_n	fmcomms5 0 rx frame
rx_data_in_0_p	fmcomms5 0 rx data
rx_data_in_0_n	fmcomms5 0 rx data
tx_clk_out_0_p	fmcomms5 0 tx clk
tx_clk_out_0_n	fmcomms5 0 tx clk
tx_frame_out_0_p	fmcomms5 0 tx frame
tx_frame_out_0_n	fmcomms5 0 tx frame

tx_data_out_0_p	fmcomms5 0 tx data
tx_data_out_0_n	fmcomms5 0 tx data
gpio_status_0	fmcomms5 0 gpio
gpio_ctl_0	fmcomms5 0 gpio
gpio_en_agc_0	fmcomms5 0 gpio
gpio_resetb_0	fmcomms5 0 gpio
gpio_debug_1_0	fmcomms5 0 gpio
gpio_debug_2_0	fmcomms5 0 gpio
gpio_calsw_1_0	fmcomms5 0 gpio
gpio_calsw_2_0	fmcomms5 0 gpio
gpio_ad5355_rfen	fmcomms5 0 gpio
gpio_ad5355_lock	fmcomms5 0 gpio
txnrx_0	fmcomms5 0 txnrx
enable_0	fmcomms5 0 enable
rx_clk_in_1_p	fmcomms5 1 rx clk
rx_clk_in_1_n	fmcomms5 1 rx clk
rx_frame_in_1_p	fmcomms5 1 rx frame
rx_frame_in_1_n	fmcomms5 1 rx frame
rx_data_in_1_p	fmcomms5 1 rx data
rx_data_in_1_n	fmcomms5 1 rx data
tx_clk_out_1_p	fmcomms5 1 tx clk
tx_clk_out_1_n	fmcomms5 1 tx clk
tx_frame_out_1_p	fmcomms5 1 tx frame
tx_frame_out_1_n	fmcomms5 1 tx frame
tx_data_out_1_p	fmcomms5 1 tx data
tx_data_out_1_n	fmcomms5 1 tx data
gpio_status_1	fmcomms5 1 gpio
gpio_ctl_1	fmcomms5 1 gpio
gpio_en_agc_1	fmcomms5 1 gpio
gpio_resetb_1	fmcomms5 1 gpio
gpio_debug_1_1	fmcomms5 1 gpio
gpio_debug_2_1	fmcomms5 1 gpio
gpio_calsw_1_1	fmcomms5 1 gpio
gpio_calsw_2_1	fmcomms5 1 gpio
txnrx_1	fmcomms5 1 txnrx
enable_1	fmcomms5 1 enable
mcs_sync	fmcomms5 sync
spi_ad9361_0	fmcomms5 ad9361 0 spi select
spi_ad9361_1	fmcomms5 ad9361 1 spi select
spi_ad5355	fmcomms5 ad5355 spi select
spi_clk	fmcomms5 spi clock
spi_mosi	fmcomms5 spi master out

spi_miso	fmcomms5 spi master in
ref_clk_p	fmcomms5 ref clock p
ref_clk_n	fmcomms5 ref clock n

INSTANTIANTED MODULES

i_ref_clk_ibuf_ds

```
IBUFDS i_ref_clk_ibuf_ds (
.I(ref_clk_p),
.IB(ref_clk_n),
.O(ref_clk_s_ds)
)
```

Module instance of IBUFGDS for LVDS to cmos clock

i_ref_clk_ibuf

```
BUFG i_ref_clk_ibuf (
.I(ref_clk_s_ds),
.O(ref_clk_s)
)
```

Module instance of BUFG for cmos clock

i_ref_clk_rbuf

```
BUFR #(
.BUFR_DIVIDE("BYPASS")
) i_ref_clk_rbuf ( .CLR (1'b0), .CE (1'b1), .I (ref_clk_s), .O (ref_clk))
```

Module instance of BUFR for cmos clock

inst_system_pl_wrapper

```
system_pl_wrapper #(
                                                                                .
FPGA_TECHNOLOGY(FPGA_TECHNOLOGY),
                                                                                .
FPGA_FAMILY(FPGA_FAMILY),
                                                                                .
SPEED_GRADE(SPEED_GRADE),
                                                                                .
DEV_PACKAGE(DEV_PACKAGE),
                                                                                .
ADC_INIT_DELAY(ADC_INIT_DELAY),
                                                                                .
DAC_INIT_DELAY(DAC_INIT_DELAY),
                                                                                .
DELAY_REFCLK_FREQUENCY(DELAY_REFCLK_FREQUENCY)
) inst_system_pl_wrapper ( .axi_aclk(s_axi_clk), .axi_aresetn(s_axi_aresetn
```

Module instance of system_pl_wrapper for the fmcomms2-3 device.