

# mod\_clock\_ena\_gen.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Generate a enable signal at some rate that divides the clock. This can be any rate. This enable will not be a 50% clock cycle or as stable as a pll. This uses the mod algorithm. Essentially it adds the number of ticks till it reaches the clock rate and then saves the remainder and generates a 1 cycle high pulse.

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## mod\_clock\_ena\_gen

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```
module mod_clock_ena_gen #(
  parameter
    CLOCK_SPEED
    =
    20000000,
  parameter
    START_AT_ZERO
    =
    0,
  parameter
    DELAY
    =
```

```
0  
) ( input clk, input rstn, input start0, input clr, input hold, input [31:0]
```

Mod rate enable generator

### Parameters

**CLOCK\_SPEED**      This is the aclk frequency in Hz  
*parameter*

**DELAY**              Delay the enable by a number of clock ticks  
*parameter*

### Ports

**clk**                  Clock used for enable generation

**rstn**                Negative reset for anything clocked on clk

**start0**             Start counter at rate if set. Otherwise set to CLOCK\_SPEED/2+rate (midpoint).

**clr**                 Clear counter back to start on active high asynchronously.

**hold**                hold enable low and pause + reset count till hold removed (low).

**rate**                rate that enable pulse will be generated, must be less than the clock rate.

**ena**                positive enable that is pulsed high at enable rate.