tb_cocotb.v

AUTHORS

JAY CONVERTINO

DATES

2025/01/27

INFORMATION

Brief

Test bench wrapper for cocotb

License MIT

tb_cocotb

```
module tb_cocotb #(
parameter
CLOCK_SPEED
  =
2000000,
parameter
DELAY
  =
0
) ( input clk, input rstn, input start0, input clr, input hold, input [31:0]
```

Mod rate enable generator test bench

Parameters

CLOCK_SPEED parameter	This is the aclk frequency in Hz
DELAY parameter	Delay the enable by a number of clock ticks

Ports

clk	Clock used for enable generation
rstn	Negative reset for anything clocked on clk
start0	Start counter at rate if set. Otherwise set to CLOCK_SPEED/2+rate (midpoint).
clr	Clear counter to initial values.
hold	hold enable low and pause + reset count till hold removed (low).
rate	rate that enable pulse will be generated, must be less then the clock rate.
ena	positive enable that is pulsed high at enable rate.

INSTANTIATED MODULES

dut

```
mod_clock_ena_gen #(
                                                                    .
CLOCK_SPEED(CLOCK_SPEED),
                                                                    .
DELAY(DELAY)
) dut ( .clk(clk), .rstn(rstn), .start0(start0), .clr(clr), .hold(hold), .ra
```

Device under test, mod_clock_ena_gen