tb_cocotb.v

AUTHORS

JAY CONVERTINO

DATES

2025/01/27

INFORMATION

Brief

Test bench wrapper for cocotb

License MIT

tb_cocotb

```verilog
module tb_cocotb #(
parameter
CLOCK_SPEED
  =
2000000,
parameter
START_AT_ZERO
  =
0,
parameter
DELAY
  =
0
) ( input clk, input rstn, input hold, input [31:0] rate, output ena )
```

Mod rate enable generator test bench

Parameters

CLOCK_SPEED   This is the aclk frequency in Hz
parameter

START_AT_ZERO   Start counter at 0 if set. Otherwise start at CLOCK_SPEED/2.
parameter

DELAY   Delay the enable by a number of clock ticks
parameter

Ports

clk   Clock used for enable generation

rstn   Negative reset for anything clocked on clk

hold   hold enable low and pause + reset count till hold removed (low).

rate   rate that enable pulse will be generated, must be less then the clock rate.

ena   positive enable that is pulsed high at enable rate.

INSTANTIATED MODULES

dut

```
mod_clock_ena_gen #(
                                                                      .
CLOCK_SPEED(CLOCK_SPEED),
                                                                      .
START_AT_ZERO(START_AT_ZERO),
                                                                      .
DELAY(DELAY)
) dut ( .clk(clk), .rstn(rstn), .hold(hold), .rate(rate), .ena(ena) )
```

Device under test, mod_clock_ena_gen