

tb_mod_ena.v

AUTHORS

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DATES

2025/01/27

INFORMATION

Brief

Test bench for mod clock divide enable generator

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tb_mod_ena

```
module tb_mod_ena #(
  parameter
    CLOCK_SPEED
    =
    20000000,
  parameter
    ENABLE_RATE
    =
    1000,
  parameter
    DELAY
    =
    0
)()
```

mod clock enable test bench

Parameters

CLOCK_SPEED parameter	Clock speed
START_AT_ZERO	Set to 1 to enable start at zero.
DELAY parameter	Set to the number of clock cycles to delay the enable output signal.

INSTANTIATED MODULES

clk_stim

```
clk_stimulus #(
    CLOCKS(1),
    CLOCK_BASE(CLOCK_SPEED),
    CLOCK_INC(1000),
    RESETS(1),
    RESET_BASE(2000),
    RESET_INC(100)
) clk_stim ( .clkv(tb_dut_clk), .rstnv(tb_dut_rstn), .rstv() )
```

Generate a 50/50 duty cycle set of clocks and reset.

dut

```
mod_clock_ena_gen #(
    CLOCK_SPEED(CLOCK_SPEED),
    DELAY(DELAY)
) dut ( .clk(tb_dut_clk), .rstn(tb_dut_rstn), .start0(1'b1), .clr(1'b0), .hd
```

Device under test, mod_clock_ena_gen