mod_clock_ena_gen.v

AUTHORS

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DATES

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INFORMATION

Brief

Generate a enable signal at some rate that divides the clock. This can be any rate. This enable will not be a 50% clock cycle or as stable as a pll. This uses the mod algorithm. Essentially it adds the number of ticks till it reaches the clock rate and then saves the remainder and generates a 1 cycle high pulse.

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mod_clock_ena_gen

```
module mod_clock_ena_gen #(
parameter
CLOCK_SPEED
  =
2000000,
parameter
START_AT_ZERO
  =
0,
parameter
DELAY
  =
```

```
 0
) ( input clk, input rstn, input start0, input clr, input hold, input [31:0]
```

Mod rate enable generator

Parameters

CLOCK_SPEED parameter	This is the aclk frequency in Hz
DELAY parameter	Delay the enable by a number of clock ticks

Ports

clk	Clock used for enable generation
rstn	Negative reset for anything clocked on clk
start0	Start counter at rate if set. Otherwise set to CLOCK_SPEED/2+rate (midpoint).
clr	Clear counter back to start on active high asycronusly.
hold	hold enable low and pause + reset count till hold removed (low).
rate	rate that enable pulse will be generated, must be less then the clock rate.
ena	positive enable that is pulsed high at enable rate.