piso.v

AUTHORS

JAY CONVERTINO

DATES

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INFORMATION

Brief

PISO (parallel in serial out) The idea is to keep this core simple, and let the control logic be handled outside of this core.

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piso

```
module piso #(
parameter
BUS_WIDTH
  =
1,
parameter
DEFAULT_RESET_VAL
  =
0,
parameter
DEFAULT_SHIFT_VAL
  =
0
```

```
) ( input wire clk, input wire rstn, input wire ena, input wire rev, input w
```

Parllel in serial out

Parametes

BUS_WIDTH	width of the parallel data input in bytes.
DEFAULT_RESET_VAL	Value that serial out will have after reset, default 0. Anything else will be 1.
DEFAULT_SHIFT_VAL	Value that will be shifted into the parallel output shift register. Default 0, anything else will be 1.

Ports

clk	global clock for the core.
rstn	negative syncronus reset to clk.
ena	enable for core, use to change output rate. Enable serial shift output.
rev	reverse, 0 is MSb first out, 1 is LSb first out.
load	load parallel data into core. Reset for next data message to send. This can be done at any time.
pdata	parallel data input, registered at load only.
reg_count_amount	If anything other than zero, the dcount and data output will use this value instead of the BUS_WIDTH size.
sdata	serialized data output.
dcount	Number of bits to shift out. 8 bit counter for up to 255. When the count hits zero, the parallel data register is empty and last bit is output on sdata.