

tb_cocotb.v

AUTHORS

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DATES

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INFORMATION

Brief

Test bench wrapper for cocotb

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tb_cocotb

```
module tb_cocotb #(
  parameter
  BUS_WIDTH
  =
  4
) ( input clk, input rstn, input ena, input rev, input load, input [BUS_WID
```

PISO Wrapper

Parameters

BUS_WIDTH Width of the parallel input in bytes
parameter

Ports

clk	Clock
rstn	negative reset
ena	enable for core, use to change output rate. Enable serial shift output.
rev	reverse, 0 is MSb first out, 1 is LSB first out.
load	load parallel data into core. This can be done at any time.
pdata	parallel data input, registered at load only.
sdata	serialized data output.
dcount	Number of bits to shift out (what is left, first bit is always available).

INSTANTIATED MODULES

dut

```
piso #(
    BUS_WIDTH(BUS_WIDTH)
) dut ( .clk(clk), .rstn(rstn), .ena(ena), .rev(rev), .load(load), .pdata(pdata), .sdata(sdata), .dcount(dcount) )
```

Device under test, piso