

# piso.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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PISO (parallel in serial out) The idea is to keep this core simple, and let the control logic be handled outside of this core.

### License MIT

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## piso

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```
module piso #(
  parameter
  BUS_WIDTH
  =
  1,
  parameter
  DEFAULT_RESET_VAL
  =
  0,
  parameter
  DEFAULT_SHIFT_VAL
  =
  0
```

```
|) ( input wire clk, input wire rstn, input wire ena, input wire rev, input v
```

Parallel in serial out

## Parameters

|                          |   |
|--------------------------|---|
| <b>BUS_WIDTH</b>         | width of the parallel data input in bytes.  |
| <b>DEFAULT_RESET_VAL</b> | Value that serial out will have after reset, default 0. Anything else will be 1.                        |
| <b>DEFAULT_SHIFT_VAL</b> | Value that will be shifted into the parallel output shift register. Default 0, anything else will be 1. |

## Ports

|                         |  |
|-------------------------|--|
| <b>clk</b>              | global clock for the core.   |
| <b>rstn</b>             | negative synchronus reset to clk.  |
| <b>ena</b>              | enable for core, use to change output rate. Enable serial shift output.  |
| <b>rev</b>              | reverse, 0 is MSb first out, 1 is LSB first out.   |
| <b>load</b>             | load parallel data into core. Reset for next data message to send. This can be done at any time.   |
| <b>pdata</b>            | parallel data input, registered at load only.  |
| <b>reg_count_amount</b> | If anything other than zero, the dcount and data output will use this value instead of the BUS_WIDTH size.   |
| <b>sdata</b>            | serialized data output.  |
| <b>dcount</b>           | Number of bits to shift out. 8 bit counter for up to 255. When the count hits zero, the parallel data register is empty and last bit is output on sdata. |