piso.v

AUTHORS

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DATES

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INFORMATION

Brief

PISO (parallel in serial out) The idea is to keep this core simple, and let the control logic be handled outside of this core.

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piso

```
module piso #(
parameter
BUS_WIDTH
 =
1
) ( input clk, input rstn, input ena, input rev, input load, input [BUS_WID
```

parllel in serial out

Parametes

BUS_WIDTH width of the parallel data input in bytes.

Ports

clk	global clock for the core.
rstn	negative syncronus reset to clk.
ena	enable for core, use to change output rate. Enable serial shift output.
rev	reverse, 0 is MSb first out, 1 is LSb first out.
load	load parallel data into core. Reset for next data message to send. This can be done at any time.
pdata	parallel data input, registered at load only.
sdata	serialized data output.
dcount	Number of bits to shift out. When the count hits zero, the parallel data register is empty and last bit is output on sdata.