

# sipo.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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SIPO (serial in parallel out) The idea is to keep this core simple, and let the control logic be handled outside of this core.

### License MIT

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## sipo

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```
module sipo #(
  parameter
    BUS_WIDTH
    =
  1
) ( input clk, input rstn, input ena, input load, output [BUS_WIDTH*8-1:0]
```

serial in parallel out

### Parametes

**BUS\_WIDTH** width of the parallel data input in bytes.

## Ports

<b>clk</b>	global clock for the core.
<b>rstn</b>	negative synchronus reset to clk.
<b>ena</b>	enable for core, use to change input rate. Enable serial shift input.
<b>load</b>	load parallel data from core, and reset counters for next incoming serial data.
<b>pdata</b>	parallel data output, valid when dcount is BUS_WIDTH*8.
<b>sdata</b>	serialized data input.
<b>dcount</b>	Number of bits to shift out. BUS_WIDTH*8 means all bits have been sampled and put into the register.