sipo.v

AUTHORS

JAY CONVERTINO

DATES

2025/04/15

INFORMATION

Brief

SIPO (serial in parallel out) The idea is to keep this core simple, and let the control logic be handled outside of this core.

License MIT

Copyright 2025 Jay Convertino

Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions:

The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software.

THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

sipo

```
module sipo #(
parameter
BUS_WIDTH
=
1,
parameter
COUNT_AMOUNT
=
0
) ( input wire clk, input wire rstn, input wire ena, input wire rev, input wire
```

Serial to Parallel out

Parametes

BUS_WIDTH width of the parallel data input in bytes.

Ports

clk global clock for the core.

negative syncronus reset to clk. rstn

enable for core, use to change input rate. Enable serial shift input. ena

reverse, 0 is MSb first out, 1 is LSb first out. rev

load load parallel data from core, and reset counters for next incoming serial data. pdata parallel data output, valid when dcount is BUS_WIDTH*8 or reg_count_amount If anything other than zero, the dcount and data output will use this value instead of the $\ensuremath{\mathsf{BUS_WIDTH}}$ size. reg_count_amount

sdata serialized data input.

Number of bits to shift out. BUS WIDTH*8 or COUNT AMOUNT means all bits dcount

have been sampled and put into the register.