sipo.v

AUTHORS

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DATES

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INFORMATION

Brief

SIPO (serial in parallel out) The idea is to keep this core simple, and let the control logic be handled outside of this core.

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sipo

```
module sipo #(
parameter
BUS_WIDTH
  =
1,
parameter
COUNT_AMOUNT
  =
0
) ( input wire clk, input wire rstn, input wire ena, input wire rev, input w
```

Serial to Parallel out

Parametes

BUS_WIDTH	width of the parallel data input in bytes.

Ports

clk	global clock for the core.
rstn	negative syncronus reset to clk.
ena	enable for core, use to change input rate. Enable serial shift input.
rev	reverse, 0 is MSb first out, 1 is LSb first out.
load	load parallel data from core, and reset counters for next incoming serial data.
pdata	parallel data output, valid when dcount is BUS_WIDTH*8 or reg_count_amount
reg_count_amount	If anything other than zero, the dcount and data output will use this value instead of the BUS_WIDTH size.
sdata	serialized data input.
dcount	Number of bits to shift out. BUS_WIDTH*8 or COUNT_AMOUNT means all bits have been sampled and put into the register.