

# sipo.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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SIPO (serial in parallel out) The idea is to keep this core simple, and let the control logic be handled outside of this core.

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## sipo

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```
module sipo #(
  parameter
    BUS_WIDTH
    =
    1,
  parameter
    COUNT_AMOUNT
    =
    0
) ( input wire clk, input wire rstn, input wire ena, input wire rev, input v
```

Serial to Parallel out

## Parameters

<b>BUS_WIDTH</b>	width of the parallel data input in bytes.
<b>COUNT_AMOUNT</b>	If anything other than zero, the dcount and data output will use this value instead of the BUS_WIDTH size.

## Ports

<b>clk</b>	global clock for the core.
<b>rstn</b>	negative synchronus reset to clk.
<b>ena</b>	enable for core, use to change input rate. Enable serial shift input.
<b>rev</b>	reverse, 0 is MSb first out, 1 is LSB first out.
<b>load</b>	load parallel data from core, and reset counters for next incoming serial data.
<b>pdata</b>	parallel data output, valid when dcount is BUS_WIDTH*8 or COUNT_AMOUNT.
<b>sdata</b>	serialized data input.
<b>dcount</b>	Number of bits to shift out. BUS_WIDTH*8 or COUNT_AMOUNT means all bits have been sampled and put into the register.