

sipo.v

AUTHORS

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DATES

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INFORMATION

Brief

SIPO (serial in parallel out) The idea is to keep this core simple, and let the control logic be handled outside of this core.

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sipo

```
module sipo #(
  parameter
    BUS_WIDTH
    =
  1
) ( input clk, input rstn, input ena, input rev, input load, output [BUS_W]
```

serial in parallel out

Parametes

BUS_WIDTH width of the parallel data input in bytes.

Ports

| | |
|---------------|--|
| clk | global clock for the core. |
| rstn | negative synchronus reset to clk. |
| ena | enable for core, use to change input rate. Enable serial shift input. |
| rev | reverse, 0 is MSb first out, 1 is LSB first out. |
| load | load parallel data from core, and reset counters for next incoming serial data. |
| pdata | parallel data output, valid when dcount is BUS_WIDTH*8. |
| sdata | serialized data input. |
| dcount | Number of bits to shift out. BUS_WIDTH*8 means all bits have been sampled and put into the register. |