sipo.v

AUTHORS

JAY CONVERTINO

DATES

2025/04/15

INFORMATION

Brief

SIPO (serial in parallel out) The idea is to keep this core simple, and let the control logic be handled outside of this core.

License MIT

sipo

```
module sipo #(
parameter
BUS_WIDTH
 =
1
) ( input clk, input rstn, input ena, input load, output [BUS_WIDTH*8-1:0]
```

serial in parallel out

Parametes

BUS_WIDTH width of the parallel data input in bytes.

Ports

clk	global clock for the core.
rstn	negative syncronus reset to clk.
ena	enable for core, use to change input rate. Enable serial shift input.
load	load parallel data from core, and reset counters for next incoming serial data.
pdata	parallel data output, valid when dcount is BUS_WIDTH*8.
sdata	serialized data input.
dcount	Number of bits to shift out. BUS_WIDTH*8 means all bits have been sampled and put into the register.