

# tb\_cocotb.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Test bench wrapper for cocotb

### License MIT

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## tb\_cocotb

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```
module tb_cocotb #(
  parameter
  BUS_WIDTH
  =
  4
) ( input clk, input rstn, input ena, input rev, input load, output [BUS_W
```

SIPO interface DUT

### Parameters

**BUS\_WIDTH**      Width of the data port in bytes.  
*parameter*

**Ports**

<b>clk</b>	Clock
<b>rstn</b>	negative reset
<b>ena</b>	enable for core, use to change input rate. Enable serial shift input.
<b>rev</b>	reverse, 0 is MSb first out, 1 is LSB first out.
<b>load</b>	load parallel data from core, and reset counters for next incoming serial data.
<b>pdata</b>	parallel data output, valid when dcount is BUS_WIDTH*8.
<b>sdata</b>	serialized data input.
<b>dcount</b>	Number of bits to shift out. BUS_WIDTH*8 means all bits have been sampled and put into the register.

**INSTANTIATED MODULES**

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**dut**

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```
sipo #(
    .BUS_WIDTH(BUS_WIDTH)
) dut ( .clk(clk), .rstn(rstn), .ena(ena), .rev(rev), .load(load), .pdata(pdata), .sdata(sdata), .dcount(dcount) )
```

Device under test, sipo