

system_wrapper.v

AUTHORS

JAY CONVERTINO

DATES

2024/11/25

INFORMATION

Brief

System wrapper for pl

License MIT

Copyright 2024 Jay Convertino

Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions:

The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software.

THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

system_wrapper

```
module system_wrapper #(
    parameter
    clock_speed
    =
    2000000,
    parameter
    baud_rate
    =
    1000000,
    parameter
    mil1553_sample_rate
```

```

    =
    2000000
) ( input clk, input [1:0] push_buttons, inout [7:0] pmod_ja, input ftdi_tx,

```

System wrapper for pl

Parameters

clock_speed <small>parameter</small>	Requested Master Clock Speed from clk wiz
baud_rate <small>parameter</small>	UART BAUD rate
mil1553_sample_rate <small>parameter</small>	Sample rate for 1553, must be 2 MHz or above, and divide evenly into clock_speed.

Ports

clk	Input clock for all clocks
push_buttons	Buttons used for reset (push button 0).
pmod_ja	1553 PMOD device port (JA)
ftdi_tx	FTDI UART input (TX)
ftdi_rx	FTDI UART output (RX)
ftdi_rts	FTDI Request To Send, input.
ftdi_cts	FTDI Clear to send, output.

INSTANTIATED MODULES

inst_clk_wiz_1

```

clk_wiz_1 inst_clk_wiz_1 (
    clk_out1(sys_clk),
    reset(push_buttons[0]),
    clk_in1(clk)
)

```

Module instance of clock wizard to change input clock to requested clock speed.

inst_sys_rstgen

```

sys_rstgen inst_sys_rstgen (
    slowest_sync_clk(sys_clk),
    ext_reset_in(push_buttons[0]),
    aux_reset_in(1'b1),
    mb_debug_sys_rst(1'b0),
    dcm_locked(1'b1),

```

```

mb_reset(),
bus_struct_reset(),
peripheral_reset(),
interconnect_aresetn(),
peripheral_aresetn(resetn)
)

```

Module instance of reset gen to create system reset.

inst_uart_1553_core

```

uart_1553_core #(
clock_speed(clock_speed),
uart_baud_clock_speed(clock_speed),
uart_baud_rate(baud_rate),
uart_parity_ena(0),
uart_parity_type(0),
uart_stop_bits(1),
uart_data_bits(8),
uart_rx_delay(0),
uart_tx_delay(0),
mil1553_sample_rate(mil1553_sample_rate),
mil1553_rx_bit_slice_offset(0),
mil1553_rx_invert_data(0),
mil1553_rx_sample_select(0)
) inst_uart_1553_core ( .aclk(sys_clk), .arstn(resetn), .uart_clk(sys_clk),

```

Module instance of the 1553 UART with all cores tied together as a common device.