

system_wrapper.v

AUTHORS

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DATES

2024/11/25

INFORMATION

Brief

System wrapper for pl

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system_wrapper

```
module system_wrapper #(
    parameter
    clock_speed
    =
    2000000,
    parameter
    baud_rate
    =
    1000000,
    parameter
    mil1553_sample_rate
```

```

    =
    2000000
) ( input clk, input [1:0] push_buttons, inout [7:0] pmod_ja, input ftdi_tx,

```

System wrapper for pl

Parameters

clock_speed <small>parameter</small>	Requested Master Clock Speed from clk wiz
baud_rate <small>parameter</small>	UART BAUD rate
mil1553_sample_rate <small>parameter</small>	Sample rate for 1553, must be 2 MHz or above, and divide evenly into clock_speed.

Ports

clk	Input clock for all clocks
push_buttons	Buttons used for reset (push button 0).
pmod_ja	1553 PMOD device port (JA)
ftdi_tx	FTDI UART input (TX)
ftdi_rx	FTDI UART output (RX)

INSTANTIATED MODULES

inst_clk_wiz_1

```

clk_wiz_1 inst_clk_wiz_1 (
    clk_out1(sys_clk),
    reset(push_buttons[0]),
    clk_in1(clk)
)

```

Module instance of clock wizard to change input clock to requested clock speed.

inst_sys_rstgen

```

sys_rstgen inst_sys_rstgen (
    slowest_sync_clk(sys_clk),
    ext_reset_in(1'b1),
    aux_reset_in(push_buttons[0]),
    mb_debug_sys_rst(1'b0),
    dcm_locked(1'b1),
    mb_reset(),
)

```

```

bus_struct_reset(),
peripheral_reset(reset),
interconnect_aresetn(),
peripheral_aresetn(resetn)
)

```

Module instance of reset gen to create system reset.

inst_uart_1553_core

```

uart_1553_core #(
clock_speed(clock_speed),
uart_baud_clock_speed(clock_speed),
uart_baud_rate(baud_rate),
uart_parity_ena(0),
uart_parity_type(0),
uart_stop_bits(1),
uart_data_bits(8),
uart_rx_delay(0),
uart_tx_delay(0),
mil1553_sample_rate(mil1553_sample_rate),
mil1553_rx_bit_slice_offset(0),
mil1553_rx_invert_data(0),
mil1553_rx_sample_select(0)
) inst_uart_1553_core ( .aclk(sys_clk), .arstn(resetn), .uart_clk(sys_clk),

```

Module instance of the 1553 UART with all cores tied together as a common device.