# tb_coctb.v

## AUTHORS

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## DATES

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## INFORMATION

### Brief

Test bench wrapper for cocotb

### License MIT



### tb_cocotb

```
module tb_cocotb #(
parameter
ADDRESS_WIDTH
  =
16,
parameter
BUS_WIDTH
  =
4
) ( input clk, input rstn, input [ADDRESS_WIDTH-1:0] s_apb_paddr, input [0:0
```

APB3 slave to uP interface DUT

### Parameters

| | |
|---|---|
| **ADDRESS_WIDTH**<br>parameter | Width of the APB3 address port in bits. |
| **BUS_WIDTH**<br>parameter | Width of the APB3 bus data port in bytes. |

### Ports

| | |
|---|---|
| **clk** | Clock |
| **rstn** | negative reset |
| **s_apb_paddr** | APB3 address bus, up to 32 bits wide. |
| **s_apb_psel** | APB3 select per slave (1 for this core). |
| **s_apb_penable** | APB3 enable device for multiple transfers after first. |
| **s_apb_pready** | APB3 ready is a output from the slave to indicate its able to process the request. |
| **s_apb_pwrite** | APB3 Direction signal, active high is a write access. Active low is a read access. |
| **s_apb_pwdata** | APB3 write data port. |
| **s_apb_prdata** | APB3 read data port. |
| **s_apb_pslverror** | APB3 error indicates transfer failure, not implimented. |
| **up_rreq** | uP bus read request |
| **up_rack** | uP bus read ack |
| **up_raddr** | uP bus read address |
| **up_rdata** | uP bus read data |
| **up_wreq** | uP bus write request |
| **up_wack** | uP bus write ack |
| **up_waddr** | uP bus write address |
| **up_wdata** | uP bus write data |

## INSTANTIATED MODULES

## dut

```
up_apb3 #(
                                                                                .
ADDRESS_WIDTH(ADDRESS_WIDTH),
                                                                                .
BUS_WIDTH(BUS_WIDTH)
) dut ( .clk(clk), .rstn(rstn), .s_apb_paddr(s_apb_paddr), .s_apb_psel(s_apb
```

Device under test, up_apb3