

UP\_APB3



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# 1 Usage

## 1.1 Introduction

This core converts the APB3 bus to the uP bus. This allows any core with a uP bus to be interfaced with a APB3 bus. These busses are very similar and is done with combinatoral logic only.

## 1.2 Dependencies

The following are the dependencies of the cores.

- fusesoc 2.X
- iverilog (simulation)
- cocotb (simulation)

### 1.2.1 fusesoc\_info Depenecies

- dep
  - AFRL:utility:helper:1.0.0

## 1.3 In a Project

This core is made to interface APB3 bus to uP based device cores. This is part of a family of converters based on Analog Devices uP specification. Using this allows usage of Analog Devices AXI Lite core, AFRL APB3, AFRL Wishbone Classic, and AFRL Wishbone Pipeline converters. Meaning any uP core can be easily customized to any bus quickly. These are made for relatively slow speed bus device interfaces. An example of a Verilog uP interface provided below.

```
//output signals assigned to registers.
assign up_rack  = r_up_rack;
assign up_wack  = r_up_wack;
assign up_rdata = r_up_rdata;
assign irq      = r_irq;

assign s_rx_ren = (up_raddr[3:0] == RX_FIFO_REG) &&
    ↪ up_rreq;

//up registers decoder
always @(posedge clk)
begin
    if(rstn == 1'b0)
```

```

begin
    r_up_rack    <= 1'b0;
    r_up_wack    <= 1'b0;
    r_up_rdata   <= 0;

    r_overflow   <= 1'b0;

    r_control_reg <= 0;
end else begin
    r_up_rack    <= 1'b0;
    r_up_wack    <= 1'b0;
    r_tx_wen     <= 1'b0;
    r_up_rdata   <= r_up_rdata;
    //clear reset bits
    r_control_reg[RESET_RX_BIT] <= 1'b0;
    r_control_reg[RESET_TX_BIT] <= 1'b0;

    if(rx_full == 1'b1)
    begin
        r_overflow <= 1'b1;
    end

    //read request
    r_up_rack <= up_rreq;

    if(up_rreq == 1'b1)
    begin
        case(up_raddr[3:0])
            RX_FIFO_REG: begin
                r_up_rdata <= rx_rdata & {{(BUS_WIDTH*8-
                    ↪ DATA_BITS){1'b0}}, {DATA_BITS{1'b1}}}};
            end
            STATUS_REG: begin
                r_up_rdata <= {{(BUS_WIDTH*8-8){1'b0}},
                    ↪ s_parity_err, s_frame_err, r_overflow,
                    ↪ r_irq_en, tx_full, tx_empty, rx_full,
                    ↪ rx_valid};
                r_overflow <= 1'b0;
            end
            default: begin
                r_up_rdata <= 0;
            end
        endcase
    end

    r_up_wack <= up_wreq;

```

```

//write request
if(up_wreq == 1'b1)
begin
    case(up_waddr[3:0])
        TX_FIFO_REG: begin
            r_tx_wdata <= up_wdata;
            r_tx_wen <= 1'b1;
        end
        CONTROL_REG: begin
            r_control_reg <= up_wdata;
        end
        default: begin
        end
    endcase
end
end
end

//up control register processing and fifo reset
always @(posedge clk)
begin
    if(rstn == 1'b0)
    begin
        r_rstn_rx_delay <= ~0;
        r_rstn_tx_delay <= ~0;
        r_irq_en <= 1'b0;
    end else begin
        r_rstn_rx_delay <= {1'b1, r_rstn_rx_delay[
            ↪ FIFO_DEPTH-1:1]};
        r_rstn_tx_delay <= {1'b1, r_rstn_tx_delay[
            ↪ FIFO_DEPTH-1:1]};

        if(r_control_reg[RESET_RX_BIT])
        begin
            r_rstn_rx_delay <= {FIFO_DEPTH{1'b0}};
        end

        if(r_control_reg[RESET_TX_BIT])
        begin
            r_rstn_tx_delay <= {FIFO_DEPTH{1'b0}};
        end

        if(r_control_reg[ENABLE_INTR_BIT] != r_irq_en)
        begin
            r_irq_en <= r_control_reg[ENABLE_INTR_BIT];
        end
    end
end

```

```
    end
  end
end
```

## 2 Architecture

The only module is the up\_apb3 module. It is listed below.

- **up\_apb3** Convert APB3 to the Analog Devices uP BUS. (see core for documentation).

Please see 5 for more information.

## 3 Building

The APB3 core is written in Verilog 2001. They should synthesize in any modern FPGA software. The core comes as a fusesoc packaged core and can be included in any other core. Be sure to make sure you have met the dependencies listed in the previous section. Linting is performed by verible using the lint target.

### 3.1 fusesoc

Fusesoc is a system for building FPGA software without relying on the internal project management of the tool. Avoiding vendor lock in to Vivado or Quartus. These cores, when included in a project, can be easily integrated and targets created based upon the end developer needs. The core by itself is not a part of a system and should be integrated into a fusesoc based system. Simulations are setup to use fusesoc and are a part of its targets.

### 3.2 Source Files

#### 3.2.1 fusesoc\_info File List

- src
  - src/up\_apb3.v
- tb
  - tb/tb\_apb3.v
- tb\_cocotb

- 'tb/tb\_cocotb.py': 'file\_type': 'user', 'copyto': '.'
- 'tb/tb\_cocotb.v': 'file\_type': 'verilogSource'

### 3.3 Targets

#### 3.3.1 fusesoc\_info Targets

- default  
Info: Default for IP intergration.
- lint  
Info: Lint with Verible
- sim  
Info: Base simulation using icarus as default.
- sim\_cocotb  
Info: Cocotb unit tests

### 3.4 Directory Guide

Below highlights important folders from the root of the directory.

1. **docs** Contains all documentation related to this project.
  - **manual** Contains user manual and github page that are generated from the latex sources.
  - **specs** Contains specifications for the bus.
2. **src** Contains source files for the core
3. **tb** Contains test bench files for iverilog and cocotb
  - **cocotb** testbench files

## 4 Simulation

There are a few different simulations that can be run for this core.

### 4.1 iverilog

iverilog is used for simple test benches for quick verification, visually, of the core.

### 4.2 cocotb

To use the cocotb tests you must install the following python libraries.

```
$ pip install cocotb
$ pip install cocotbext-up
$ pip install cocotbext-apb
```

Each module has a cocotb based simulation. These use the cocotb extensions APB and uP. To install these locally use the following.cocotb

```
$ pip install —breaksystem-packages -e .
```

- **sim\_cocotb** Standard simulation APB3 to uP conversion using cocotbexts.

Then you must use the cocotb sim target. The targets above can be run with various parameters.

```
$ fusesoc run —target sim_cocotb AFRL:bus:up_apb3
  ↪ :1.0.0
```



## 5 Module Documentation

- **up\_apb3** APB3 to uP converter
- **tb\_apb3-v** Verilog test bench
- **tb\_cocotb-py** Cocotb python test routines
- **tb\_cocotb-v** Cocotb verilog test bench

The next sections document the module in detail.

## up\_apb3.v

---

### AUTHORS

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JAY CONVERTINO

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### DATES

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2024/03/19

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### INFORMATION

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#### Brief

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APB3 slave to uP interface

#### License MIT

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## up\_apb3

---

```
module up_apb3 #(
    parameter
    ADDRESS_WIDTH
    =
    16,
    parameter
    BUS_WIDTH
    =
    4
) ( input clk, input rstn, input [ADDRESS_WIDTH-1:0] s_apb_paddr, input [0:0] s_apb_wdata,
```

APB3 slave to uP interface

## Parameters

<code>ADDRESS_WIDTH</code> <small>parameter</small>	Width of the APB3 address port in bits.
<code>BUS_WIDTH</code> <small>parameter</small>	Width of the APB3 bus data port in bytes.

## Ports

<code>clk</code>	Clock
<code>rstn</code>	negative reset
<code>s_apb_paddr</code>	APB3 address bus, up to 32 bits wide.
<code>s_apb_psel</code>	APB3 select per slave (1 for this core).
<code>s_apb_penable</code>	APB3 enable device for multiple transfers after first.
<code>s_apb_pready</code>	APB3 ready is a output from the slave to indicate its able to process the request.
<code>s_apb_pwrite</code>	APB3 Direction signal, active high is a write access. Active low is a read access.
<code>s_apb_pwdata</code>	APB3 write data port.
<code>s_apb_prdata</code>	APB3 read data port.
<code>s_apb_pslverror</code>	APB3 error indicates transfer failure, not implimented.
<code>up_rreq</code>	uP bus read request
<code>up_rack</code>	uP bus read ack
<code>up_raddr</code>	uP bus read address
<code>up_rdata</code>	uP bus read data
<code>up_wreq</code>	uP bus write request
<code>up_wack</code>	uP bus write ack
<code>up_waddr</code>	uP bus write address
<code>up_wdata</code>	uP bus write data

## VARIABLES

---

### valid

---

```
assign valid = s_apb_psel & s_apb_penable & rstn
```

This will add an extra clock cycle. since enable happens after select. both are needed to use the device.

### s\_apb\_pslverror

---

```
assign s_apb_pslverror = 1'b0
```

APB3 error is always 0, no error.

### up\_waddr

---

```
assign up_waddr = s_apb_paddr[ADDRESS_WIDTH-1:shift]
```

up\_waddr and s\_apb\_addr are a direct mapping.

## up\_waddr

---

up\_raddr and s\_apb\_addr are a direct mapping.

## up\_wdata

---

```
assign up_wdata = s_apb_pdata
```

up\_wdata and s\_apb\_pdata are a direct mapping.

## s\_apb\_prdata

---

```
assign s_apb_prdata = up_rdata
```

s\_apb\_prdata and up\_rdata are a direct mapping.

## up\_wreq

---

```
assign up_wreq = valid & s_apb_pwrite & r_cycle
```

uP write request is a combination of the APB3 valid and APB3 write select (active high is write).

## up\_rreq

---

```
assign up_rreq = valid & ~s_apb_pwrite & r_cycle
```

uP read request is a combination of the APB3 valid and APB3 write select (active low is read).

## s\_apb\_pready

---

```
assign s_apb_pready = (  
  up_wack |  
  up_rack  
) & rstn
```

Ready is being treated like a awk

## tb\_apb3.v

---

### AUTHORS

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JAY CONVERTINO

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### DATES

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2021/06/23

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### INFORMATION

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#### Brief

---

Test bench for apb3 slave

#### License MIT

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## tb\_apb3

---

```
module tb_apb3 (
```

Test bench for apb3 slave. simple write and then read.

### INSTANTIATED MODULES

---

#### up\_apb3

---

```
up_apb3 #(
```

```

ADDRESS_WIDTH(16),
BUS_WIDTH(4)
) dut ( .clk(tb_data_clk), .rstn(tb_rstn), .s_apb_paddr(r_apb_paddr), .s_apb

```

Device under test, apb3 to uP

# tb\_cocotb.py

---

## AUTHORS

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JAY CONVERTINO

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## DATES

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2025/03/04

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## INFORMATION

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### Brief

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Cocotb test bench

### License MIT

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## FUNCTIONS

---

### random\_bool

---

```
def random_bool()
```

Return a infinite cycle of random bools

Returns: List

### start\_clock

---

```
def start_clock(  
    dut  
)
```

Start the simulation clock generator.

### Parameters

**dut** Device under test passed from cocotb test function

## reset\_dut

---

```
async def reset_dut(  
    dut  
)
```

Cocotb coroutine for resets, used with await to make sure system is reset.

## increment test

---

Coroutine that is identified as a test routine. Write data, on one clock edge, read on the next.

### Parameters

**dut** Device under test passed from cocotb.

## increment test stream

---

Coroutine that is identified as a test routine. Write data, in a stream to registers, then read back stream.

### Parameters

**dut** Device under test passed from cocotb.

## in\_reset

---

```
@cocotb.test()  
async def in_reset(  
    dut  
)
```

Coroutine that is identified as a test routine. This routine tests if device stays in unready state when in reset.

### Parameters

**dut** Device under test passed from cocotb.

## no\_clock

---

```
@cocotb.test()  
async def no_clock(  
    dut  
)
```



---

Coroutine that is identified as a test routine. This routine tests if no ready when clock is lost and device is left in reset.

### Parameters

**dut**     Device under test passed from cocotb.

## tb\_coctb.v

---

### AUTHORS

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JAY CONVERTINO

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### DATES

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2025/03/26

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### INFORMATION

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#### Brief

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Test bench wrapper for cocotb

#### License MIT

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## tb\_cocotb

---

```
module tb_cocotb #(
  parameter
    ADDRESS_WIDTH
    =
    16,
  parameter
    BUS_WIDTH
    =
    4
) ( input clk, input rstn, input [ADDRESS_WIDTH-1:0] s_apb_paddr, input [0:0] s_apb_wdata,
```

APB3 slave to uP interface DUT

## Parameters

<b>ADDRESS_WIDTH</b> parameter	Width of the APB3 address port in bits.
<b>BUS_WIDTH</b> parameter	Width of the APB3 bus data port in bytes.

## Ports

<b>clk</b>	Clock
<b>rstn</b>	negative reset
<b>s_apb_paddr</b>	APB3 address bus, up to 32 bits wide.
<b>s_apb_psel</b>	APB3 select per slave (1 for this core).
<b>s_apb_penable</b>	APB3 enable device for multiple transfers after first.
<b>s_apb_pready</b>	APB3 ready is a output from the slave to indicate its able to process the request.
<b>s_apb_pwrite</b>	APB3 Direction signal, active high is a write access. Active low is a read access.
<b>s_apb_pwdata</b>	APB3 write data port.
<b>s_apb_prdata</b>	APB3 read data port.
<b>s_apb_pslverror</b>	APB3 error indicates transfer failure, not implimented.
<b>up_rreq</b>	uP bus read request
<b>up_rack</b>	uP bus read ack
<b>up_raddr</b>	uP bus read address
<b>up_rdata</b>	uP bus read data
<b>up_wreq</b>	uP bus write request
<b>up_wack</b>	uP bus write ack
<b>up_waddr</b>	uP bus write address
<b>up_wdata</b>	uP bus write data

## INSTANTIATED MODULES

---

### dut

---

```
up_apb3 #(
    ADDRESS_WIDTH(ADDRESS_WIDTH),
    BUS_WIDTH(BUS_WIDTH)
) dut ( .clk(clk), .rstn(rstn), .s_apb_paddr(s_apb_paddr), .s_apb_psel(s_apb_psel), .s_apb_penable(s_apb_penable), .s_apb_pready(s_apb_pready), .s_apb_pwrite(s_apb_pwrite), .s_apb_pwdata(s_apb_pwdata), .s_apb_prdata(s_apb_prdata), .s_apb_pslverror(s_apb_pslverror), .up_rreq(up_rreq), .up_rack(up_rack), .up_raddr(up_raddr), .up_rdata(up_rdata), .up_wreq(up_wreq), .up_wack(up_wack), .up_waddr(up_waddr), .up_wdata(up_wdata))
```

Device under test, up\_apb3