

# up\_apb3.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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APB3 slave to uP interface

### License MIT

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## up\_apb3

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```
module up_apb3 #(
    parameter
    ADDRESS_WIDTH
    =
    16,
    parameter
    BUS_WIDTH
    =
    4
) ( input clk, input rstn, input [ADDRESS_WIDTH-1:0] s_apb_paddr, input [0:0] s_apb_wdata,
```

APB3 slave to uP interface

## Parameters

<b>ADDRESS_WIDTH</b> parameter	Width of the APB3 address port in bits.
<b>BUS_WIDTH</b> parameter	Width of the APB3 bus data port in bytes.

## Ports

<b>clk</b>	Clock
<b>rstn</b>	negative reset
<b>s_apb_paddr</b>	APB3 address bus, up to 32 bits wide.
<b>s_apb_psel</b>	APB3 select per slave (1 for this core).
<b>s_apb_penable</b>	APB3 enable device for multiple transfers after first.
<b>s_apb_pready</b>	APB3 ready is a output from the slave to indicate its able to process the request.
<b>s_apb_pwrite</b>	APB3 Direction signal, active high is a write access. Active low is a read access.
<b>s_apb_pwdata</b>	APB3 write data port.
<b>s_apb_prdata</b>	APB3 read data port.
<b>s_apb_pslverror</b>	APB3 error indicates transfer failure, not implimented.
<b>up_rreq</b>	uP bus read request
<b>up_rack</b>	uP bus read ack
<b>up_raddr</b>	uP bus read address
<b>up_rdata</b>	uP bus read data
<b>up_wreq</b>	uP bus write request
<b>up_wack</b>	uP bus write ack
<b>up_waddr</b>	uP bus write address
<b>up_wdata</b>	uP bus write data

## VARIABLES

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### valid

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```
assign valid = s_apb_psel & s_apb_penable & rstn
```

This will add an extra clock cycle. since enable happens after select. both are needed to use the device.

### s\_apb\_pslverror

---

```
assign s_apb_pslverror = 1'b0
```

APB3 error is always 0, no error.

### up\_waddr

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```
assign up_waddr = s_apb_paddr[ADDRESS_WIDTH-1:shift]
```

up\_waddr and s\_apb\_addr are a direct mapping.

## up\_waddr

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up\_raddr and s\_apb\_addr are a direct mapping.

## up\_wdata

---

```
assign up_wdata = s_apb_pdata
```

up\_wdata and s\_apb\_pdata are a direct mapping.

## s\_apb\_prdata

---

```
assign s_apb_prdata = up_rdata
```

s\_apb\_prdata and up\_rdata are a direct mapping.

## up\_wreq

---

```
assign up_wreq = valid & s_apb_pwrite
```

uP write request is a combination of the APB3 valid and APB3 write select (active high is write).

## up\_rreq

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```
assign up_rreq = valid & ~s_apb_pwrite
```

uP read request is a combination of the APB3 valid and APB3 write select (active low is read).

## s\_apb\_pready

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```
assign s_apb_pready = (
    up_rack |                                up_wack |
    valid ~
) & rstn
```

Diagrams seem to indicate that we should indicate ready when not sel and enable, which is why valid is complimented.