

# up\_wishbone\_classic.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Wishbone Classic slave to uP interface

### License MIT

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## up\_wishbone\_standard

---

```
module up_wishbone_standard #(
    parameter
    ADDRESS_WIDTH
    =
    16,
    parameter
    BUS_WIDTH
    =
    4
) ( input clk, input rst, input s_wb_cyc, input s_wb_stb, input s_wb_we, in
```

Wishbone Classic Standard slave to uP

## Parameters

<b>ADDRESS_WIDTH</b> parameter	Width of the Wishbone address port in bits.
<b>BUS_WIDTH</b> parameter	Width of the Wishbone bus data port in bytes.

## Ports

<b>clk</b>	Clock
<b>rst</b>	Positive reset
<b>s_wb_cyc</b>	Bus Cycle in process
<b>s_wb_stb</b>	Valid data transfer cycle
<b>s_wb_we</b>	Active High write, low read
<b>s_wb_addr</b>	Bus address
<b>s_wb_data_i</b>	Input data
<b>s_wb_sel</b>	Device Select
<b>s_wb_ack</b>	Bus transaction terminated
<b>s_wb_data_o</b>	Output data
<b>s_wb_err</b>	Active high when a bus error is present
<b>up_rreq</b>	uP bus read request
<b>up_rack</b>	uP bus read ack
<b>up_raddr</b>	uP bus read address
<b>up_rdata</b>	uP bus read data
<b>up_wreq</b>	uP bus write request
<b>up_wack</b>	uP bus write ack
<b>up_waddr</b>	uP bus write address
<b>up_wdata</b>	uP bus write data

## VARIABLES

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### valid

---

```
assign valid = s_wb_cyc & s_wb_stb & ~r_rst[0]
```

Indicate valid request from wishbone.

### up\_rreq

---

```
assign up_rreq = ~s_wb_we & valid & r_req
```

Convert wishbone read requests to up requests

### up\_wreq

---

```
assign up_wreq = s_wb_we & valid & r_req
```

Convert wishbone write requests to up requests

## s\_wb\_err

---

```
assign s_wb_err = r_err
```

check for errors

## up\_raddr

---

```
assign up_raddr = (
    s_wb_addr[ADDRESS_WIDTH-1:shift]          ~s_wb_we & ~r_rst[0] ?
    :
    0
)
```

assign address to read address port if selected

## up\_waddr

---

```
assign up_waddr = (
    s_wb_addr[ADDRESS_WIDTH-1:shift]          s_wb_we & ~r_rst[0] ?
    :
    0
)
```

assign address to write address port if selected

## up\_ack

---

```
assign up_ack = (
    up_rack |
    up_wack
)
```

ack is ack for both, or them so either may pass

## s\_wb\_ack

---

```
assign s_wb_ack = up_ack
```

combined uP ack is wishbone ack.