

# up\_wishbone\_pipeline.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Wishbone Pipeline Slave to uP interface

### License MIT

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## up\_wishbone\_pipeline

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```
module up_wishbone_pipeline #(
    parameter
    ADDRESS_WIDTH
    =
    16,
    parameter
    BUS_WIDTH
    =
    4
) ( input clk, input rst, input s_wb_cyc, input s_wb_stb, input s_wb_we, inp
```

Wishbone Classic slave to uP up\_wishbone\_classic

## Parameters

**ADDRESS\_WIDTH** Width of the Wishbone address port in bits.

parameter

**BUS\_WIDTH** Width of the Wishbone bus data port in bytes.

parameter

## Ports

<b>clk</b>	Clock
<b>rst</b>	Positive reset
<b>s_wb_cyc</b>	Bus Cycle in process
<b>s_wb_stb</b>	Valid data transfer cycle
<b>s_wb_we</b>	Active High write, low read
<b>s_wb_addr</b>	Bus address
<b>s_wb_data_i</b>	Input data
<b>s_wb_sel</b>	Device Select
<b>s_wb_bte</b>	Burst Type Extension
<b>s_wb_cti</b>	Cycle Type
<b>s_wb_ack</b>	Bus transaction terminated
<b>s_wb_data_o</b>	Output data
<b>s_wb_err</b>	Active high when a bus error is present
<b>up_rreq</b>	uP bus read request
<b>up_rack</b>	uP bus read ack
<b>up_raddr</b>	uP bus read address
<b>up_rdata</b>	uP bus read data
<b>up_wreq</b>	uP bus write request
<b>up_wack</b>	uP bus write ack
<b>up_waddr</b>	uP bus write address
<b>up_wdata</b>	uP bus write data

## VARIABLES

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### valid

---

```
assign valid = s_wb_cyc & s_wb_stb & ~r_rst[0]
```

Indicate valid request from wishbone.

### s\_wb\_stall

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```
assign s_wb_stall = ~up_ack & s_wb_cyc & ~r_rst[0]
```

if we have not ack'd, cyc is active stall the bus

## up\_rreq

---

```
assign up_rreq = (
    s_wb_cyc                                     r_up_rreq ? r_up_rreq &
    :
    valid & ~s_wb_we & ~r_rst[0]
)
```

Convert wishbone read requests to up read requests

## up\_wreq

---

```
assign up_wreq = (
    s_wb_cyc                                     r_up_wreq ? r_up_wreq &
    :
    valid & s_wb_we & ~r_rst[0]
)
```

Convert wishbone write requests to up write requests

## up\_ack

---

```
assign up_ack = (
    up_rack |
    up_wack
)
```

ack is ack for both, or them so either may pass

## s\_wb\_ack

---

```
assign s_wb_ack = up_ack & ~r_rst[0]
```

combined uP ack is wishbone ack.

## up\_raddr

---

```
assign up_raddr = (
    s_wb_addr                                     ~s_wb_we & ~r_rst[0] ?
    :
    0
)
```

assign wishbone address to read port if selected

## up\_waddr

---

```
assign up_waddr = (
    s_wb_addr
    :
    0
)
```

assign wishbone address to write port if selected