## tb wishbone slave.v **AUTHORS** JAY CONVERTINO **DATES** 2021/06/23 **INFORMATION Brief** Test bench for wishbone classic slave License MIT Copyright 2021 Jay Convertino Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions: The above copyright notice and this permission notice shall be included in all copies or substantial portions THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE. tb wishbone slave module tb\_wishbone\_slave () Test bench for apb3 slave. simple write and then read. **INSTANTIATED MODULES** dut up\_wishbone\_standard #(

```
ADDRESS_WIDTH(16),

BUS_WIDTH(4)
) dut ( .clk(tb_data_clk), .rst(tb_rst), .s_wb_cyc(r_wb_cyc), .s_wb_stb(r_wk
```

Device under test, up\_wishbone\_standard to uP