

# tb\_cocotb.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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Test bench wrapper for cocotb

### License MIT

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## tb\_cocotb

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```
module tb_cocotb #(
  parameter
    ADDRESS_WIDTH
    =
    16,
  parameter
    BUS_WIDTH
    =
    4
) ( input clk, input rst, output rstn, input s_wb_cyc, input s_wb_stb, input
```

Wishbone Classic slave to uP up\_wishbone\_classic DUT

Parameters

<b>ADDRESS_WIDTH</b> <small>parameter</small>	Width of the Wishbone address port in bits.
<b>BUS_WIDTH</b> <small>parameter</small>	Width of the Wishbone bus data port in bytes.

Ports

<b>clk</b>	Clock
<b>rst</b>	Positive reset
<b>s_wb_cyc</b>	Bus Cycle in process
<b>s_wb_stb</b>	Valid data transfer cycle
<b>s_wb_we</b>	Active High write, low read
<b>s_wb_addr</b>	Bus address
<b>s_wb_data_i</b>	Input data
<b>s_wb_sel</b>	Device Select
<b>s_wb_ack</b>	Bus transaction terminated
<b>s_wb_data_o</b>	Output data
<b>s_wb_err</b>	Active high when a bus error is present
<b>up_rreq</b>	uP bus read request
<b>up_rack</b>	uP bus read ack
<b>up_raddr</b>	uP bus read address
<b>up_rdata</b>	uP bus read data
<b>up_wreq</b>	uP bus write request
<b>up_wack</b>	uP bus write ack
<b>up_waddr</b>	uP bus write address
<b>up_wdata</b>	uP bus write data

INSTANTIATED MODULES

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dut

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```
up_wishbone_standard #(
    ADDRESS_WIDTH(ADDRESS_WIDTH),
    BUS_WIDTH(BUS_WIDTH)
) dut ( .clk(clk), .rst(rst), .s_wb_cyc(s_wb_cyc), .s_wb_stb(s_wb_stb), .s_wb_we(s_wb_we), .s_wb_addr(s_wb_addr), .s_wb_data_i(s_wb_data_i), .s_wb_sel(s_wb_sel), .s_wb_ack(s_wb_ack), .s_wb_data_o(s_wb_data_o), .s_wb_err(s_wb_err), .up_rreq(up_rreq), .up_rack(up_rack), .up_raddr(up_raddr), .up_rdata(up_rdata), .up_wreq(up_wreq), .up_wack(up_wack), .up_waddr(up_waddr), .up_wdata(up_wdata))
```

Device under test, up\_wishbone\_standard