UTIL_HELPER

November 26, 2024

Jay Convertino

Contents

1 Usage

1.1 Introduction

Util helper are sets of different header functions that can be included with Verilog source code. These functions are safe for synthesis if used correctly. Such as generating contants used in the source code. The current helper utility files are.

- util_helper_math.vh
    1. int clogb2(value) ... will return the log base 2 of the argument (value), rounded up to the nearest integer.
    2. int cmax(max1, max2) ... will return the number that is the max of the arguments max1, max2.
    3. int abs(value) ... will return the absolute value of the argument passed.

Fusesoc will require a dependency include, like the following.

```
dep:
  depend:
    - AFRL:utility:helper:1.0.0
```

It will also have to be included in the file you would like to use the functions in. An example is...

```
module flip_flop (input clk, input rst, input Q, output D
    ↪ );

`include "util_helper_math.vh"

endmodule
```

1.2 Dependencies

The following are the dependencies of the cores.

- fusesoc 2.X
- iverilog (simulation)

1.3 fusesoc

Fusesoc is a system for building FPGA software without relying on the internal project management of the tool. Avoiding vendor lock in to Vivado or Quartus. These cores, when included in a project, can be

easily integrated and targets created based upon the end developer needs. The core by itself is not a part of a system and should be integrated into a fusesoc based system. Simulations are setup to use fusesoc and are a part of its targets.

1.4 Source Files

1.4.1 fusesoc_info File List

- src
  - 'src/util_helper_math.vh': 'is_include_file': True
- tb
  - tb/tb_helper.v

1.5 Targets

1.5.1 fusesoc_info Targets

- default

  Info: Include all helper functions for verilog.

- sim

  Info: Test helper funtions.

1.6 Directory Guide

Below highlights important folders from the root of the directory.

1. **docs** Contains all documentation related to this project.
   - **manual** Contains user manual and github page that are generated from the latex sources.
2. **src** Contains source files for util_helper.
3. **tb** Contains test bench files.

2 Simulation

A barebones test bench for iverilog is included in tb/tb_helper.v . This can be run from fusesoc with the following.

```
$ fusesoc run --target=sim AFRL:utility:helper:1.0.0
```

3 Module Documentation

This project has multiple functions.

- **util_helper_math.vh**
- **tb_helper.v**

The next sections documents various functions per header.

util_helper_math.vh

AUTHORS

JAY CONVERTINO

DATES

2022/08/19

INFORMATION

Brief

helper functions for verilog relating to math.

License MIT

FUNCTIONS

clogb2

```
function integer clogb2
```

Copied from the IEEE 1364-2001 Standard, int clogb2(value) will return the log base 2 of the argument (value), rounded up to the nearest integer.

cmax

```
function integer cmax
```

int cmax(max1, max2) ... will return the number that is the max of the arguments max1, max2.

abs

```
function integer abs
```

int abs(value) ... will return the absolute value of the argument passed.

tb_helper.v

AUTHORS

JAY CONVERTINO

DATES

2022/08/10

INFORMATION

Brief

test bench helper functions for verilog relating to math.

License MIT

tb_helper

```
module tb_helper
```

test bench helper functions for verilog relating to math.