system_wrapper.v

AUTHORS

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DATES

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INFORMATION

Brief

System wrapper for ps.

License MIT

system_wrapper

```
module system_wrapper (
                                                                `ifdef _JTAG_IO

input
tck,
input
tms,
input
tdi,
output
tdo,
                                                                `endif
```

```
input
clk,
input
resetn,
                                                    inout [
12:0]
ddr2_addr,
                                                   inout [
2:0]
ddr2_ba,
inout
ddr2_cas_n,
inout
ddr2_ck_n,
inout
ddr2_ck_p,
inout
ddr2_cke,
inout
ddr2_cs_n,
                                                   inout [
1:0]
ddr2_dm,
                                                    inout [
15:0]
ddr2_dq,
                                                   inout [
1:0]
ddr2_dqs_n,
                                                   inout [
1:0]
ddr2_dqs_p,
inout
ddr2_odt,
inout
ddr2_ras_n,
inout
ddr2_reset_n,
inout
ddr2_we_n,
output
eth_mdc,
inout
eth_mdio,
input
eth_rstn,
input
eth_crsdv,
input
eth_rxerr,
                                                    input [
1:0]
eth_rxd,
output
eth_txen,
                                                   output [
1:0]
eth_txd,
output
eth_refclk,
input
eth_50mclk,
                                                  output [
3:0]
vga_r,
                                                  output [
```

```
3:0]
vga_g,
                                                                output [
3:0]
vga_b,
output
vga_hs,
output
vga_vs,
                                                                output [
15:0]
leds,
                                                                 input [
15:0]
slide_switches,
input
ftdi_tx,
output
ftdi_rx,
input
ftdi_rts,
output
ftdi_cts,
                                                                 inout [
3:0]
qspi_dq,
output
qspi_csn,
output
sd_reset,
input
sd_cd,
output
sd_sck,
inout
sd_cmd,
                                                                inout [
3:0]
sd_dat
)
```

System wrapper for Vexriscv Veronica RISCV ps.

Ports

tck `ifdef _JTAG_IO input`	JTAG
tms `input`	JTAG
tdi `input`	JTAG
tdo `output`	JTAG
clk `endif input`	Master Input Clock
resetn `input`	Master Reset Input
ddr2_addr `inout[ 12: 0]`	DDR interface
ddr2_ba `inout[ 2: 0]`	DDR interface

ddr2_cas_n inout	DDR interface
ddr2_ck_n inout	DDR interface
ddr2_ck_p inout	DDR interface
ddr2_cke inout	DDR interface
ddr2_cs_n inout	DDR interface
ddr2_dm inout[1: 0]	DDR interface
ddr2_dq inout[15: 0]	DDR interface
ddr2_dqs_n inout[1: 0]	DDR interface
ddr2_dqs_p inout[1: 0]	DDR interface
ddr2_odt inout	DDR interface
ddr2_ras_n inout	DDR interface
ddr2_reset_n inout	DDR interface
ddr2_we_n inout	DDR interface
eth_mdc output	ethernet interface
eth_mdio inout	ethernet interface
eth_rstn input	ethernet interface
eth_crsdv input	ethernet interface
eth_rxerr input	ethernet interface
eth_rxd input[1: 0]	ethernet interface
eth_txen output	ethernet interface
eth_txd output[1: 0]	ethernet interface
eth_refclk output	ethernet interface
eth_50mclk input	ethernet interface
vga_r output[3: 0]	vga interface
vga_g output[3: 0]	vga interface

vga_b output[3: 0]	vga interface
vga_hs output	vga interface
vga_vs output	vga interface
leds output[15: 0]	board leds
slide_switches input[15: 0]	board slide switches
ftdi_tx input	FTDI UART TX
ftdi_rx output	FTDI UART RX
ftdi_rts input	FTDI UART RTS
ftdi_cts output	FTDI UART CTS
qspi_dq inout[3: 0]	QUAD SPI
qspi_csn output	QUAD SPI
sd_reset output	SD CARD Reset
sd_cd input	SD CARD CD
sd_sck output	SD CARD sck
sd_cmd inout	SD CARD cmd
sd_dat inout[3: 0]	SD CARD dat

INSTANTIANTED MODULES

inst_util_mii_to_rmii

```
util_mii_to_rmii #(
                                                                                .
INTF_CFG(0),
                                                                                .
RATE_10_100(0)
) inst_util_mii_to_rmii ( .mac_tx_en(MII_tx_en), .mac_txd(MII_txd), .mac_t
```

convert from mii to rmii (UNTESTED)

inst_system_ps_wrapper

```
system_ps_wrapper inst_system_ps_wrapper (
```

```
`ifdef
_JTAG_IO
.
tck(tck),
.
tms(tms),
.
tdi(tdi),
.
tdo(tdo),
.
endif
.
DDR_addr(ddr2_addr),
.
DDR_ba(ddr2_ba),
.
DDR_cas_n(ddr2_cas_n),
.
DDR_ck_n(ddr2_ck_n),
.
DDR_ck_p(ddr2_ck_p),
.
DDR_cke(ddr2_cke),
.
DDR_cs_n(ddr2_cs_n),
.
DDR_dm(ddr2_dm),
.
DDR_dq(ddr2_dq),
.
DDR_dqs_n(ddr2_dqs_n),
.
DDR_dqs_p(ddr2_dqs_p),
.
DDR_odt(ddr2_odt),
.
DDR_ras_n(ddr2_ras_n),
.
DDR_we_n(ddr2_we_n),
.
IRQ(3'b000),
.
MDIO_mdc(eth_mdc),
.
MDIO_mdio_io(eth_mdio),
.
MII_col(MII_col),
.
MII_crs(MII_crs),
.
MII_rst_n(MII_rst_n),
.
MII_rx_clk(MII_rx_clk),
.
MII_rx_dv(MII_rx_dv),
.
MII_rx_er(MII_rx_er),
.
MII_rxd(MII_rxd),
.
MII_tx_clk(MII_tx_clk),
.
MII_tx_en(MII_tx_en),
.
MII_txd(MII_txd),
```

```
.
M_AXI_araddr(),
.
M_AXI_arprot(),
.
M_AXI_arready(1'b1),
.
M_AXI_arvalid(),
.
M_AXI_awaddr(),
.
M_AXI_awprot(),
.
M_AXI_awready(1'b1),
.
M_AXI_awvalid(),
.
M_AXI_bready(),
.
M_AXI_bresp(3'b000),
.
M_AXI_bvalid(2'b00),
.
M_AXI_rdata(32'h00000000),
.
M_AXI_rready(),
.
M_AXI_rresp(3'b000),
.
M_AXI_rvalid(1'b00),
.
M_AXI_wdata(),
.
M_AXI_wready(1'b1),
.
M_AXI_wstrb(),
.
M_AXI_wvalid(),
.
QSPI_0_io0_io(qspi_dq[0]),
.
QSPI_0_io1_io(qspi_dq[1]),
.
QSPI_0_io2_io(qspi_dq[2]),
.
QSPI_0_io3_io(qspi_dq[3]),
.
QSPI_0_ss_io(qspi_csn),
.
UART_rxd(ftdi_tx),
.
UART_txd(ftdi_rx),
.
gpio_io_i(slide_switches),
.
gpio_io_o(leds),
.
gpio_io_t(),
.
s_axi_clk(),
.
spi_io0_i(1'b0),
.
spi_io0_o(),
.
spi_io0_t(),
```

```
                                                                                .
 spi_io1_i(1'b0),                                                               .
 spi_io1_o(),                                                                   .
 spi_io1_t(),                                                                   .
 spi_sck_i(1'b0),                                                               .
 spi_sck_o(),                                                                   .
 spi_sck_t(),                                                                   .
 spi_ss_i(1'b0),                                                                .
 spi_ss_o(),                                                                    .
 spi_ss_t(),                                                                    .
 sys_clk(clk),                                                                  .
 sys_rstn(resetn),                                                              .
 vga_hsync(vga_hs),                                                             .
 vga_vsync(vga_vs),                                                             .
 vga_r(s_vga_r),                                                                .
 vga_g(s_vga_g),                                                                .
 vga_b(s_vga_b),                                                                .
 sd_resetn(s_sd_resetn),                                                        .
 sd_cd(sd_cd),                                                                  .
 sd_sck(sd_sck),                                                                .
 sd_cmd(sd_cmd),                                                                .
 sd_dat(sd_dat)
)
```

Wraps all of the RISCV CPU core and its devices.