system_wrapper.v

AUTHORS

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DATES

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INFORMATION

Brief

System wrapper for ps.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
ACLK_FREQ_MHZ
  =
50
)
                                                                        (
`ifdef _JTAG_IO input
tck,
input
tms,
input
tdi,
output
```

```
 tdo,
 `endif input
 clk,
 input
 resetn,
 inout
  [12:0]
 ddr2_addr,
 inout
  [ 2:0]
 ddr2_ba,
 inout
 ddr2_cas_n,
 inout
 ddr2_ck_n,
 inout
 ddr2_ck_p,
 inout
 ddr2_cke,
 inout
 ddr2_cs_n,
 inout
  [ 1:0]
 ddr2_dm,
 inout
  [15:0]
 ddr2_dq,
 inout
  [ 1:0]
 ddr2_dqs_n,
 inout
  [ 1:0]
 ddr2_dqs_p,
 inout
 ddr2_odt,
 inout
 ddr2_ras_n,
 inout
 ddr2_reset_n,
 inout
 ddr2_we_n,
 output
  [15:0]
 leds,
 input
  [15:0]
 slide_switches,
 input
 ftdi_tx,
 output
 ftdi_rx,
 input
 ftdi_rts,
 output
 ftdi_cts,
 input
 sd_spi_miso,
 output
 sd_spi_mosi,
 output
 sd_spi_csn,
 output
 sd_spi_sclk,
 output
 sd_reset
)
```

System wrapper for Vexriscv Veronica RISCV ps.

Ports

tck `ifdef _JTAG_IO input	JTAG
tms input`ifdef _JTAG_IO input	JTAG
tdi input`ifdef _JTAG_IO input	JTAG
tdo output`ifdef _JTAG_IO input	JTAG
clk output`endif input	Master Input Clock
resetn input`endif input	Master Reset Input
ddr2_addr inout [12:0]	DDR interface
ddr2_ba inout [2:0]	DDR interface
ddr2_cas_n inout [2:0]	DDR interface
ddr2_ck_n inout [2:0]	DDR interface
ddr2_ck_p inout [2:0]	DDR interface
ddr2_cke inout [2:0]	DDR interface
ddr2_cs_n inout [2:0]	DDR interface
ddr2_dm inout [1:0]	DDR interface
ddr2_dq inout [15:0]	DDR interface
ddr2_dqs_n inout [1:0]	DDR interface
ddr2_dqs_p inout [1:0]	DDR interface
ddr2_odt inout [1:0]	DDR interface
ddr2_ras_n inout [1:0]	DDR interface
ddr2_reset_n inout [1:0]	DDR interface
ddr2_we_n inout [1:0]	DDR interface
leds output [15:0]	board leds
slide_switches input [15:0]	board slide switches
ftdi_tx input [15:0]	FTDI UART TX
ftdi_rx	FTDI UART RX

output [15:0]

ftdi_rts input [15:0]	FTDI UART RTS
ftdi_cts output [15:0]	FTDI UART CTS
sd_spi_miso input [15:0]	SD CARD Master In Master Out SPI
sd_spi_mosi output [15:0]	SD CARD Master Out Master In SPI
sd_spi_csn output [15:0]	SD CARD Chip Select SPI
sd_spi_sclk output [15:0]	SD CARD clock SPI

inst_clk_wiz_1

Generate system clocks

inst_ddr_rstgen

Generate DDR Reset

inst_sys_rstgen

Generate general system resets

inst_cpu_rstgen

Generate general system resets

inst_axi_ddr_ctrl

AXI DDR Controller, 200 MHz in for 50 Mhz out (200/4 = 50).

inst_system_ps_wrapper

Wraps all of the RISCV CPU core and its devices.