

# system\_wrapper.v

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## AUTHORS

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## DATES

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## INFORMATION

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### Brief

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System wrapper for ps.

### License MIT

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## system\_wrapper

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```
module system_wrapper #(
  parameter
  ACLK_FREQ_MHZ
  =
  50
)
`ifdef _JTAG_IO input
tck,
input
tms,
input
tdi,
output
```

```
tdo,  
`endif input  
clk,  
input  
resetn,  
inout  
[12:0]  
ddr2_addr,  
inout  
[ 2:0]  
ddr2_ba,  
inout  
ddr2_cas_n,  
inout  
ddr2_ck_n,  
inout  
ddr2_ck_p,  
inout  
ddr2_cke,  
inout  
ddr2_cs_n,  
inout  
[ 1:0]  
ddr2_dm,  
inout  
[15:0]  
ddr2_dq,  
inout  
[ 1:0]  
ddr2_dqs_n,  
inout  
[ 1:0]  
ddr2_dqs_p,  
inout  
ddr2_odt,  
inout  
ddr2_ras_n,  
inout  
ddr2_reset_n,  
inout  
ddr2_we_n,  
output  
[15:0]  
leds,  
input  
[15:0]  
slide_switches,  
input  
ftdi_tx,  
output  
ftdi_rx,  
input  
ftdi_rts,  
output  
ftdi_cts,  
input  
sd_spi_miso,  
output  
sd_spi_mosi,  
output  
sd_spi_csn,  
output  
sd_spi_sclk,  
output  
sd_reset  
)
```

System wrapper for Vexriscv Veronica RISCv ps.

## Ports

<b>tck</b>	JTAG
<code>`ifdef _JTAG_IO input</code>	
<b>tms</b>	JTAG
<code>input`ifdef _JTAG_IO input</code>	
<b>tdi</b>	JTAG
<code>input`ifdef _JTAG_IO input</code>	
<b>tdo</b>	JTAG
<code>output`ifdef _JTAG_IO input</code>	
<b>clk</b>	Master Input Clock
<code>output`endif input</code>	
<b>resetrn</b>	Master Reset Input
<code>input`endif input</code>	
<b>ddr2_addr</b>	DDR interface
<code>inout [12:0]</code>	
<b>ddr2_ba</b>	DDR interface
<code>inout [2:0]</code>	
<b>ddr2_cas_n</b>	DDR interface
<code>inout [2:0]</code>	
<b>ddr2_ck_n</b>	DDR interface
<code>inout [2:0]</code>	
<b>ddr2_ck_p</b>	DDR interface
<code>inout [2:0]</code>	
<b>ddr2_cke</b>	DDR interface
<code>inout [2:0]</code>	
<b>ddr2_cs_n</b>	DDR interface
<code>inout [2:0]</code>	
<b>ddr2_dm</b>	DDR interface
<code>inout [1:0]</code>	
<b>ddr2_dq</b>	DDR interface
<code>inout [15:0]</code>	
<b>ddr2_dqs_n</b>	DDR interface
<code>inout [1:0]</code>	
<b>ddr2_dqs_p</b>	DDR interface
<code>inout [1:0]</code>	
<b>ddr2_odt</b>	DDR interface
<code>inout [1:0]</code>	
<b>ddr2_ras_n</b>	DDR interface
<code>inout [1:0]</code>	
<b>ddr2_reset_n</b>	DDR interface
<code>inout [1:0]</code>	
<b>ddr2_we_n</b>	DDR interface
<code>inout [1:0]</code>	
<b>leds</b>	board leds
<code>output [15:0]</code>	
<b>slide_switches</b>	board slide switches
<code>input [15:0]</code>	
<b>ftdi_tx</b>	FTDI UART TX
<code>input [15:0]</code>	
<b>ftdi_rx</b>	FTDI UART RX

output [15:0]	
<b>ftdi_rts</b>	FTDI UART RTS
input [15:0]	
<b>ftdi_cts</b>	FTDI UART CTS
output [15:0]	
<b>sd_spi_miso</b>	SD CARD Master In Master Out SPI
input [15:0]	
<b>sd_spi_mosi</b>	SD CARD Master Out Master In SPI
output [15:0]	
<b>sd_spi_csn</b>	SD CARD Chip Select SPI
output [15:0]	
<b>sd_spi_sclk</b>	SD CARD clock SPI
output [15:0]	

## inst\_clk\_wiz\_1

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Generate system clocks

## inst\_ddr\_rstgen

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Generate DDR Reset

## inst\_sys\_rstgen

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Generate general system resets

## inst\_cpu\_rstgen

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Generate general system resets

## inst\_axi\_ddr\_ctrl

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AXI DDR Controller, 200 MHz in for 50 Mhz out ( $200/4 = 50$ ).

## inst\_system\_ps\_wrapper

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Wraps all of the RISCv CPU core and its devices.