VERONICA_RISCV

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Contents

1 Usage **2**
1.1 Introduction 2
1.2 Dependencies 2
1.2.1 fusesoc_info Depenecies 2

2 Architecture **4**

3 Building **4**
3.1 fusesoc 4
3.2 Source Files 4
3.2.1 fusesoc_info File List 4
3.3 Targets 6
3.3.1 fusesoc_info Targets 6
3.4 Directory Guide 9

4 Simulation **10**

5 Module Documentation **11**
5.1 nexys a7 100t system wrapper 12

1 Usage

1.1 Introduction

The Veronica RISCV is a base Vexriscv system. This version of the Vexriscv core emulates the E31 core in its mapping of features. Difference is that this core can generate a MMU and non-PMP enabled versions. The JTAG configuration can also be changed between the Xilinx BSCANE, or JTAG IO for external devices, or none. Each target tries to use all of the resources of the board using free IP's from the vendor, or open source IP cores intergrated into fusesoc.

1.2 Dependencies

The following are the dependencies of the cores.

- fusesoc 2.X
- iverilog (simulation)
- cocotb (simulation)

1.2.1 fusesoc_info Depenecies

- tb_cocotb
  - ::jtag_vpi:0-r5
- nexys-a7-100t
  - AFRL:utility:digilent_nexys-a7-100t_board_base_constr:1.0.0
  - AFRL:utility:digilent_nexys-a7-100t_board_base_ddr_cfg:1.0.0
  - AFRL:utility:vivado_board_support_packages
- nexys-a7-100t_bootgen
  - AFRL:utility:digilent_veronica_nexys_boot_gen:1.0.0
- genesys2
  - AFRL:utility:digilent_genesys2_board_base_constr:1.0.0
  - AFRL:utility:digilent_genesys2_board_base_ddr_cfg:1.0.0
  - AFRL:utility:vivado_board_support_packages
- NetFPGA-1G-CML
  - AFRL:utility:digilent_NetFPGA-1G-CML_board_base_constr:1.0.0
  - AFRL:utility:digilent_NetFPGA-1G-CML_board_base_ddr_cfg:1.0.0

    - AFRL:utility:vivado_board_support_packages
- KC705
    - AFRL:utility:xilinx_kc705_board_base_constr:1.0.0
    - AFRL:utility:xilinx_kc705_board_base_ddr_cfg:1.0.0
    - AFRL:utility:vivado_board_support_packages
- VC707
    - AFRL:utility:xilinx_vc707_board_base_constr:1.0.0
    - AFRL:utility:xilinx_vc707_board_base_ddr_cfg:1.0.0
    - AFRL:utility:vivado_board_support_packages
- crosslink-nx_eval
    - AFRL:utility:lattice_crosslink-nx_eval_board_base:1.0.0
- dep
    - AFRL:utility:helper:1.0.0
    - AFRL:utility:tcl_helper_check:1.0.0
    - AFRL:device:axi_lite_spi_master:1.0.0
    - AFRL:device:axi_lite_uart_lite:1.0.0
    - AFRL:device:axi_lite_gpio:1.0.0
    - zipcpu:axi_lite:crossbar:1.0.0
- dep_jtag_io
    - spinalhdl:cpu:veronica_jtag_io:1.0.0
- dep_secure_jtag_io
    - spinalhdl:cpu:veronica_secure_jtag_io:1.0.0
- dep_linux_jtag_io
    - spinalhdl:cpu:veronica_linux_jtag_io:1.0.0
- dep_jtag_bscane
    - spinalhdl:cpu:veronica_jtag_xilinx_bscane:1.0.0
- dep_secure_jtag_bscane
    - spinalhdl:cpu:veronica_secure_jtag_xilinx_bscane:1.0.0
- dep_linux_jtag_bscane
    - spinalhdl:cpu:veronica_linux_jtag_xilinx_bscane:1.0.0

2 Architecture

The project contains four wrappers

- **system_wrapper** Contains the top level project module and contains system_ps_wrapper.
- **system_ps_wrapper** Contains the processor system IP wrappers.

Please see 5 for more information per target.

3 Building

The all Veronica RISCV project source files are written in Verilog 2001. They should synthesize in any modern FPGA software. The core comes as a fusesoc packaged core and can be included in any other core. Be sure to make sure you have meet the dependencies listed in the previous section.

3.1 fusesoc

Fusesoc is a system for building FPGA software without relying on the internal project management of the tool. Avoiding vendor lock in to Vivado or Quartus. These cores, when included in a project, can be easily integrated and targets created based upon the end developer needs. The core by itself is not a part of a system and should be integrated into a fusesoc based system. Simulations are setup to use fusesoc and are a part of its targets.

3.2 Source Files

3.2.1 fusesoc_info File List

- tb_cocotb
  - 'tb/tb_cocotb.py': 'file_type': 'user', 'copyto': '.'
  - 'tb/tb_cocotb.v': 'file_type': 'verilogSource'
  - 'tb/export_fix.sh': 'file_type': 'user', 'copyto': '.'
- common
  - 'common/system_ps_axi_perf_wrapper.v': 'file_type': 'verilogSource'
- nexys-a7-100t

  - 'nexys-a7-100t/system_wrapper.v': 'file_type': 'verilogSource'
  - 'nexys-a7-100t/system_constr.tcl': 'file_type': 'SDC'
  - 'nexys-a7-100t/system_gen_ps.tcl': 'file_type': 'tclSource'
  - 'nexys-a7-100t/system_gen.tcl': 'file_type': 'tclSource'
- genesys2
  - 'genesys2/system_wrapper.v': 'file_type': 'verilogSource'
  - 'genesys2/system_constr.tcl': 'file_type': 'SDC'
  - 'genesys2/system_gen_ps.tcl': 'file_type': 'tclSource'
  - 'genesys2/system_gen.tcl': 'file_type': 'tclSource'
- NetFPGA-1G-CML
  - 'NetFPGA-1G-CML/system_wrapper.v': 'file_type': 'verilog-Source'
  - 'NetFPGA-1G-CML/system_constr.tcl': 'file_type': 'SDC'
  - 'NetFPGA-1G-CML/system_gen_ps.tcl': 'file_type': 'tclSource'
  - 'NetFPGA-1G-CML/system_gen.tcl': 'file_type': 'tclSource'
- KC705
  - 'KC705/system_wrapper.v': 'file_type': 'verilogSource'
  - 'KC705/system_constr.tcl': 'file_type': 'SDC'
  - 'KC705/system_gen_ps.tcl': 'file_type': 'tclSource'
  - 'KC705/system_gen.tcl': 'file_type': 'tclSource'
- VC707
  - 'VC707/system_wrapper.v': 'file_type': 'verilogSource'
  - 'VC707/system_constr.tcl': 'file_type': 'SDC'
  - 'VC707/system_gen_ps.tcl': 'file_type': 'tclSource'
  - 'VC707/system_gen.tcl': 'file_type': 'tclSource'
- crosslink-nx_eval
  - 'crosslink-nx_eval/system_constr.pdc': 'file_type': 'PDC'
  - 'crosslink-nx_eval/system_wrapper.v': 'file_type': 'verilogSource'
- dep_vivado_jtag_io
  - 'common/xilinx/system_define.tcl': 'file_type': 'tclSource'
- dep_jtag_io
  - 'common/system_ps_wrapper_jtag.v': 'file_type': 'verilogSource'

- dep_secure_jtag_io
  - 'common/system_ps_wrapper_jtag.v': 'file_type': 'verilogSource'
- dep_linux_jtag_io
  - 'common/system_ps_wrapper_jtag.v': 'file_type': 'verilogSource'
- dep_jtag_bscane
  - 'common/system_ps_wrapper.v': 'file_type': 'verilogSource'
- dep_secure_jtag_bscane
  - 'common/system_ps_wrapper.v': 'file_type': 'verilogSource'
- dep_linux_jtag_bscane
  - 'common/system_ps_wrapper.v': 'file_type': 'verilogSource'

3.3 Targets

3.3.1 fusesoc_info Targets

- nexys-a7-100t

  Info: Base for nexys-a7-100t digilent development board builds, do not use.

- nexys-a7-100t_secure_jtag_io

  Info: Build for nexys-a7-100t digilent development board with PMP enabled Veronica RISCV.

- nexys-a7-100t_jtag_io

  Info: Build for nexys-a7-100t digilent development board with standard Veronica RISCV.

- nexys-a7-100t_secure_jtag_bscane

  Info: Build for nexys-a7-100t digilent development board with PMP enabled Veronica RISCV.

- nexys-a7-100t_jtag_bscane

  Info: Build for nexys-a7-100t digilent development board with standard Veronica RISCV.

- nexys-a7-100t_linux_jtag_bscane

  Info: Build for nexys-a7-100t digilent development board with Linux Veronica RISCV.

- nexys-a7-100t_linux_jtag_bscane_bootgen

  Info: Build for nexys-a7-100t digilent development board with Linux Veronica RISCV with bootgen for uboot.

- genesys2

  Info: Base for genesys2 digilent development board builds, do not use.

- genesys2_secure_jtag_io

  Info: Build for genesys2 digilent development board with PMP enabled Veronica RISCV.

- genesys2_jtag_io

  Info: Build for genesys2 digilent development board with standard Veronica RISCV.

- genesys2_secure_jtag_bscane

  Info: Build for genesys2 digilent development board with PMP enabled Veronica RISCV.

- genesys2_jtag_bscane

  Info: Build for genesys2 digilent development board with standard Veronica RISCV.

- genesys2_linux_jtag_bscane

  Info: Build for genesys2 digilent development board with Linux Veronica RISCV.

- NetFPGA-1G-CML

  Info: Base for NetFPGA-1G-CML digilent development board builds, do not use.

- NetFPGA-1G-CML_secure_jtag_io

  Info: Build for NetFPGA-1G-CML digilent development board with PMP enabled Veronica RISCV.

- NetFPGA-1G-CML_jtag_io

  Info: Build for NetFPGA-1G-CML digilent development board with standard Veronica RISCV.

- NetFPGA-1G-CML_secure_jtag_bscane

  Info: Build for NetFPGA-1G-CML digilent development board with PMP enabled Veronica RISCV.

- NetFPGA-1G-CML_jtag_bscane

  Info: Build for NetFPGA-1G-CML digilent development board with standard Veronica RISCV.

- NetFPGA-1G-CML_linux_jtag_bscane

  Info: Build for NetFPGA-1G-CML digilent development board with Linux Veronica RISCV.

- kc705

  Info: Base for kc705 xilinx development board builds, do not use.

- kc705_secure_jtag_bscane

  Info: Build for kc705 xilinx development board with PMP enabled Veronica RISCV.

- kc705_jtag_bscane

  Info: Build for kc705 xilinx development board with standard Veronica RISCV.

- kc705_linux_jtag_bscane

  Info: Build for kc705 xilinx development board with Linux Veronica RISCV.

- vc707

  Info: Base for VC707 xilinx development board builds, do not use.

- vc707_secure_jtag_bscane

  Info: Build for vc707 xilinx development board with PMP enabled Veronica RISCV.

- vc707_jtag_bscane

  Info: Build for vc707 xilinx development board with standard Veronica RISCV.

- vc707_linux_jtag_bscane

  Info: Build for vc707 xilinx development board with Linux Veronica RISCV.

- crosslink-nx_eval

  Info: Defaults for CrossLink NX Evaluation Board, do not use.

- crosslink-nx_eval_jtag_io

  Info: Build for crosslink-nx_eval development board with standard Veronica RISCV.

- crosslink-nx_eval_secure_jtag_io

  Info: Build for crosslink-nx_eval development board with secure Veronica RISCV.

- crosslink-nx_eval_linux_jtag_io

  Info: Build for crosslink-nx_eval development board with Linux Veronica RISCV.

- sim_cocotb

  Info: Cocotb unit tests

3.4 Directory Guide

Below highlights important folders from the root of the directory.

1. **docs** Contains all documentation related to this project.
   - **manual** Contains user manual and github page that are generated from the latex sources.
2. **nexys-a7-100t** Contains source files for nexys-a7-100t
3. **crosslink-nx_eval** Contains source file for crosslink-nx_eval, a future target.

4 Simulation

There is no simulation at the moment. Maybe a future addition?

5 Module Documentation

There project has multiple modules. The targets are the top system wrappers.

- **nexys-a7-100t**
- **crosslink-nx_eval**

The next sections document the module in great detail.

system_wrapper.v

AUTHORS

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DATES

2024/11/25

INFORMATION

Brief

System wrapper for ps.

License MIT

system_wrapper

```
module system_wrapper #(
parameter
ACLK_FREQ_MHZ
 =
50
)
                                                                        (
`ifdef _JTAG_IO input
tck,
input
tms,
input
tdi,
output
```

```
 tdo,
 `endif input
 clk,
 input
 resetn,
 inout
  [12:0]
 ddr2_addr,
 inout
  [ 2:0]
 ddr2_ba,
 inout
 ddr2_cas_n,
 inout
 ddr2_ck_n,
 inout
 ddr2_ck_p,
 inout
 ddr2_cke,
 inout
 ddr2_cs_n,
 inout
  [ 1:0]
 ddr2_dm,
 inout
  [15:0]
 ddr2_dq,
 inout
  [ 1:0]
 ddr2_dqs_n,
 inout
  [ 1:0]
 ddr2_dqs_p,
 inout
 ddr2_odt,
 inout
 ddr2_ras_n,
 inout
 ddr2_reset_n,
 inout
 ddr2_we_n,
 output
  [15:0]
 leds,
 input
  [15:0]
 slide_switches,
 input
 ftdi_tx,
 output
 ftdi_rx,
 input
 ftdi_rts,
 output
 ftdi_cts,
 input
 sd_spi_miso,
 output
 sd_spi_mosi,
 output
 sd_spi_csn,
 output
 sd_spi_sclk,
 output
 sd_reset
)
```

System wrapper for Vexriscv Veronica RISCV ps.

Ports

tck `ifdef _JTAG_IO input	JTAG
tms input`ifdef _JTAG_IO input	JTAG
tdi input`ifdef _JTAG_IO input	JTAG
tdo output`ifdef _JTAG_IO input	JTAG
clk output`endif input	Master Input Clock
resetn input`endif input	Master Reset Input
ddr2_addr inout [12:0]	DDR interface
ddr2_ba inout [2:0]	DDR interface
ddr2_cas_n inout [2:0]	DDR interface
ddr2_ck_n inout [2:0]	DDR interface
ddr2_ck_p inout [2:0]	DDR interface
ddr2_cke inout [2:0]	DDR interface
ddr2_cs_n inout [2:0]	DDR interface
ddr2_dm inout [1:0]	DDR interface
ddr2_dq inout [15:0]	DDR interface
ddr2_dqs_n inout [1:0]	DDR interface
ddr2_dqs_p inout [1:0]	DDR interface
ddr2_odt inout [1:0]	DDR interface
ddr2_ras_n inout [1:0]	DDR interface
ddr2_reset_n inout [1:0]	DDR interface
ddr2_we_n inout [1:0]	DDR interface
leds output [15:0]	board leds
slide_switches input [15:0]	board slide switches
ftdi_tx input [15:0]	FTDI UART TX
ftdi_rx	FTDI UART RX

output [15:0]

ftdi_rts input [15:0]	FTDI UART RTS
ftdi_cts output [15:0]	FTDI UART CTS
sd_spi_miso input [15:0]	SD CARD Master In Master Out SPI
sd_spi_mosi output [15:0]	SD CARD Master Out Master In SPI
sd_spi_csn output [15:0]	SD CARD Chip Select SPI
sd_spi_sclk output [15:0]	SD CARD clock SPI

inst_clk_wiz_1

Generate system clocks

inst_ddr_rstgen

Generate DDR Reset

inst_sys_rstgen

Generate general system resets

inst_cpu_rstgen

Generate general system resets

inst_axi_ddr_ctrl

AXI DDR Controller, 200 MHz in for 50 Mhz out (200/4 = 50).

inst_system_ps_wrapper

Wraps all of the RISCV CPU core and its devices.