Q1: Do the following addition and subtraction by hand:

\$76 + \$3A

If these numbers are unsigned numbers,

If these numbers are signed numbers,

overflow: yes

overflow: yes no

=\$B0

\$A3-\$6C

If these numbers are unsigned numbers,

If these numbers are signed numbers,

overflow: yes

=\$37

Q2: Do your results calculated by hand in Q1 match the simulation results? Yes

overflow: yes no

No

Q3: Do the following addition and subtraction by hand:

\$F3 + \$C9

If these numbers are unsigned numbers, **overflow**:

If these numbers are signed numbers,

no overflow: yes no

=\$BC

\$4B-\$8D

If these numbers are unsigned numbers, overflow:

If these numbers are signed numbers,

no

overflow: yes no

=\$BE

Q4: Do your results calculated by hand in Q3 match the simulation results with the new data?

Yes

No

Using **F11** key, execute the instructions one at a time and fill the values of **N**, **Z**, **V**, and **C** bits in Condition Coder Register (CCR).

Code Line	Memory	Machine	Assembly	N	Z	٧	С
	Address	Codes	Code				
1:	\$4100	В6	LDAA 3000h	1	0	0	0
	\$4101	30					
	\$4102	00					
2:	\$4103	F6	LDAB 3001h	1	0	0	0
	\$4104	30					
	\$4105	01					
3:	\$4106	18	ABA	1	0	0	1
	\$4107	06					
4:	\$4108	7A	STAA 3002h	1	0	0	1
	\$4109	30					
	\$410A	02					
5:	\$410B	В6	LDAA 3003h	0	0	0	1
	\$410C	30					
	\$410D	03					
6:	\$410E	F6	LDAB 3004h	1	0	0	1
	\$410F	30					
	\$4110	04					
7:	\$4111	18	SBA	1	0	1	1
	\$4112	16					
	\$4113	7A	STAA 3005h	1	0	0	1
	\$4114	30					
	\$4115	05					
6:	\$4116	20	BRA endmain	1	0	0	1
	\$4117	FE					

Figure 9.