DHBW Mannheim Product specification

5-bit binary-to-BCD converter

DHM185, DHM185X, DHM185G

GENERAL DESCRIPTION

This monolithic converter is derived from the 27C16 or 27C32 read-only memory (DHM185), from the ATtiny26 microcontroller (DHM185X), or from GAL16V8D (DHM185G). It demonstrates the versatility of a readonly memory in that an unlimited number of reference tables or conversion tables may be built into a system using economical, customized read-only memories. This converter does not make advantage of the fact that the least significant bits (LSB) of the binary and BCD codes are logically equal, and does therefore not require bypass of the LSB. Instead, the converter has a true 5-bit input in each case. The device is therefore not easily cascadable to N bits. The behavior of this device is similar to that of the 74185, but because of the different LSB passthrough handling both ICs are not compatible.

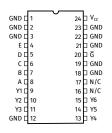
An overriding enable input is provided on the DHM185 and DHM185X converter which, when taken high, inhibits the function, causing all outputs to go into high impedance mode. On the DHM185G the outputs are always enabled.

The DHM185 family devices are characterized for operation over the temperature range of 0°C to 70°C.

The function performed by this 5-bit binary-to-BCD converter is analogous to the algorithm:

- a. Divide the binary input by 10, discarding the residue. Output the value on the MSD outputs Y5, Y6.
- b. Take the binary input modulo 10 and output the value on the LSD outputs Y1, Y2, Y3, Y4.

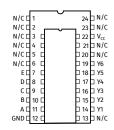
DHM185 DIP24 package (TOP VIEW)

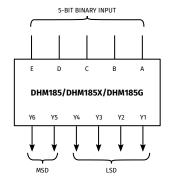


DHM185X DIP20 package (TOP VIEW)



DHM185G DIP20/24 package (TOP VIEW)





ORDERING INFORMATION

TYPE NUMBER	PACKAGE							
	NAME	DESCRIPTION	VERSION					
DHM185	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1					
DHM185X	DIP20	plastic dual in-line package; 20 leads (400 mil)	SOT146-4					
DHM185G	DIP20/24	plastic dual in-line package; 24 leads (600 mil) with 20 lead piggy-backed GAL	SOT101-1					

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FUNCTION TABLE

	INPUTS					OUTPUTS						
BINARY VALUE	BINARY SELECT				ENABLE							
VALUE	E	D	С	В	A	G	Y6	Y5	Y4	Y3	Y2	Y1
0	L	L	L	L	L	L	L	L	L	L	L	L
1	L	L	L	L	Н	L	L	L	L	L	L	Н
2	L	L	L	Н	L	L	L	L	L	L	Н	L
3	L	L	L	Н	Н	L	L	L	L	L	Н	Н
4	L	L	Н	L	L	L	L	L	L	Н	L	L
5	L	L	Н	L	Н	L	L	L	L	Н	L	Н
6	L	L	Н	Н	L	L	L	L	L	Н	Н	L
7	L	L	Н	Н	Н	L	L	L	L	Н	Н	Н
8	L	Н	L	L	L	L	L	L	Н	L	L	L
9	L	Н	L	L	Н	L	L	L	Н	L	L	Н
10	L	Н	L	Н	L	L	L	Н	L	L	L	L
11	L	Н	L	Н	Н	L	L	Н	L	L	L	Н
12	L	Н	Н	L	L	L	L	Н	L	L	Н	L
13	L	Н	Н	L	Н	L	L	Н	L	L	Н	Н
14	L	Н	Н	Н	L	L	L	Н	L	Н	L	L
15	L	Н	Н	Н	Н	L	L	Н	L	Н	L	Н
16	Н	L	L	L	L	L	L	Н	L	Н	Н	L
17	Н	L	L	L	Н	L	L	Н	L	Н	Н	Н
18	Н	L	L	Н	L	L	L	Н	Н	L	L	L
19	Н	L	L	Н	Н	L	L	Н	Н	L	L	Н
20	Н	L	Н	L	L	L	Н	L	L	L	L	L
21	Н	L	Н	L	Н	L	Н	L	L	L	L	Н
22	Н	L	Н	Н	L	L	Н	L	L	L	Н	L
23	Н	L	Н	Н	Н	L	Н	L	L	L	Н	Н
24	Н	Н	L	L	L	L	Н	L	L	Н	L	L
25	Н	Н	L	L	Н	L	Н	L	L	Н	L	Н
26	Н	Н	L	Н	L	L	Н	L	L	Н	Н	L
27	Н	Н	L	Н	Н	L	Н	L	L	Н	Н	Н
28	Н	Н	Н	L	L	L	Н	L	Н	L	L	L
29	Н	Н	Н	L	Н	L	Н	L	Н	L	L	Н
30	Н	Н	Н	Н	L	L	Н	Н	L	L	L	L
31	Н	Н	Н	Н	Н	L	Н	Н	L	L	L	Н
ALL	Х	Χ	Χ	Χ	Χ	Н	Z	Z	Z	Z	Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

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