

IBM z16 Technical Introduction

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IBM Z



IBM Redbooks

IBM z16 Technical Introduction

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Note: Before using this information and the product it supports, read the information in “Notices” on page v.

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Preface

This IBM® Redbooks® publication introduces the latest member of the IBM Z® platform that is built with the IBM Telum processor: the IBM z16 server.

The IBM Z platform is recognized for its security, resiliency, performance, and scale. It is relied on for mission-critical workloads and as an essential element of hybrid cloud infrastructures. The IBM z16 server adds capabilities and value with innovative technologies that are needed to accelerate the digital transformation journey.

This book explains how the IBM z16 server uses innovations and traditional IBM Z strengths to satisfy the growing demand for cloud, analytics, and a more flexible infrastructure. With the IBM z16 servers as the base, applications can run in a trusted, reliable, and secure environment that improves operations and lessens business risk.

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Enduring the pace of digital transformation with the IBM z16 server

For several years, digital transformation has been changing the way companies run and affecting every part of their business from the infrastructure to processes, workflows, and even their culture. The ongoing pandemic accelerated the rate and pace of the digital transformation journey, which caused most companies to find novel ways to sustain operations while unlocking new opportunities and increasing innovation.

Open industry standard tools and agile DevOps methodologies are key to any successful digital transformation strategy and to accelerate modernization. An integrated platform that supports cloud-native development and infrastructure automation is essential.

To move the business forward while continuing to maintain the necessary levels of resiliency, compliance, and sustainability, a secure infrastructure with more flexibility and agility is needed. The latest member of the IBM Z family, the IBM z16 server, can help with these new demands through *accelerated AI*, *cyberresiliency*, and a *modernized hybrid cloud*.

In this chapter, you learn about the IBM z16 capabilities and the business value that it can provide.

This chapter describes the following topics:

- ▶ 1.1, “The platform for the digital transformation journey” on page 2
- ▶ 1.2, “IBM z16 technical overview” on page 5
- ▶ 1.3, “IBM z16 software support” on page 11

1.1 The platform for the digital transformation journey

More than any other platform, the IBM z16 server offers a high-value architecture that can satisfy the growing demands that are driven by the pace of digital transformation, such as:

- ▶ More compute power for increased throughput
- ▶ Special hardware co-processors and accelerators to enhance performance
- ▶ Large-scale memory to process data faster
- ▶ Industry-unique cache design to optimize performance
- ▶ Accelerated I/O bandwidth to process massive amounts of data
- ▶ Quantum-safe cryptography to protect sensitive data now and in the future
- ▶ Flexible, on-premises hardware consumption pricing to handle the impact of unpredictable high spikes on business-critical workloads in a cost-effective manner
- ▶ Instant recovery:
 - Reduce the duration that is needed to start or shut down an OS or services.
 - Recover faster from system events.
 - Tailored short-duration boosts to mitigate the impact of IBM SAN Volume Controller memory dumps, middleware restarts, and IBM HyperSwap® recovery processes
- ▶ Ability to dynamically shift production capacity across sites

The IBM Z platform is recognized for its security, resiliency, performance, and scale, and it is relied on for mission-critical workloads and as an essential element of hybrid cloud infrastructures. The IBM z16 server adds more capabilities and value with innovative technologies that are needed to accelerate the digital transformation journey.

The IBM z16 server is the first IBM Z platform that is built with the *IBM Telum processor*.¹ It is designed to help businesses:

- ▶ Create value in every interaction and optimize decision making with the on-chip Accelerator for Artificial Intelligence (AI). The Accelerator for AI can deliver the speed and scale that is required to infuse AI inferencing into workloads with no impact on service delivery.
- ▶ Act now to protect today's data against current and future threats with quantum-safe protection through quantum-safe cryptography APIs and crypto-discovery tools.
- ▶ Enhance resiliency with flexible capacity to dynamically shift system resources across locations to proactively avoid disruptions.
- ▶ Modernize and integrate applications and data in a hybrid cloud environment with consistent and flexible deployment options to innovate with speed and agility.
- ▶ Reduce cost and keep up with changing regulations through a solution that helps simplify and streamline compliance tasks.

¹ [IBM Telum Processor: the next-gen microprocessor for IBM Z and IBM LinuxONE](#)

Figure 1-1 shows the available IBM z16 A01 configuration options (one to four 19-inch frames).



Figure 1-1 IBM z16 19-inch frame configurations

The IBM z16 server is built with the on-chip Accelerator for AI that enables decision velocity while its quantum-safe technologies protect your sensitive data now and into the future. It provides a flexible infrastructure to meet the resiliency and compliance demands of a constantly changing environment with capabilities to accelerate modernization and delivery of new services.

Predicting and automating with accelerated AI

An approach where data gravity and transaction gravity intersect, that co-collocates data, transactional systems, and AI inferencing, can deliver insights at speed and scale to enable decision velocity. Decision velocity means delivering insights faster to make decisions to help identify new business opportunities improve customer experience, and reduce operational risk.

Consider the following points:

- ▶ The on-chip Integrated Accelerator for AI is designed for high-speed, real-time inferencing at scale. It is designed to add more than six TFLOPS of processing power shared by all cores on the chip. This centralized AI design is intended to provide extremely high performance and consistent low-latency inferencing for processing a mix of transactional and AI workloads at speed and scale.

Now, complex neural network inferencing that uses real-time data can be run and delivers insights within high throughput enterprise workloads in real time while still meeting stringent SLAs.

- ▶ A robust ecosystem of frameworks and open source tools, combined with the IBM Deep Learning Compiler that generates inferencing programs that are highly optimized for the IBM Z architecture and the Integrated Accelerator for AI, help enable rapid development and deployment of deep learning and machine learning models on IBM Z to accelerate time to market.

Secure with a cyber-resilient system

With the opportunity that is created by quantum computing comes the threat to today's public key cryptography. Businesses must start now to prepare for the time when a quantum computer can break today's cryptography. In fact, today's data is at risk for future exposure through "harvest now, decrypt later" attacks.

IBM z16 is the industry-first quantum-safe system, which is protected by quantum-safe technology across multiple layers of firmware. Quantum-safe secure boot technology helps protect IBM z16 firmware from quantum attacks through a built-in dual signature scheme with no configuration changes that are required for enablement.

With the new Crypto Express8S, IBM z16 helps deliver quantum-safe APIs that position businesses to begin the use of quantum-safe cryptography along with classical cryptography as they begin modernizing applications and building new applications.

Discovering where and what kind of cryptography is being used is a key first step along the journey to quantum-safety. IBM z16 provides instrumentation that can be used to track cryptographic instruction execution in the CP Assist for Cryptographic Functions (CPACF).

Additionally, IBM Application Discovery and Delivery Intelligence (ADDI) was enhanced with new crypto discovery capabilities.

To move the enterprises forward in a world that is constantly changing, businesses require an infrastructure that is flexible, secure, and resilient. The risk and potential disruption from extreme weather events, cyberattacks, and more continues to increase. An ever-changing and complex regulatory environment is also driving up the cost to maintain and keep up with regulations.

Consider the following points:

- ▶ IBM z16 enhancements in resiliency include a new capability that is called *IBM Z Flexible Capacity for Cyber Resiliency*. With Flexible Capacity for Cyber Resiliency, you can remotely shift capacity and production workloads between IBM z16 systems at different sites on-demand and stay at the alternative site for up to one year. This capability can help demonstrate compliance with regulations that require organizations to dynamically shift production to an alternative site and remain there for an extended period. This capability is also designed to help you proactively avoid disruptions from unplanned events, and from planned scenarios, such as site facility maintenance.
- ▶ System Recovery Boost enhancements are also available with IBM z16. The enhancements can provide boosted processor capacity and parallelism for specific events. Client-selected middleware starts and restarts can be boosted to expedite recovery for middleware regions and restore steady-state operations as soon as possible. IBM SAN Volume Controller memory dump processing and HyperSwap configuration load and reload can be boosted to minimize the impact on running workloads.
- ▶ Parallel Sysplex enhancements include improved Integrated Coupling Adapter Short Reach (ICA SR) performance and Coupling Facility (CF) image scalability, technology, and protocol upgrades for coupling links, simplified Dynamic CF Dispatching (DYNDISP) support, and resiliency enhancements for CF cache and lock structures.

- ▶ IBM Z Security and Compliance Center is designed to help simplify and streamline compliance tasks. This solution provides a centralized, interactive dashboard for a consolidated view of compliance posture and system-generated evidence in near real time. You can now check the regulatory posture of your systems on-demand and more easily identify drift so that it can be remedied quickly.

Modernize for hybrid cloud

IBM z16 delivers technology innovation in AI, security, and resiliency on a flexible infrastructure that is designed for mission-critical workloads in a hybrid cloud environment. IBM z16 continues to deliver new and improved cloud capabilities on the platform.

IBM z16 provides the foundation for application modernization and hybrid cloud velocity by delivering leading hybrid cloud infrastructure to support the optimization of mission-critical applications and data.

IBM z16 and the accompanying IBM Z and cloud software, which is developed to support a cloud-native experience, delivers a broad set of open and industry-standard tools, including an agile DevOps methodology to accelerate modernization. These capabilities deliver speed to market and agility for development and operational teams as IBM z16 integrates as a critical component of hybrid cloud.

Businesses can accelerate modernization and delivery of new services by using the following key software offerings along with IBM z16:

- ▶ IBM Z and Cloud Modernization Stack to help empower developers to modernize and integrate z/OS applications with services across the hybrid cloud. This solution provides a flexible and integrated platform to support z/OS-based cloud-native development, application, and data modernization and infrastructure automation.
- ▶ Red Hat OpenShift and IBM Cloud Paks running on IBM z16 infrastructure provide the combination of infrastructure, hybrid cloud container platform, and middleware to modernize applications and develop cloud-native applications that integrate, extend, and supply data and workloads from IBM z16 across the hybrid cloud with Red Hat OpenShift.

1.2 IBM z16 technical overview

The IBM z16 is built with a 19-inch format that scales 1 - 4 frames, depending on the configuration. The 19-inch frames support American Society of Heating, Refrigerating, and Air-Conditioning Engineers (ASHRAE) Class A3 data centers.

The IBM z16 ensures continuity and upgradeability from the IBM z15™ and IBM z14. It has five orderable features: Max39, Max82, Max125, Max168, and Max200. The feature names are based on the maximum number of characterizable processor units (PUs) that use the IBM Telum processor chip design.

Table 1-1 lists some of the IBM z16 A01 technical capabilities.

Table 1-1 Technical highlights of the IBM z16

Greater total system capacity and more subcapacity settings for CPUs. The IBM z/Architecture® ensures continuity and upgradeability from previous models.	Up to 200 characterizable PUs. Up to 39 subcapacity settings for CPUs. Up to 317 total capacity levels.
Dual-chip modules (DCMs) using the IBM Telum processor to help improve the execution of processor-intensive workloads.	5.2 GHz (using 7 nm technology)
Memory per system, which ensures high availability (HA) in the memory subsystem by using proven redundant array of independent memory (RAIM) technology.	Up to 40 TB of addressable real memory per system.
A large fixed hardware system area (HSA) that is managed separately from ordered memory.	256 GB
Processor cache structure improvements and larger cache sizes to help with more demanding production workloads. The result is 1.5x cache capacity per core compared to IBM z15, at reduced average access latency, by way of a flatter system topology and overall improved system performance and scalability.	<ul style="list-style-type: none"> ▶ First-level cache (L1): 128 KB ▶ Second-level cache (L2): 32 MB ▶ Third-level cache (L3): 256 MB ▶ Fourth-level cache (L4): 2048 MB
The channel subsystem (CSS) is built for I/O resilience. The number of logical channel subsystems (LCSSs), subchannel sets, and I/O devices are consistent with its predecessor platform, as is the number of logical partitions (LPARs).	<ul style="list-style-type: none"> ▶ Six LCSS ▶ 85 LPAR ▶ Four subchannel sets ▶ 64,000 I/O devices per subchannel set
Proven technology (sixth-generation high frequency and fourth-generation out-of-order design) with a single-instruction, multiple-data (SIMD) processor that increases parallelism to accelerate analytics processing. In addition, simultaneous multithreading (SMT) increases processing efficiency and throughput and raises the number of instructions in flight. Special coprocessors and new hardware instructions for accelerating selected workloads.	
IBM Virtual Flash Memory (VFM) can be used to handle paging workload spikes and improve availability.	
The IBM Z Sort accelerator helps reduce CPU costs, speed up the sorting process, and improve database functions.	
Improved cryptographic functions and performance, which is achieved by having one dedicated cryptographic coprocessor per processor unit.	
Enhanced ICA-SR coupling link protocol provides up to 10% improvement for read and lock requests, and up to 25% for write requests and duplexed write requests compared to CF service times on IBM z15 systems.	
Improved CF processor scalability for CF images. The relative scaling of a CF image beyond a 9-way is significantly improved, meaning that the effective capacity of IBM z16 CF images continue to increase all the way up to the max of 16 processors in a CF image.	
New dedicated on-chip AI accelerator is designed for high-speed, real-time inferencing at scale.	
Improved data compression operations are achieved by having one dedicated compression coprocessor per processor unit, and new hardware instructions.	

For more information about the IBM z16, see Chapter 2, “IBM z16 hardware overview” on page 13, and Chapter 4, “IBM z16 system design strengths” on page 45.

1.2.1 Storage connectivity

Storage connectivity is provided on the IBM z16 by FICON Express and the IBM zHyperLink Express features.

FICON Express

FICON Express features follow the established Fibre Channel (FC) standards to support data storage and access requirements, along with the latest FC technology in storage and access devices.

FICON Express features support the following protocols:

- ▶ FICON
This enhanced protocol (as compared to FC) provides for communication across channels, channel to channel (CTC) connectivity, and with FICON devices, such as disks, tapes, and printers. It is used in z/OS, z/VM®, z/VSE® (Virtual Storage Extended), z/TPF (Transaction Processing Facility), and Linux on IBM Z environments.
- ▶ Fibre Channel Protocol (FCP)
This standard protocol is used for communicating with disk and tape devices through FC switches and directors. The FCP channel can connect to FCP SAN fabrics and access FCP/SCSI devices. FCP is used by z/VM, kernel-based virtual machine (KVM), z/VSE, and Linux on IBM Z environments.

FICON Express32S features are implemented by using Peripheral Component Interconnect Express (PCIe) cards, and offers better port granularity and improved capabilities over the previous FICON Express features. FICON Express32S is the preferred technology for new systems. The features support a link data rate up to 32 Gbps and can auto-negotiate to 8, 16, or 32 Gbps.

zHyperLink Express

zHyperLink was created to provide fast access to data by way of low-latency connections between the IBM Z platform and storage.

The zHyperLink Express1.1 feature allows you to make synchronous requests for data that is in the storage cache of the IBM DS8900F. This process is done by directly connecting the zHyperLink Express1.1 port in the IBM z16 to an I/O Bay port of the IBM DS8000®. This short distance (up to 150 m [492 feet]), direct connection is designed for low-latency reads and writes, such as with IBM DB2® for z/OS synchronous I/O reads and log writes.

Working with the FICON SAN Infrastructure, zHyperLink can improve application response time, which reduces I/O-sensitive workload response time by half without requiring application changes.²

Note: The zHyperLink channels complement FICON channels, but they do *not* replace FICON channels. FICON remains the main data driver and is mandatory for zHyperLink usage.

² The performance results can vary depending on the workload. Use zBNA tool for the zHyperLink planning.

For more information about the supported FICON Express and zHyperLink Express features, see 3.2, “Storage connectivity” on page 31.

1.2.2 Network connectivity

HiperSockets

IBM HiperSockets is an integrated function of the IBM Z platforms that supplies attachments to up to 32 high-speed virtual LANs, with minimal system and network overhead.

HiperSockets is a function of the Licensed Internal Code (LIC). It provides LAN connectivity across multiple system images on the same IBM Z platform by performing memory-to-memory data transfers in a secure way.

The HiperSockets function eliminates the use of I/O subsystem operations. It also eliminates having to traverse an external network connection to communicate between LPARs in the same IBM Z platform. In this way, HiperSockets can help with server consolidation by connecting virtual servers and simplifying the enterprise network.

The IBM z16 is a fully virtualized platform that can support many system images at once. Therefore, network connectivity covers the connections between the platform and external networks with Open Systems Adapter-Express (OSA-Express) and RDMA over Converged Ethernet (RoCE) Express features, and specialized internal connections for intra-system communication through IBM HiperSockets and Internal Shared Memory (ISM).

OSA-Express

The OSA-Express features provide local area network (LAN) connectivity and comply with IEEE standards. In addition, OSA-Express features assume several functions of the TCP/IP stack that normally are performed by the PU, which allows significant performance benefits by offloading processing from the operating system.

OSA-Express7S 1.2 features continue to support copper and fiber optic (single-mode and multimode) environments.

RoCE Express

The RoCE Express3 features can provide local area network (LAN) connectivity for Linux on IBM Z and comply with IEEE standards. In addition, RoCE Express features assume several functions of the TCP/IP stack that normally are performed by the PU, which allows significant performance benefits by offloading processing from the operating system.

The 25 GbE and 10 GbE RoCE Express3 features³ use Remote Direct Memory Access (RDMA) over Converged Ethernet (RoCE) to provide fast memory-to-memory communications between two IBM Z platforms.

These features help reduce consumption of CPU resources for applications that use the TCP/IP stack (such as IBM WebSphere® that accesses an IBM Db2® database). They can also help reduce network latency with memory-to-memory transfers by using Shared Memory Communications over RDMA (SMC-R).

With SMC-R, you can transfer huge amounts of data quickly and at low latency. SMC-R is transparent to the application and requires no code changes, which enables rapid time to value.

³ RoCE Express features can also be used as general-purpose IP interfaces with Linux on IBM Z.

Internal Shared Memory

ISM is a virtual Peripheral Component Express (PCI) network adapter that enables direct access to shared virtual memory. It provides a highly optimized network interconnect for IBM Z platform intra-communications. Shared Memory Communications-Direct Memory Access (SMC-D) uses ISM.

SMC-D optimizes operating systems communications in a way that is transparent to socket applications. It also reduces the CPU cost of TCP/IP processing in the data path, which enables highly efficient and application-transparent communications.

SMC-D requires no extra physical resources (such as RoCE Express features, PCIe bandwidth, ports, I/O slots, network resources, or Ethernet switches). Instead, SMC-D uses LPAR-to-LPAR communication through HiperSockets or an OSA-Express feature for establishing the initial connection.

z/OS and Linux on IBM Z support SMC-R and SMC-D. Now, data can be shared by way of memory-to-memory transfer between z/OS and Linux on IBM Z.

For more information about the available network connectivity features, see 3.3, “Network connectivity” on page 34.

1.2.3 Cryptography

IBM z16 provides two main cryptographic functions: CP Assist for Cryptographic Functions (CPACF) and Crypto-Express8S.

CPACF

CPACF is a high performance, low-latency coprocessor that performs symmetric key encryption operations and calculates message digests (hashes) in hardware. The following algorithms are supported:

- ▶ AES
- ▶ Data Encryption Standard (DES) and Triple Data Encryption Standard (TDES)
- ▶ Secure Hash Algorithm (SHA)-1
- ▶ SHA-2
- ▶ SHA-3

CPACF supports Elliptic Curve Cryptography (ECC) clear key, improving the performance of Elliptic Curve algorithms. The following algorithms are supported:

- ▶ EdDSA (Ed448 and Ed25519)
- ▶ ECDSA (P-256, P-384, and P-521)
- ▶ ECDH (P-256, P-384, P521, X25519, and X448)
- ▶ Support for protected key signature creation

Crypto-Express8S

The tamper-sensing and tamper-responding Crypto-Express8S features provide acceleration for high-performance cryptographic operations and support up to 85 domains with the IBM z16 A01. This specialized hardware performs AES, DES and TDES, RSA, Elliptic Curve (ECC), SHA-1, and SHA-2, and other cryptographic operations.

It also supports specialized high-level cryptographic APIs and functions, including those functions that are required with quantum-safe cryptography and in the banking industry. Crypto-Express8S features are designed to meet the Federal Information Processing Standards (FIPS) 140-2 Level 4 and Payment Card Industry PTS HSM (PCI-HSM) security requirements for hardware security modules (HSMs).

For more information about cryptographic features and functions, see 3.6, “Cryptographic features” on page 41, and 4.7, “Quantum-safe technology” on page 74.

1.2.4 Clustering connectivity

A Parallel Sysplex is an IBM Z clustering technology that is used to make applications that are running on logical and physical IBM Z platforms highly reliable and available. The IBM Z platforms in a Parallel Sysplex are interconnected by way of coupling links.

Coupling connectivity on the IBM z16 uses Coupling Express2 E Long Reach (CE2 LR) and ICA SR features. The ICA SR feature supports distances up to 150 meters (492 feet); the CE2 LR feature supports unrepeated distances of up to 10 km (6.21 miles) between IBM Z platforms.

For more information about coupling and clustering features, see 3.4, “Clustering connectivity” on page 38.

1.2.5 Special-purpose features and functions

IBM takes a *total systems* view regarding the design and development the IBM Z platform. The IBM Z stack is built around digital services, agile application development, connectivity, and system management. This design approach creates an integrated, diverse platform with specialized hardware and dedicated computing capabilities.

The IBM z16 delivers a range of features and functions, allowing PUs to concentrate on computational tasks, while distinct, specialized features take care of the rest. For more information about these features and other IBM z16 features, see in Chapter 4, “IBM z16 system design strengths” on page 45.

1.2.6 Capacity on Demand and performance

The IBM z16 enables just-in-time deployment of processor resources. The Capacity on Demand (CoD) function can dynamically change available system capacity. This function can help respond to new business requirements with flexibility and precise granularity.

The IBM Tailored Fit Pricing for IBM Z options is designed to deliver unmatched simplicity and predictability of hardware capacity and software pricing, even in the constantly evolving era of hybrid cloud.

IBM Z helps to make embracing hybrid cloud easier with Tailored Fit Pricing for IBM Z. The pricing option delivers simplicity, flexibility, and predictability of pricing across the stack, even with constantly increasing unpredictability in business demand.

Also contributing to the extra capacity on the IBM z16 are numerous improvements in processor chip design, including new instructions, multithreading, and redesigned and larger caches.

In its maximum configuration, the IBM z16 A01 Max200 can deliver up to 17%⁴ more capacity than the IBM z15 T01 Max190. A IBM z16 A01 1-way system has approximately 11% more capacity than a IBM z15 T01 1-way system.

⁴ Variations on all the observed increased performance depend on the configuration and workload type.

Within each single drawer, IBM z16 provides 25% greater capacity than IBM z15 for standard models and 40% greater capacity on the max config model, enabling efficient scaling of partitions.

For more information, see 4.3, “Capacity and performance” on page 57.

1.2.7 Reliability, availability, and serviceability

The IBM z16 offers the same high quality of service and reliability, availability, and serviceability (RAS) that is traditional in IBM Z platforms. The RAS strategy uses a building-block approach that meets the stringent requirements for achieving continuous, reliable operation. The following RAS building blocks are available:

- ▶ Error prevention
- ▶ Error detection
- ▶ Recovery
- ▶ Problem determination
- ▶ Service structure
- ▶ Change management
- ▶ Measurement
- ▶ Analysis

The RAS design objective is to manage change by learning from previous product releases and investing in new RAS functions to eliminate or minimize all sources of outages.

System Recovery Boost with the optional System Recovery Boost Upgrade (temporary capacity upgrade) is a function to accelerate operating system and services start and shutdown times. The IBM z16 also provides boosted processor capacity and parallelism for specific events, such as middleware starts and restarts, SVC dump processing, and HyperSwap configuration load and reload, to minimize the impact on running workloads.

For more information about RAS, see 4.4, “Reliability, availability, and serviceability” on page 63.

1.3 IBM z16 software support

The IBM z16 supports a wide range of IBM and ISV software solutions. This range includes traditional batch and online transaction processing (OLTP) environments, such as IBM Customer Information Control System (IBM CICS®), IBM Information Management System (IBM IMS), and IBM Db2. It also includes the following web services (among others):

- ▶ Java platform
- ▶ Linux and open standards applications
- ▶ WebSphere
- ▶ IBM z/OS Connect Enterprise Edition

The following operating systems are supported on the IBM z16:

- ▶ z/OS Version 2 Release 5 with program temporary fixes (PTFs)
- ▶ z/OS Version 2 Release 4 with PTFs
- ▶ z/OS Version 2 Release 3 with PTFs
- ▶ z/OS Version 2 Release 2 with PTFs (toleration support only)
- ▶ z/VM Version 7 Release 3
- ▶ z/VM Version 7 Release 2 with PTFs
- ▶ z/VM Version 7 Release 1 with PTFs

- ▶ z/VSE Version 6 Release 2 with PTFs
- ▶ z/TPF Version 1 Release 1 (compatibility support)

IBM plans to support 21st Century Software VSEn V6.3 on IBM z16. For more information, see [this web page](#).

IBM plans to support the following Linux on IBM Z distributions⁵ on IBM z16:

- ▶ SUSE SLES 15 SP3 and SUSE SLES 12 SP5
- ▶ Red Hat RHEL 8.4 and Red Hat RHEL 7.9
- ▶ Ubuntu 22.04 LTS and Ubuntu 20.04.1 LTS

The support statements for the IBM z16 also cover the KVM hypervisor on distribution levels that have KVM support.

For more information about the IBM z16 software support, see Chapter 5, “Operating system support” on page 77.

1.3.1 IBM compilers

Compilers are built with specific knowledge of the system architecture, which is used during code generation. Therefore, the use of the latest compilers is essential to extract the maximum benefit of a platform’s capabilities. IBM compilers use the latest architecture enhancements and new instruction sets to deliver more value.

With IBM Enterprise COBOL for z/OS and IBM Enterprise PL/I for z/OS, decades of IBM experience in application development can be used to integrate COBOL and PL/I with web services, XML, and Java. Such interoperability makes it possible to capitalize on IT investments, while smoothly incorporating new, web-based applications into the infrastructure.

z/OS, XL C/C++, and XL C/C++ for Linux on IBM Z help with creating and maintaining critical business applications that are written in C or C++ to maximize application performance and improve developer productivity. These compilers transform C or C++ source code into executable code that fully uses the z/Architecture. This transformation is possible because of hardware-tailored optimizations, built-in functions, performance-tuned libraries, and language constructs that simplify system programming and boost application runtime performance.

Compilers, such as COBOL, PL/I, and z/OS XL C/C++, are inherently optimized on the IBM z16 because they use floating point registers rather than memory or fast mathematical computations. The use of compilers that take advantage of hardware enhancements is key to improving application performance, reducing CPU usage, and lowering operating costs.

For more information, see 5.1.2, “Application development and languages” on page 79 and 5.1.3, “Supported IBM compilers” on page 80.

⁵ All require extra service. For more information, see 5.2.6, “Linux on IBM Z” on page 85.



IBM z16 hardware overview

This chapter expands on the descriptions of the key hardware elements of the IBM z16 that were presented in 1.2, “IBM z16 technical overview” on page 5.

For more information about the key capabilities and enhancements of the IBM z16, see *IBM z16 (3931) Technical Guide*, SG24-8951.

This chapter describes the following topics:

- ▶ 2.1, “Models and upgrade paths” on page 14
- ▶ 2.2, “Frames and cabling” on page 15
- ▶ 2.3, “CPC drawers” on page 17
- ▶ 2.4, “I/O system structure” on page 24
- ▶ 2.5, “Power and cooling” on page 26

2.1 Models and upgrade paths

The IBM z16 (machine type 3931) has one model: the A01. The maximum number of characterizable processors is represented by feature names Max39, Max82, Max125, Max168, and Max200.

The IBM z16 A01 central processor complex (CPC) is built by using the IBM Telum processor design. Each processor chip consists of eight cores. Two processor chips are packaged in the dual-chip module (DCM). Each DCM can have 9 - 11 or 10 - 15 active processor unit (PU) cores (depending on configuration). Spare PUs, System Assist Processors (SAPs), and two Integrated Firmware Processors (IFPs) are included in the IBM z16 configuration.

The number of characterizable PUs, SAPs, and spare PUs for the various features is listed in Table 2-1. For more information about PU characterization types, see “PU characterization” on page 21.

Table 2-1 IBM z16 A01 processor unit configurations

Feature name	Number of CPC drawers	Feature code	Characterizable processor units	Standard SAPs	Spares
Max39	1	0667	0 - 39	5	2
Max82	2	0668	0 - 82	10	2
Max125	3	0669	0 - 125	15	2
Max168	4	0670	0 - 168	20	2
Max200	4	0671	0 - 200	24	2

The supported upgrade paths for the IBM z16 A01 are shown in Figure 2-1.

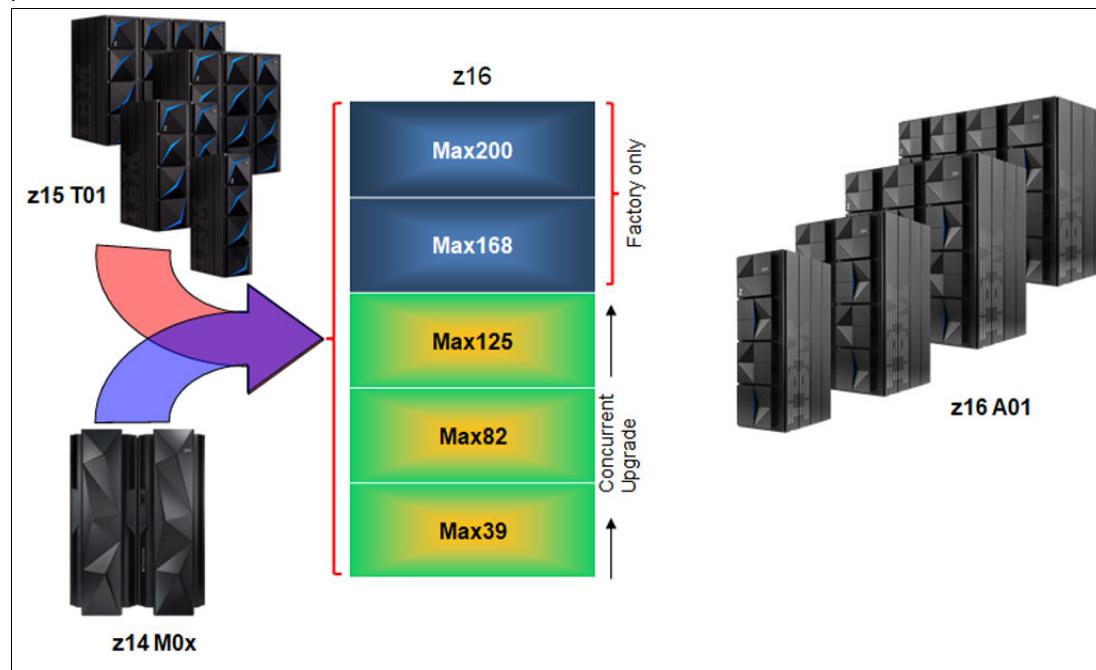


Figure 2-1 IBM z16 A01 upgrade paths

If an upgrade request cannot be fulfilled by using the existing configuration, a hardware upgrade is required in which one or more CPC drawers are added to accommodate the needed capacity. With the IBM z16 A01, more CPC drawers can be installed concurrently from a Max39 to a Max82, and to a Max125.

Note: No field upgrade is available to a Max 168 or a Max 200; these two features are factory-shipped only.

With the IBM z16 A01, concurrent upgrades are available for central processors (CPs), Integrated Facilities for Linux (IFLs), Integrated Coupling Facilities (ICFs), IBM Z Integrated Information Processors (zIIPs), and SAPs. However, concurrent PU upgrades require that more PUs are physically installed, but not activated previously.

In the rare event of a PU failure, one of the spare PUs is immediately and transparently activated and assigned the characteristics of the failing PU. Two spare PUs are always available on an IBM z16 A01.

The IBM z16 A01 offers 317 capacity levels. In all, 200 capacity levels are based on the number of physically used CPs, plus up to 117 subcapacity models for the first 39 CPs.

For more information, see 4.3.1, “Capacity settings” on page 57.

2.2 Frames and cabling

The IBM z16 A01 uses 19-inch frames and industry-standardized power and hardware. It can be configured as a one-, two-, three-, or four-frame system. Each frame takes up only two standard 24-inch floor tiles of space, which aligns with modern data center layouts.

The IBM z16 A01 configuration options as compared to previous IBM Z platforms are listed in Table 2-2.

Table 2-2 IBM z16 configuration options compared to IBM z14 and IBM z15 configurations

System	Number of frames	Number of CPC drawers	Number of I/O drawers	I/O and power connections	Power options ^a	Cooling options
IBM z16	1 - 4	1 - 4	0 - 12 ^b	Rear only	PDU or BPA	Radiator (air) only
IBM z15	1 - 4	1 - 5	0 - 12 ^c	Rear only	PDU or BPA	Radiator (air) or water-cooling unit (WCU)
IBM z14	2	1 - 4	0 - 5	Front and rear	BPA	Radiator (air) or WCU

a. The Power Distribution Unit (PDU) option supports the air-cooling (radiator) option; the Bulk Power Assembly (BPA) option supports both air-cooling and water-cooling options.

b. Maximum of 12 if ordered with a PDU or maximum of 10 if ordered with a BPA.

c. Maximum of 12 if ordered with a PDU or maximum of 11 if ordered with a BPA.

The number of Peripheral Component Interconnect Express+ (PCIe+) I/O drawers can vary based on the number of I/O features, power options (PDU or BPA), and number of CPC drawers installed. For a PDU system, a maximum configuration of up to 12 PCIe+ I/O drawers can be installed. PCIe+ I/O drawers can be added concurrently.

In addition, the IBM z16 A01 supports top-exit options for the fiber optic and copper cables that are used for I/O and power. These options give you more flexibility in planning where the system is installed, eliminate the need for cables to be run under a raised floor, and increase air flow over the system.

The IBM z16 A01 supports installation on raised floor and non-raised floor environments.

Figure 2-2 shows the front view of a fully configured IBM z16 A01 with radiator cooling, four CPC drawers, and 12 PCIe+ I/O drawers.

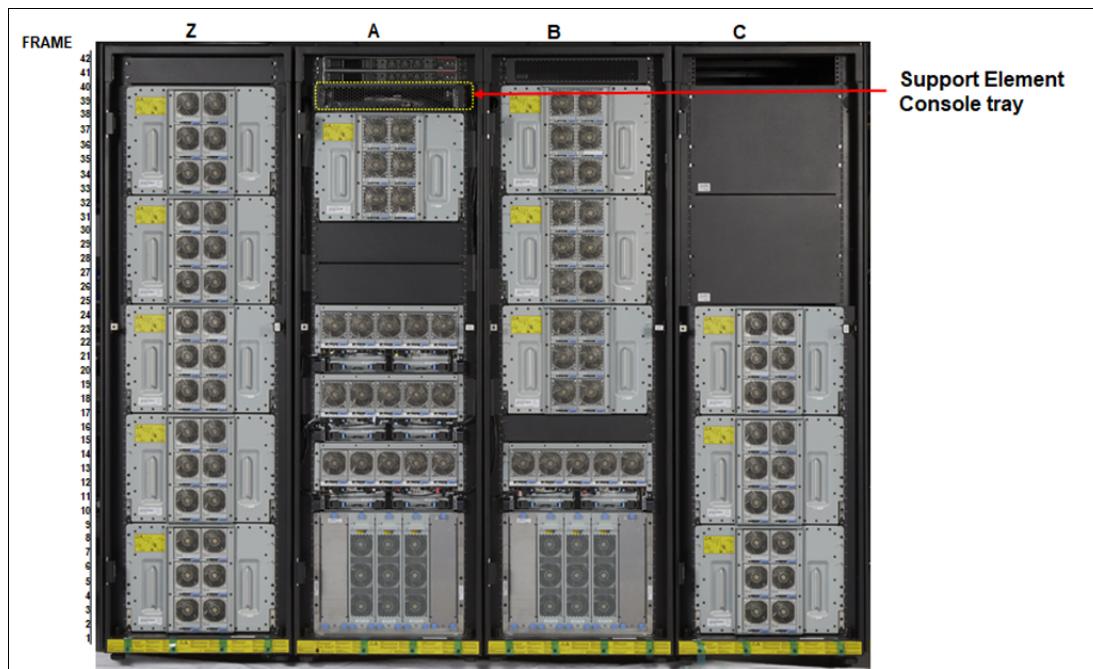


Figure 2-2 Front view of a fully configured IBM z16 A01 with radiator cooling

Figure 2-3 shows the rear view of a fully configured PDU-based IBM z16 A01 with a total of 16 drawers (I/O and CPC combined), and two radiator cooling units.

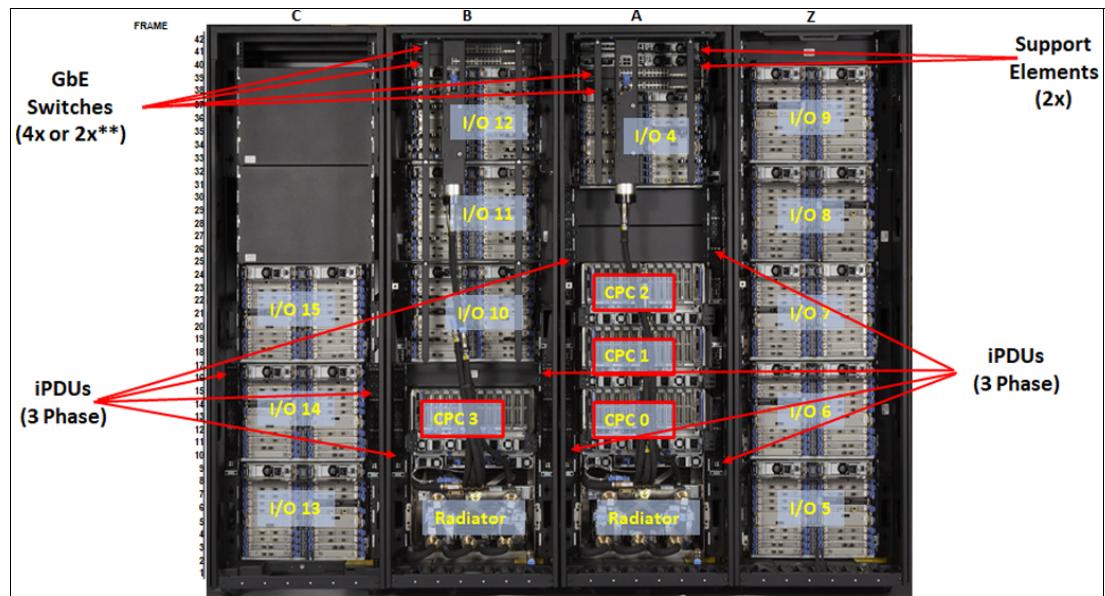


Figure 2-3 Rear view of a fully configured IBM z16

The IBM configurator that is used during the order process calculates the number of frames that is required and placement of CPC and PCIe+ I/O drawers.

Factors that determine the number of frames for IBM z16 A01 configuration include the following features:

- ▶ Number of CPC drawers
- ▶ Plan ahead features for more CPC drawers
- ▶ Number of I/O features (determines the number of PCIe+ I/O drawers)
- ▶ PDU or BPA power

2.3 CPC drawers

The IBM z16 A01 can be configured with up to four CPC drawers (three in the A Frame and one in the B Frame). Each CPC drawer contains the following elements:

- ▶ DCMs
- Four DCMs that containing 8 central processor (CP) chips and 64 physical cores per drawer interconnected (each cooled by an internal water loop).
- ▶ Memory:
- A minimum of 512 GB and a maximum of 40 TB of memory per system (excluding 256 GB for hardware system area [HSA]) is available for use. For more information, see Table 2-3 on page 22.
 - Up to 48 dual inline memory modules (DIMMs) that are 32, 64, 128, 256, or 512 GB are plugged in a CPC drawer.

- ▶ Fanouts
 - Each CPC drawer supports up to 12 PCIe+ fanout adapters to connect to the PCIe+ I/O drawers, and Integrated Coupling Adapter Short Reach (ICA SR) coupling links:
 - Two-port Peripheral Component Interconnect Express (PCIe) 16 GBps I/O fanout, each port supports one domain in the 16-slot PCIe+ I/O drawers.
 - ICA SR1.1 and ICA SR PCIe fanouts for coupling links (two links, 8 GBps each).
- ▶ Three or four Power Supply Units (PSUs), depending on the configuration (PDU or BPA), which provide power to the CPC drawer and are accessible from the rear. Loss of one PSU leaves enough power to satisfy the power requirements of the entire drawer. The PSUs can be concurrently maintained.
- ▶ Two dual-function Base Management Cards (BMCs)\Oscillator Cards (OSCs), which provide redundant interfaces to the internal management network and provide clock synchronization to the IBM Z platform.
- ▶ Two dual-function Processor Power Cards (PPCs), which control Voltage Regulation, PSU and Fan control. The PPCs are redundant and can be concurrently maintained.
- ▶ Five fans are installed at the front of the drawer to provide cooling airflow for the resources that are installed in the drawer (except for the PU SCMs, which are internally water-cooled).

The CPC drawer communication topology is shown in Figure 2-4. All CPC drawers are interconnected with high-speed communications links (A-Bus) through the PU chips. Symmetric multiprocessor (SMP-9) cables are used to interconnect all the CPC drawers. The X-Bus provides connectivity between DCMs within on the drawer, while the M-Bus connects the two PU chips on each DCM.

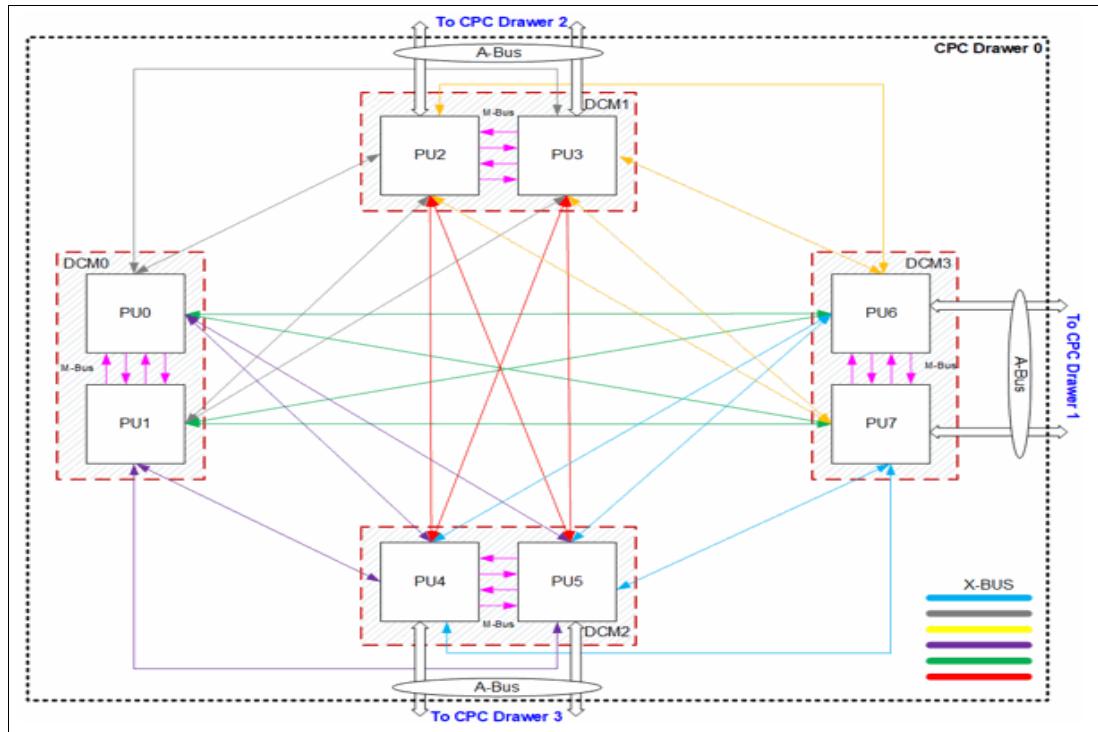


Figure 2-4 IBM z16 A01 CPC drawer communication topology

The design that is used to connect the PU and storage control allows the system to be operated and controlled by the IBM Processor Resource/Systems Manager (PR/SM) facility as a memory-coherent SMP system.

2.3.1 Dual-chip modules

The CPC drawer always includes four DCMs. Each DCM contains two PU chips. Each PU chip contains eight cores each with 128 KB Instruction and Data L1 cache and 32 MB semi-private L2 caches.

2.3.2 Processor unit

PU is the generic term for an IBM z/Architecture processor. Each PU is a superscalar processor with the following attributes:

- ▶ Up to six instructions can be decoded per clock cycle.
- ▶ Up to 10 instructions can be in execution per clock cycle.
- ▶ Instructions can be issued out of order. The PU uses a high-frequency, low-latency pipeline that provides robust performance across a wide range of workloads.
- ▶ Memory accesses might not be in the same instruction order (out-of-order operand fetching).
- ▶ Most instructions flow through a pipeline with varying numbers of steps for different types of instructions. Several instructions can be running at any moment, and are subject to the maximum number of decodes and completions per cycle.

Processor cache structure

The on-chip cache for the PU (core) features the following design:

- ▶ Each PU core has an L1 cache (private) that is divided into a 128 KB cache for instructions and a 128 KB cache for data.
- ▶ Each PU core has a semi-private L2 cache, which is implemented as 32 MB, near the core.

Note: L1 and L2 are physical cache and are implemented in dense SRAM.

- ▶ Each PU core contains a 256 MB shared-victim virtual L3 cache. The shared-victim virtual L3 Cache is a logical construction that comprises all eight semi-private L2s ($8 \times 32 \text{ MB} = 256 \text{ MB}$) belonging to the other cores.
- ▶ Each CPC drawer contains a 2 GB shared-victim virtual L4, consisting of the “remote” virtual L3 caches of the DCMs in the CPC drawer.

This on-chip cache implementation optimizes system performance for high-frequency processors and includes the following features:

- ▶ Cache improvements
- ▶ New Translation/TLB2 design
- ▶ Pipeline optimizations
- ▶ Better branch prediction
- ▶ New accelerators and architectures
- ▶ Secure Execution support

The IBM z16 cache structure is shown Figure 2-5.

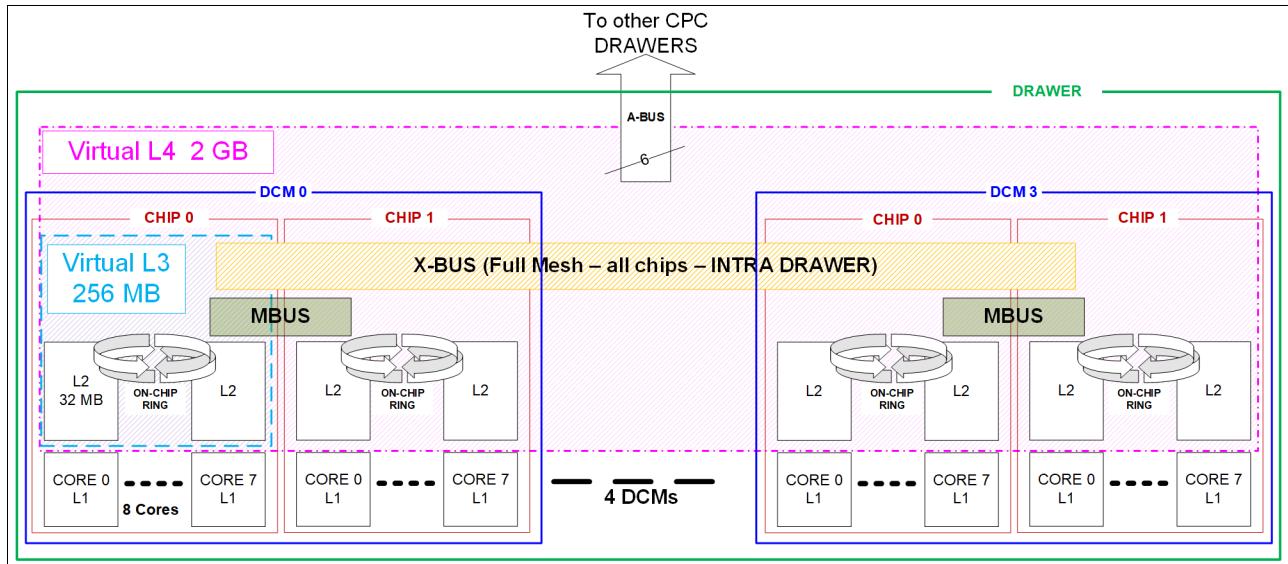


Figure 2-5 IBM z16 cache structure

PU sparing

Hardware fault detection is embedded throughout the system design and is combined with comprehensive instruction-level retry and dynamic PU sparing. This function provides the reliability and availability that is required for true IBM Z integrity.

On-core cryptographic hardware

Dedicated on-chip cryptographic hardware for each PU core includes extended key and hash sizes for the Advanced Encryption Standard (AES) and Secure Hash Algorithm (SHA). For more information, see 3.6, “Cryptographic features” on page 41. This cryptographic hardware is available with any processor type; for example, CP, zIIP, and IFL.

On-chip functions

Consider the following points:

- IBM Integrated Accelerator for zEnterprise® Data Compression replaces the IBM zEnterprise Data Compression (zEDC) Express PCIe feature that was on previous IBM Z platforms.
- The sort accelerator uses the sort instruction (SORTL) instruction to be used by DFSORT and the IBM Db2 Utilities for z/OS Suite to help reduce CPU usage and improve elapsed time for sort workloads.
- Integrated Accelerator for Artificial Intelligence (AIU) is implemented on each PU chip and shared among all cores. It provides matrix array for multiplication and convolution alongside the specialty engines for complex functions.

The AIU provides a Neural Network Processing Assist (NNPA) instruction, which operates directly on tensor data in user space.

Software support

The IBM z16 PUs provide full compatibility with software for z/Architecture, and extend the Instruction Set Architecture (ISA) to enable enhanced functions and performance. New for IBM z16 is instructions for AIU engine.

PU characterization

PUs are ordered in single increments. The internal system functions are based on the configuration that is ordered. They characterize each PU into one of various types during system initialization, which is often called a power-on reset (POR) operation.

Characterizing PUs dynamically without a POR is possible by using a process that is called *Dynamic Processor Unit Reassignment*. A PU that is not characterized cannot be used. Each PU can be designated with one of the following characterizations:

- ▶ CP: These standard processors are used for general workloads.
- ▶ IFL: Designates processors to be used specifically for running the Linux application programs.
- ▶ Unassigned Integrated Facilities for Linux (UIFL): Allows you to directly purchase an IFL feature that is marked as being deactivated upon installation, which avoids software charges until the IFL is brought online for use.
- ▶ zIIP: An “Off Load Processor” for workloads that are restricted to Db2 type applications. Also used for the System Recovery Boost feature. For more information, see 4.4, “Reliability, availability, and serviceability” on page 63.
- ▶ Integrated Coupling Facility (ICF): Designates processors to be used specifically for coupling.
- ▶ SAP: Designates processors to be used specifically for assisting I/O operations.
- ▶ IFP: The IFP is standard and not defined by the customer (it is used for infrastructure management).

At least one CP must be purchased before a zIIP can be purchased. You can purchase up to two zIIPs for each purchased CP (assigned or unassigned) on the system. However, a logical partition (LPAR) definition can go beyond the 1:2 ratio. For example, on a system with two physical CPs, a maximum of four physical zIIPs can be installed. An LPAR definition for that system can contain up to two logical CPs and four logical zIIPs. Another possible configuration is one logical CP and three logical zIIPs.

Converting a PU from one type to any other type is possible by using the Dynamic Processor Unit Reassignment process. These conversions occur concurrently with the system operation.

Note: The addition of ICFs, IFLs, zIIPs, and SAP to the IBM z16 does not change the system capacity setting or its millions of service units (MSU) rating.

2.3.3 Memory

Maximum physical memory size is directly related to the number of CPC drawers in the system. An IBM Z platform includes more installed memory than was ordered because part of the installed memory is used to implement the redundant array of independent memory (RAIM) design. With the IBM z16, up to 10 TB of memory per CPC drawer can be ordered and up to 40 TB for a four-CPC drawer system.

Important: z/OS requires a minimum of 8 GB of memory (2 GB of memory when running under z/VM). z/OS V2R5 can support up to 16 TB of memory in an LPAR.

The minimum and maximum memory sizes for each IBM z16 feature are listed in Table 2-3.

Table 2-3 IBM z16 Model A01 memory per feature

Feature name	CPC drawers	Memory
Max39 (Feature Code 0667)	1	512 GB - 10 TB
Max82 (Feature Code 0668)	2	512 GB - 20 TB
Max125 (Feature Code 0669)	3	512 GB - 30 TB
Max168 (Feature Code 0670)	4	512 GB - 40 TB
Max200 (Feature Code 0671)	4	512 GB - 40 TB

The HSA on the IBM z16 has a fixed amount of memory (256 GB) that is managed separately from available memory. However, the maximum amount of orderable memory can vary from the theoretical number because of dependencies on the memory granularity. On IBM z16 platforms, the granularity for memory is in 64, 128, 256, 512, 1024, and 2048 GB increments.

Physically, memory is organized in the following ways:

- ▶ A CPC drawer always contains a minimum of 1024 GB to a maximum of 10 TB of installed memory, of which 10 TB maximum is usable by the operating system.
- ▶ A CPC drawer can have more installed memory than is enabled. The excess memory can be enabled by a Licensed Internal Code (LIC) load.
- ▶ Memory upgrades are first satisfied by using installed but unused memory capacity until it is exhausted. When no more unused memory is available from the installed cards, the cards must be upgraded to a higher capacity, or a CPC drawer with more memory must be installed.

When an LPAR is activated, PR/SM attempts to allocate PUs and the memory of an LPAR in a single CPC drawer. However, if this allocation is not possible, PR/SM uses memory resources in any CPC drawer. For example, if the allocated PUs span more than one CPC drawer, PR/SM attempts to allocate memory across that same set of CPC drawers (even if all required memory is available in only one of those CPC drawers).

No matter which CPC drawer the memory is installed in, an LPAR can access that memory after it is allocated. The IBM z16 is an SMP system because the PUs can access all of the available memory.

A memory upgrade is considered to be concurrent when it requires no change of the physical memory cards. A memory card change is disruptive when no use is made of Enhanced Drawer Availability (EDA). In a multiple-CPC drawer system, a single CPC drawer can be concurrently removed and reinstalled for a repair with EDA.

For model upgrades that involve the addition of a CPC drawer, the minimum usable memory increment (512 GB) is added to the system. During an upgrade, adding a CPC drawer and physical memory in the new drawer are concurrent operations.

Concurrent memory upgrade

If physical memory is available, memory can be upgraded concurrently by using Licensed Internal Code Configuration Control (LICCC).

Redundant array of independent memory

RAIM technology makes the memory subsystem (in essence) a fully fault-tolerant N+1 design. The RAIM design automatically detects and recovers from failures of dynamic random access memory (DRAM), sockets, memory channels, or DIMMs.

The RAIM design is fully integrated in the IBM z16, and is enhanced to include one Memory Controller Unit (MCU) per processor chip, with eight memory channels and one DIMM per channel. The MCU enables memory to be implemented as RAIM. This technology has significant reliability, availability, and serviceability (RAS) capabilities in the area of error correction. Bit, lane, DRAM, DIMM, socket, and complete memory channel failures (including many types of multiple failures) can be detected and corrected.

For more information about memory design and configuration options, see *IBM z16 (3931) Technical Guide*, SG24-8951.

2.3.4 Hardware system area

The HSA is a fixed-size, reserved area of memory that is separate from the customer-purchased memory. The HSA is used for several internal functions, but the bulk of it is used by channel subsystem (CSS) functions.

The fixed size 256 GB HSA of IBM z16 is large enough to accommodate any LPAR definitions or changes, which eliminates most outage situations and the need for extensive planning.

A fixed, large HSA allows the dynamic I/O capability of the IBM z16 to be enabled by default. It also enables the dynamic addition and removal of the following features:

- ▶ LPAR to new or existing CSS
- ▶ CSS (up to six can be defined in IBM z16 A01)
- ▶ Subchannel set (up to four can be defined in IBM z16 A01)
- ▶ Devices, up to the maximum number permitted, in each subchannel set
- ▶ Logical processors by type
- ▶ Cryptographic adapters

2.4 I/O system structure

The IBM z16 supports the PCIe-based infrastructure for the PCIe+ I/O drawers. The PCIe I/O infrastructure consists of the Dual Port PCIe fanouts in the CPC drawers that support 16 GBps connectivity to the PCIe+ I/O drawer.

Ordering of I/O features: Ordering I/O feature types determines the suitable number of PCIe+ I/O drawers.

Figure 2-6 shows a high-level view of the I/O system structure for the IBM z16 A01.

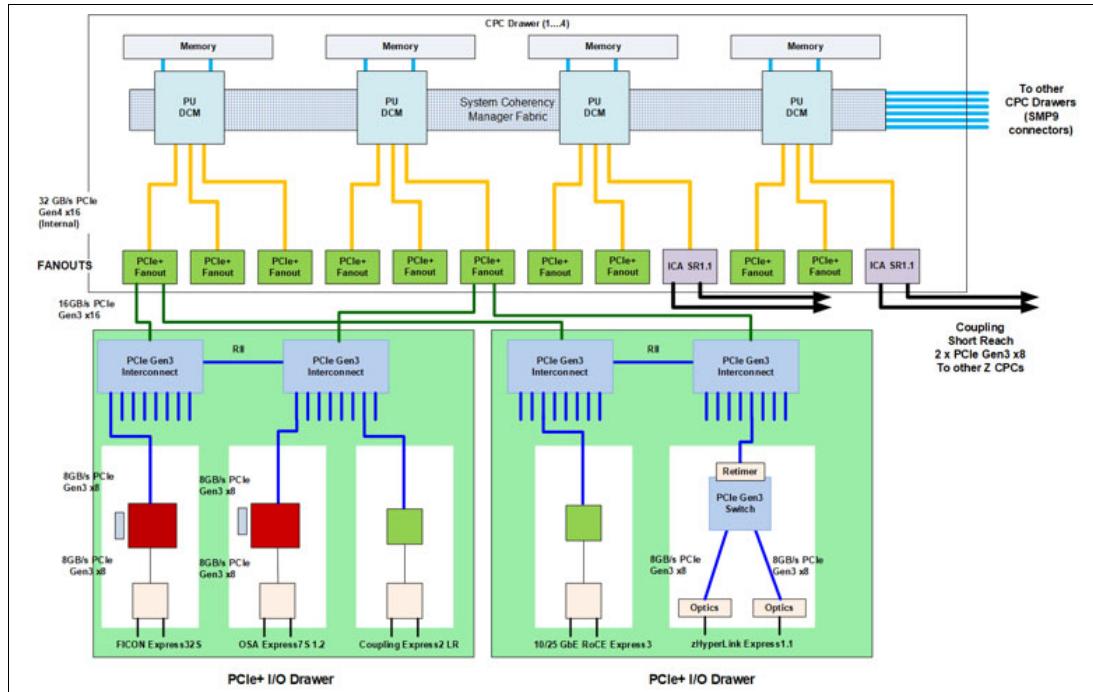


Figure 2-6 IBM z16 A01 I/O system structure

The IBM z16 A01 CPC drawer has 12 fanouts (numbered LG01 - LG12). The fanouts that are installed in these positions can be one of the following types:

- ▶ Dual port PCIe+ fanouts for PCIe+ I/O drawer connectivity
- ▶ ICA SR fanouts for coupling
- ▶ Filler plates to assist with airflow cooling

For coupling link connectivity (Parallel Sysplex and Server Time Protocol (STP) configuration), the IBM z16 supports the following link types:

- ▶ ICA SR1.1 and ICA SR (installed in a CPC drawer)
- ▶ Coupling Express2 Long Reach (CE LR) (installed in a PCIe+ I/O drawer)

For systems with multiple CPC drawers, the locations of the PCIe+ fanouts are configured and plugged across all drawers for maximum availability. This configuration helps ensure that alternative paths maintain access to critical I/O devices, such as storage and networks (see Figure 2-7 on page 25).

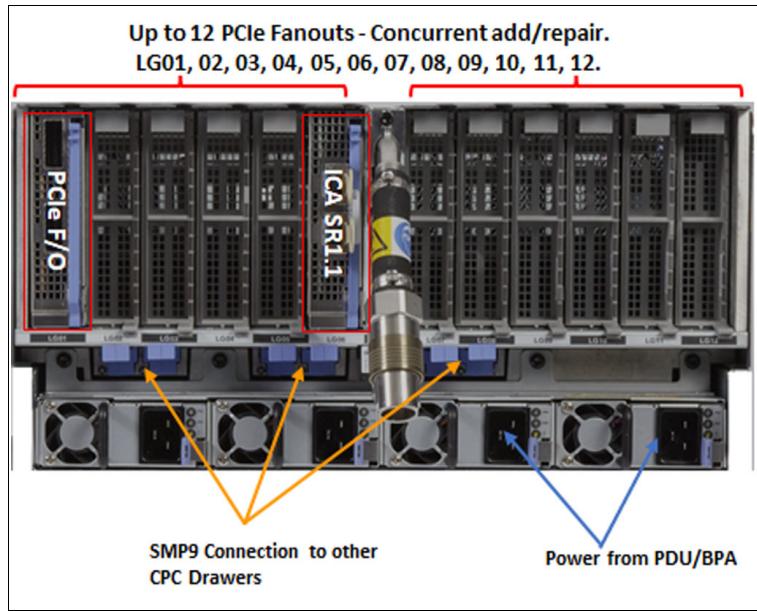


Figure 2-7 IBM z16 A01 CPC drawer: Rear view

The PCIe+ I/O drawer (see Figure 2-8), is a 19-inch single side drawer that is 8U high. I/O features are installed horizontally, with cooling air flow from front to rear. The drawer contains 16 adapter slots and two slots for PCIe switch cards.

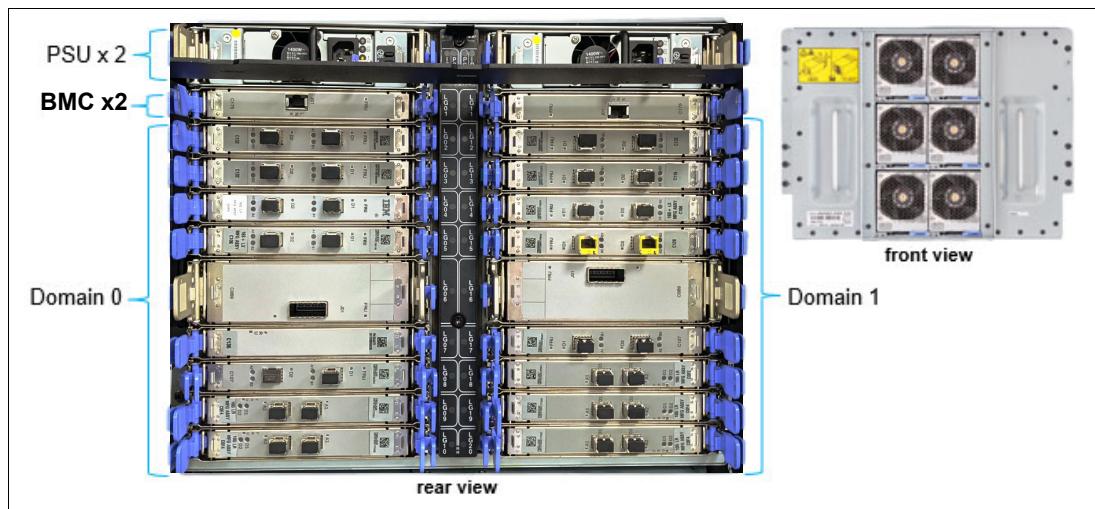


Figure 2-8 PCIe+ I/O drawer: Rear and front view

The two I/O domains per drawer each contain up to eight I/O features that support the following types:

- ▶ FICON Express32S, FICON Express16SA, or FICON Express16S+
- ▶ OSA-Express7S 1.2, OSA-Express7S, or OSA-Express6S
- ▶ Crypto-Express8S, Crypto-Express7S, or Crypto-Express6S
- ▶ RDMA over Converged Ethernet (RoCE) Express3, RoCE Express2.1, or RoCE Express2
- ▶ zHyperLink Express 1.1 and zHyperLink Express
- ▶ Coupling Express2 LR

For more information about the I/O feature that is available with the IBM z16, see Chapter 3, “Supported features and functions” on page 29.

2.5 Power and cooling

The IBM z16 A01 meets the American Society of Heating, Refrigerating, and Air-Conditioning Engineers ([ASHRAE](#)) Class A3 specifications. ASHRAE is an organization that is devoted to the advancement of indoor-environment-control technology in the heating, ventilation, and air conditioning industry.

2.5.1 Power options

The IBM z16 A01 19-inch frames are available with the following power options:

- ▶ PDU

Use of PDU for IBM z16 A01 can enable fewer frames, which allows for extra I/O slots and improves power efficiency to lower overall energy costs. It offers some standardization and ease of data center installation planning. PDU supports up to 12 PCIe+ I/O drawers.

- ▶ Bulk Power Assembly (BPA)

The BPA supports up to 10 PCIe+ I/O drawers. This option is required when ordered with Balanced Power.

BPA support removal^a: Based on the direction of the market, the IBM z16 is planned to be the last IBM Z platform to support BPA. Customers should plan to migrate from BPA to Intelligent Power Distribution Unit (iPDU).

- a. Statements by IBM regarding its plans, directions, and intent are subject to change or withdrawal without notice at the sole discretion of IBM. Information regarding potential future products is intended to outline general product direction and should not be relied on in making a purchasing decision.

The IBM z16 operates with one or two sets of redundant power supplies. Each set has its own individual power cords or pair of power cords, depending on the number of Bulk Power Regulator (BPR) pairs that are installed. Power cords attach to a three-phase, 50/60 Hz, 200 - 480 V AC power source. The loss of one power supply per set has no effect on system operation.

The optional Balanced Power Plan Ahead feature is available for future growth, which also assures adequate and balanced power for all possible configurations. With this feature, downtime for upgrading a system is eliminated because the initial installation includes the maximum power requirements in terms of BPRs and power cords.

2.5.2 Cooling options

The IBM z16 cooling system is available only with the Radiator (air) cooling option. The previous water-cooling solution that was available with IBM z15 is not offered with IBM z16.

DCMs are always cooled with an internal water loop. The liquid in the internal water system is cooled by using an internal radiator. The radiator, PCIe+ I/O drawers, power enclosures, and CPC drawers are cooled by chilled air with blowers.

The air-cooling system in the IBM z16 is redesigned for better availability and lower cooling power consumption. The radiator design is a closed-loop water-cooling pump system for the DCMs in the CPC drawers. It is designed with N+1 pumps, blowers, controls, and sensors. The radiator unit is cooled by air.

2.5.3 Power considerations

Consider the following points about power:

- ▶ A total of 1 - 4 42U 19-inch IBM frames are used (replacing the two 24-inch frame).
- ▶ Air flow is front to rear. All blowers are mounted on the front of the frame.
- ▶ All external power cabling is at the rear of the frames (no power cabling in front).
- ▶ Top or bottom exit power is supported.
- ▶ A High-Voltage DC (HVDC) option is not available.
- ▶ No Emergency Power Off (EPO) switch is used.

Specific power requirements depend on the number of frames, CPC drawers, and type of I/O units that are installed, and the power option (PDU or BPA).

For more information about the maximum power consumption tables for the various configurations and environments, see *IBM 3931 Installation Manual for Physical Planning*, GC28-7015.

For more information about the power and weight estimation tool, see [IBM Resource Link®](#).



Supported features and functions

IBM Z features and functions that are supported on the IBM z16 are highlighted in this chapter. The information that is provided expands on the overview of the key hardware elements that are described in Chapter 1, “Enduring the pace of digital transformation with the IBM z16 server” on page 1, and Chapter 2, “IBM z16 hardware overview” on page 13.

For more information about the key capabilities and enhancements of the IBM z16, see *IBM z16 (3931) Technical Guide*, SG24-8951. For more information about the I/O features and functions, see *IBM Z Connectivity Handbook*, SG24-5444.

This chapter includes the following topics:

- ▶ 3.1, “IBM z16 I/O connectivity overview” on page 30
- ▶ 3.2, “Storage connectivity” on page 31
- ▶ 3.3, “Network connectivity” on page 34
- ▶ 3.4, “Clustering connectivity” on page 38
- ▶ 3.5, “*Server Time Protocol*” on page 39
- ▶ 3.6, “Cryptographic features” on page 41
- ▶ 3.7, “IBM Virtual Flash Memory” on page 43
- ▶ 3.8, “Hardware Management Console and Support Element” on page 44

3.1 IBM z16 I/O connectivity overview

The IBM z16 provides a Peripheral Component Interconnect Express (PCIe)-based infrastructure for the PCIe+ I/O drawers to support the following features:

- ▶ Storage connectivity:
 - zHyperLink Express1.1 (new build and carry forward)
 - zHyperLink Express (carry forward only)
 - FICON Express32S (new build only)
 - FICON Express16SA (carry forward only)
 - FICON Express16S+ (carry forward only)
- ▶ Network connectivity:
 - OSA-Express7S 1.2 (new build only)
 - OSA-Express7S (carry forward only)
 - OSA-Express6S (carry forward only)
 - RDMA over Converged Ethernet (RoCE) Express3 (new build only)
 - RoCE Express2.1 (carry forward only)
 - RoCE Express2 (carry forward only)
- ▶ Clustering connectivity:
 - ICA SR1.1 (new build or carry forward)
 - ICA Short Reach (SR) (carry forward only)
 - Coupling Express2 Long Reach (LR) (new build only)
- ▶ Cryptographic features:
 - Crypto Express8S, one or two hardware security modules (HSMs)¹ (new build only)
 - Crypto Express7S, 1-port, or 2-port² (carry forward only)
 - Crypto Express6S (carry forward only)

Detailed specifications for these features are provided in the subsequent sections.

The following features that were supported on earlier IBM Z platforms are *not* orderable and *cannot* be carried forward to the IBM z16:

- ▶ FICON Express16S
- ▶ FICON Express8S
- ▶ OSA-Express5S
- ▶ 10 GbE RoCE Express
- ▶ Crypto Express5S
- ▶ IBM zEnterprise Data Compression (zEDC)
- ▶ Coupling Express LR

Note: The LC Duplex connector type is used for all fiber optic cables, except the cables that are used for zHyperLink Express, and ICA SR connections, which have multi-fiber termination push-on (MTP) connectors.

¹ The Crypto Express8S is available with one or two HSMs. The HSM is the IBM 4770 Peripheral Component Interconnect Express Cryptographic Coprocessor (PCIeCC).

² The Crypto Express7S comes with one (1-port) or two (2-port) HSMs. The HSM is the IBM 4769 PCIe Cryptographic Coprocessor (PCIeCC).

3.2 Storage connectivity

The main focus for storage connectivity is to continuously improve the latency for I/O transmission. With the introduction of zHyperLink Express, IBM ensures the optimization of the I/O infrastructure. The FICON Express32S feature offers increased speed and supports similar functions as its predecessor (FICON Express16SA).

For more information about FICON channels, see the [IBM Z I/O connectivity web page](#).

Technical papers about performance data are also available.

Storage connectivity options are listed in Table 3-1.

Table 3-1 Storage connectivity features

Feature	Feature codes	Bit rate in Gbps (or stated)	Cable type	Maximum unrepeated distance	Ordering information IBM z16 A01
zHyperLink Express1.1	0451	8 (GBps)	OM3 and OM4	See Table 3-2	New build, carry forward
zHyperLink Express	0431				Carry forward
FICON Express32S LX	0461	8, 16, or 32	SM 9 μm	10 km ^a (6.2 miles)	New build
FICON Express32S SX	0462	8, 16, or 32	OM2, OM3, and OM4	See Table 3-2	New build
FICON Express16SA LX	0436	8 or 16	SM 9 μm	10 km (6.2 miles)	Carry forward
FICON Express16SA SX	0437	8 or 16	OM2, OM3, and OM4	See Table 3-3	Carry forward
FICON Express16S+ LX	0427	4, 8, or 16	SM 9 μm	10 km (6.2 miles)	Carry forward
FICON Express16S+ SX	0428	4, 8, or 16	OM2, OM3, and OM4	See Table 3-3	Carry forward

a. At 32 Gbps, distance to the first direct-connected device (other FICON adapter, SAN switch, storage device, WDM module, and so on) is limited to 5 km (3.1 miles).

3.2.1 zHyperLink Express

IBM zHyperLink Express is a short-distance IBM Z I/O adapter with up to 5x lower latency than High-Performance FICON for read requests. This feature is housed in the PCIe+ I/O drawer and is a two-port adapter that is used for short distances (direct connectivity between a IBM z15 and a DS8880 or newer). The zHyperLink Express is designed to support distances up to 150 meters (492 feet) at a link data rate of 8 GBps.

The maximum unrepeated distances for different multimode fiber optic cable types when used with zHyperLink Express are listed in Table 3-2.

Table 3-2 Unrepeated distances for multimode fiber optic cable types for zHyperLink Express

Cable type ^a (modal bandwidth)	8 Gbps
OM3 (50 µm at 2000 MHz-km)	100 meters (328 feet)
OM4 (50 µm at 4700 MHz-km)	150 meters (492 feet)

a. Fiber optic cable with 24 fibers (12 transmit plus 12 receive fibers) and MTP connectors.

A 24-fiber cable with MTP connectors is required for the ports of the zHyperLink Express feature. Internally, a single cable contains 12 fibers for transmit and 12 fibers for receive.

Note: FICON connectivity to each storage system is required. The FICON connection is used for zHyperLink initialization, I/O requests that are not eligible for zHyperLink communications, and as an alternative path if zHyperLink requests fail. For example, storage cache misses or busy storage device conditions can cause requests to fail.

3.2.2 FICON Express features

FICON Express features continue to evolve and deliver improved throughput, and reliability, availability, and serviceability (RAS). In the IBM z16, these features can provide connectivity to other systems, such as Fibre Channel (FC) switches and various devices in a SAN environment.

The FICON Express features are fully supported on the IBM z16. They are commonly used with IBM z/OS, IBM z/VM (and guest systems), Linux on IBM Z, IBM z/VSE, and IBM z/TPF.

The maximum unrepeated distances for different multimode fiber optic cable types when used with FICON SX (shortwave) features running at different bit rates are listed in Table 3-3.

Table 3-3 Unrepeated distances for multimode fiber optic cable types for FICON Express

Cable type (modal bandwidth)	2 Gbps	4 Gbps	8 Gbps	16 Gbps	32 Gbps
OM1 (62.5 µm at 200 MHz-km)	150 meters	70 meters	21 meters	N/A	N/A
	492 feet	230 feet	69 feet	N/A	N/A
OM2 (50 µm at 500 MHz-km)	300 meters	150 meters	50 meters	35 meters	20 meters
	984 feet	492 feet	164 feet	115 feet	65 feet
OM3 (50 µm at 2000 MHz-km)	500 meters	380 meters	150 meters	100 meters	70 meters
	1640 feet	1247 feet	492 feet	328 feet	229 feet
OM4 (50 µm at 4700 MHz-km)	N/A	400 meters	190 meters	125 meters	100 meters
	N/A	1312 feet	623 feet	410 feet	328 feet

IBM Fibre Channel Endpoint Security

IBM Fibre Channel Endpoint Security was first introduced with IBM z15 for FICON Express16SA features (Feature Code 0436 and Feature Code 0437). FICON Express32S features (Feature Code 0461 and Feature Code 0462) also provide support for IBM Fibre Channel Endpoint Security, together with Endpoint Security Enablement (Feature Code 1142). This capability adds Fibre Channel Endpoint Authentication and Encryption of Data in Flight for FICON and FC connections to IBM DS8000 storage systems.

Based tightly on the Fibre Channel–Security Protocol-2 (FC-SP-2) standard, which provides various means of authentication and essentially maps IKEv2 constructs for security association management and derivation of encryption keys to Fibre Channel Extended Link Services, the IBM Fibre Channel Endpoint Security implementation uses the IBM solution for key server infrastructure in the storage system (for data at rest encryption).

[IBM Security™ Guardium® Key Lifecycle Manager](#) server provides shared secret key generation in a master-subordinate relationship between an FC initiator (IBM Z) and the storage target. The solution implements authentication and key management called *IBM Secure Key Exchange (SKE)*.

Data that is in-flight (from or to IBM Z and IBM Storage) is encrypted when it leaves either endpoint (source) and is then decrypted at the destination. Encryption and decryption are done at the FC adapter level.

In endpoint security-related operations, the operating system that runs on the IBM Z platform is not involved. Tools are provided at the operating system level for displaying information about encryption status.

IBM Fibre Channel Endpoint Security is an orderable feature for IBM z16 (Feature Code 1146) and requires Central Processor Assist for Cryptographic Functions (CPACF) enablement (Feature Code 3863), specific storage (DS8900), and FICON Express32S features.

For more information and implementation details, see the [IBM Fibre Channel Endpoint Security for IBM z15 and LinuxONE III Announcement Letter](#).

3.3 Network connectivity

The IBM z16 offers a wide range of functions that can help consolidate or simplify the network environment. These functions are supported by HiperSockets, OSA-Express features, Shared Memory Communications (SMC), and RoCE Express features.

3.3.1 HiperSockets

IBM HiperSockets are referred to as the “network in a box” because it simulates local area network (LAN) environments entirely within the IBM Z platform. The data transfer is from logical partition (LPAR) memory to LPAR memory, which is mediated by IBM Z firmware.

The IBM z16 supports up to 32 HiperSockets. One HiperSockets network can be shared by up to 85 LPARs. Up to 4096 communication paths support a total of 12,288 IP addresses across all 32 HiperSockets.

The HiperSockets internal networks can support the following transport modes:

- ▶ Layer 2 (link layer)
- ▶ Layer 3 (network or IP layer)

Traffic can be Internet Protocol Version 4 (IPv4) or Version 6 (IPv6) or non-IP traffic. HiperSockets devices are independent of protocol and Layer 3. Each HiperSockets device has its own Layer 2 Media Access Control (MAC) address. This address is designed to allow the use of applications that depend on the existence of Layer 2 addresses, such as Dynamic Host Configuration Protocol (DHCP) servers and firewalls.

Layer 2 support can help facilitate server consolidation. Complexity can be reduced, network configuration is simplified and intuitive, and LAN administrators can configure and maintain the IBM Z environment the same way as they do for a non-IBM Z environment. HiperSockets Layer 2 support is provided by Linux on IBM Z, and by z/VM for guest use.

3.3.2 OSA-Express features

OSA-Express features achieve high levels of throughput (mixed inbound/outbound) by using a data router function. The data router enables a direct host memory-to-LAN flow. This function is designed to reduce latency and increase throughput for standard Ethernet frames (1492 bytes) and jumbo frames (8992 bytes).

3.3.3 Shared Memory Communications

The SMC capabilities of the IBM z16 optimize the communications between applications in server to server (SMC-R) or LPAR-to-LPAR (SMC-D) connectivity. With IBM z16, SMC is supported between z/OS LPARs, Linux on IBM Z LPARs, and AIX® (running on Power Systems).

SMC is available in z/OS V2R4 (with program-temporary fixes [PTFs]) and z/OS V2R5. The initial version of SMC was limited to TCP/IP connections over the same layer 2 network; therefore, it was not routable across multiple IP subnets.

SMC Version 2 (SMCv2) supports SMC over multiple IP subnets for SMC-D and SMC-R and is referred to as SMC-Dv2 and SMC-Rv2. SMCv2 requires updates to the underlying network technology. SMC-Dv2 requires ISMv2 and SMC-Rv2 requires RoCEv2.

The SMCv2 protocol is downward compatible and allows SMCv2 hosts to continue to communicate with SMCv1 previous hosts.

SMC-R provides application-transparent use of the RoCE Express features that can reduce the network overhead and latency of data transfers, which effectively offers the benefits of optimized network performance across processors.

The Internal Shared Memory (ISM) virtual Peripheral Component Express (PCI) function uses the capabilities of SMC-D. ISM is a virtual PCI network adapter that enables direct access to shared virtual memory, which provides a highly optimized network interconnect for IBM Z intra-system communications. Up to 32 channels for SMC-D traffic can be defined in an IBM z16, whereby each channel can be virtualized to a maximum of 255 Function IDs³. No other hardware is required for SMC-D.

3.3.4 RoCE Express features

The RoCE Express features help reduce the use of CPU resources for applications that use the TCP/IP stack. It might also help to reduce network latency with memory-to-memory transfers that use SMC-R in z/OS environments. It is transparent to applications, and can be used for system-to-system communication in a multiple IBM Z platform environment.

These features are installed in the PCIe+ I/O drawer and use an SR optical transceiver. Point-to-point connections and switched connections with an Ethernet switch are supported. Ethernet switches must include enablement of the *Pause frame* as defined by the IEEE 802.3x standard.

Depending on the RoCE Express feature type, a maximum of 16 or 8 RoCE Express features can be installed in the IBM z16 in any combination.

Note: The 10 GbE and 25 GbE RoCE Express3 LR are new with IBM z16. Previous RoCE generations supported SR connectivity only.

The 25 GbE RoCE Express must not be mixed with any type of 10 GbE RoCE Express in the same SMC-R link group. The 10 GbE RoCE Express adapters can be mixed in any combination in the same SMC-R link group.

³ The 10 GbE RoCE features and the ISM adapters are identified by a hexadecimal Function Identifier (FID) with a range of 00 - FF.

The network connectivity options are listed in Table 3-4.

Table 3-4 Network connectivity features

Feature	Feature code	Bit rate in Gbps (or stated)	Cable type	Maximum unrepeated distance ^a	Ordering information IBM z16 A01
OSA-Express7S 1.2 25-GbE LR	0460	25	SM 9 µm	10 km (6.2 miles)	New build
OSA-Express7S 1.2 25-GbE SR	0459		MM 50 µm	70 m (2000) 100 m (4700)	
OSA-Express7S 1.2 10-GbE LR	0456	10	SM 9 µm	10 km (6.2 miles)	New build
OSA-Express7S 1.2 10 GbE SR	0457		MM 62.5 µm MM 50 µm	33 m (200) 82 m (500) 300 m (2000)	
OSA-Express7S 1.2 GbE LX	0454	1.25	SM 9 µm	5 km (3.1 miles)	
OSA-Express7S 1.2 GbE SX	0455		MM 62.5 µm MM 50 µm	275 m (200) 550 m (500)	
OSA-Express7S 1.2 1000BASE-T	0458	1000 Mbps	Cat 5 or 6 UTP	100 m (328 feet)	
OSA-Express7S 25 GbE SR1.1	0449	25	MM 50 µm	70 m (2000) 100 m (4700)	Carry forward
OSA-Express7S 25 GbE SR	0429				
OSA-Express7S 10 GbE LR	0444	10	SM 9 µm	10 km (6.2 miles)	Carry forward
OSA-Express6S 10 GbE LR	0424				
OSA-Express5S 10 GbE LR	0415				
OSA-Express7S 10 GbE SR	0445	10	MM 62.5 µm MM 50 µm	33 m (200) 82 m (500) 300 m (2000)	Carry forward
OSA-Express6S 10 GbE SR	0425				
OSA-Express7S GbE LX	0442	1.25	SM 9 µm	5 km (3.1 miles)	Carry forward
OSA-Express6S GbE LX	0422				
OSA-Express7S GbE SX	0443	1.25	MM 62.5 µm MM 50 µm	275 m (200) 550 m (500)	Carry forward
OSA-Express6S GbE SX	0423				
OSA-Express7S 1000BASE-T	0446	1000 Mbps	Cat 5 or 6 UTP	100 m	Carry forward
OSA-Express6S 1000BASE-T	0426	100 or 1000 Mbps			

Feature	Feature code	Bit rate in Gbps (or stated)	Cable type	Maximum unrepeated distance ^a	Ordering information IBM z16 A01
25 GbE RoCE Express3 LR	0453	25	SM 9 µm	10 km (6.2 miles)	New build
25 GbE RoCE Express3 SR	0452		MM 50 µm	70 m (2000) 100 m (4700)	
10 GbE RoCE Express3 LR	0441	10	SM 9 µm	10 km (6.2 miles)	New build
10 GbE RoCE Express3 SR	0440		MM 62.5 µm MM 50 µm	33 m (200) 82 m (500) 300 m (2000)	
25 GbE RoCE Express2.1	0450	25	MM 50 µm	70 m (2000) 100 m (4700)	Carry forward
25 GbE RoCE Express2	0430				
10 GbE RoCE Express2.1	0432	10	MM 62.5 µm MM 50 µm	33 m (200) 82 m (500) 300 m (2000)	Carry forward
10 GbE RoCE Express2	0412				

a. The minimum fiber bandwidth distance in MHz-km for multi-mode fiber optic links is included in parentheses, where applicable.

3.4 Clustering connectivity

Parallel Sysplex is a clustering technology with which you can operate multiple copies of z/OS images as a single system from a user's perspective. A suitably configured Parallel Sysplex can achieve near-continuous availability. The component that enables this parallelism is the Coupling Facility (CF), which can run as a separate LPAR (internal CF) or within dedicated hardware (external CF).

What makes a group of such z/OS images into a sysplex is the inter-communication. This inter-communication is handled through coupling links. Coupling links enable all of the z/OS-to-CF communication, CF-to-CF traffic, or Server Time Protocol (STP)⁴.

For more information about coupling links technologies, see the [Coupling Facility Configuration Options](#) white paper.

Internal coupling (IC) links are used for internal communication between LPARs on the same system that is running CFs and z/OS images. The connection is emulated in Licensed Internal Code (LIC) and provides for fast and secure memory-to-memory communications between LPARs within a single system. No physical cabling is required.

Coupling Facility Control Code (CFCC) level 25 is available for the IBM z16. For more information, see the [IBM Documentation web page](#).

Coupling link options are listed in Table 3-5.

Table 3-5 Coupling link features

Feature	Feature code	Bit rate	Cable type	Maximum unrepeated distance	Ordering information
Coupling Express2 LR (CE LR)	0434	10 Gbps	SM 9 µm	10 km (6.2 miles)	New build
ICA SR 1.1	0176	8 GBps	OM3 ^a and OM4 ^a	150 m 100 m	New build or carry forward
ICA SR	0172				Carry forward
IC	No coupling link feature or fiber optic cable is required.				

a. A fiber optic cable with 24 fibers (12 transmit plus 12 receive fibers) and MTP connectors.

3.4.1 Dynamic I/O configuration for stand-alone CFs

Dynamic I/O configuration changes can be made to a stand-alone CF⁵ without requiring a disruptive power on reset.

A separate LPAR with a firmware-based appliance that contains an activation service instance is used to apply I/O configuration changes to the stand-alone CF dynamically. The firmware-based LPAR is driven by updates from an HCD instance that is running in a z/OS LPAR on a different IBM Z that is connected to the same Hardware Management Console (HMC).

The firmware LPAR is defined in the range of IBM reserved LPARs and does not support any attached I/O. That is, it does not take away any of your configurable resources.

⁴ All external coupling links can be used to carry STP timekeeping information.

⁵ A stand-alone CF does not have any running instances of z/OS or z/VM.

3.5 Server Time Protocol

STP is a message-based protocol in which timekeeping information is passed over coupling links between IBM Z platforms. The IBM z16 can participate in an STP Coordinated Timing Network (CTN). A CTN is a collection of IBM Z platforms that are time-synchronized to a time value that is called *Coordinated Server Time* (CST).

STP is implemented in LIC as a system-wide facility of the IBM z16 and other IBM Z platforms. The IBM z16 is enabled for STP by installing the STP feature code. Extra configuration is required for an IBM z16 to become a member of a CTN.

For high availability (HA) purposes, nondisruptive capability was implemented in the IBM z16 firmware that allows two CTNs to be merged into one, or to split one CTN into two, dynamically.

STP supports a multi-site timing network of up to 100 km (62 miles) over fiber optic cabling, without requiring an intermediate site. This protocol allows a Parallel Sysplex to span these distances for a multi-site Parallel Sysplex.

Note: If an IBM z16 plays a CTN role (Primary Time Server [PTS], Backup Time Server [BTS], or Arbiter), the other CTN roleplaying IBM Z platforms must include direct coupling connectivity to the IBM z16.

3.5.1 Changes to the STP implementation in the IBM z16

The following significant changes were made to the STP implementation on the IBM z16 over prior IBM Z models:

- ▶ Direct network connection to the IBM z16 CPC drawer of the External Time Source (ETS)
ETS (for Network Time Protocol [NTP] and Precision Time Protocol [PTP] network cables) now connects directly to the IBM z16 central processor complex (CPC) drawers. This connection provides greater accuracy to the external time signal.
- ▶ n-mode Power STP Imminent Disruption Signal option

On IBM Z, losing a PTS results in significant consequences to the timing network and the overall workload execution environment of the IBM Z sysplex.

Because an integrated battery facility no longer exists, support was added to the CPC to support n-mode power conditions (wall power or power cord loss). If a power condition is detected, an automated failover occurs to the BTS. The requirement for the backup power method is to hold power for 60 seconds on the PTS to allow failover to successfully complete.

HMC System Events are available for awareness through user interface or automation.

3.5.2 Network Time Protocol client support

The use of NTP servers as an ETS usually fulfills a requirement for a time source or common time reference across heterogeneous platforms. This approach also provides greater time accuracy.

NTP client support is available in the ETS/STP partition running on the IBM z16. The code interfaces with the NTP servers. This interaction allows an NTP server to become the single-time source for IBM z16 and for other servers that have NTP clients. The NTP Ethernet cable must plug directly into the Base Management Card (BMC)/Oscillator Card (OSC) ports on the IBM z16. Redundant cabling and ETS must be configured.

3.5.3 Precision Time Protocol client support

3.5.4 IEEE 1588 PTP is implemented on the IBM z16 as an ETS for a CTN. The PTP Ethernet cable must plug directly into the BMC/OSC ports on the IBM z16. Redundant cabling and ETS should be configured. **Pulse per second support**

Two OSCs⁶, which are included as a standard feature of the IBM z16, provide a dual-path interface for the pulse per second (PPS) signal. The cards contain a Bayonet Neill-Concelman (BNC) connector for PPS attachment at the front side of the CPC drawer. The redundant design allows continuous operation during the failure of one card and concurrent card maintenance.

STP tracks the highly stable and accurate PPS signal from the external time server. PPS maintains accuracy of 10 µs as measured at the PPS input of the IBM z16.

A cable connection from the PPS port to the PPS output of an NTP server is required when the IBM z16 is configured for NTP with PPS as ETS for time synchronization.

PPS is optional for PTP, but might still be required for NTP to meet Financial Regulations.

For more information, see *IBM z16 (3931) Technical Guide*, SG24-8951, and *IBM Z Server Time Protocol Guide*, SG24-8480.

⁶ The OSCs are combined with the BMCs.

3.6 Cryptographic features

The IBM z16 provides cryptographic functions that can be categorized in the following groups from an application program perspective:

- ▶ Symmetric and asymmetric⁷ cryptographic functions, which are provided by the CPACF or the Crypto Express features when defined as an accelerator.
- ▶ Asymmetric cryptographic functions, which are provided by the Crypto Express features.

3.6.1 Central Processor Assist for Cryptographic Functions

The CPACF enablement feature (3863) offers a set of symmetric cryptographic functions for high-performance encryption and decryption with clear key operations for SSL/TLS, VPN, and data-storing applications that do not require Federal Information Processing Standards (FIPS) 140-2 Level 4 security⁸. The CPACF is a no-charge optional feature that is integrated with the compression unit in the coprocessor in the IBM z16 microprocessor core.

The CPACF protected key is a function that facilitates the continued privacy of cryptographic key material while keeping the wanted high performance. CPACF ensures that key material is not visible to applications or operating systems during encryption operations. CPACF protected key provides substantial throughput improvements for large-volume data encryption and low latency for encryption of small blocks of data.

The cryptographic assist includes support for the following functions:

- ▶ Advanced Encryption Standard (AES) for 128-bit, 192-bit, and 256-bit keys
- ▶ Improved performance of AES GCM (Galois/Counter Mode) encryption
- ▶ Data Encryption Standard (DES) data encryption and decryption with single, double, or triple length keys
- ▶ Pseudo-random number generation (PRNG)
- ▶ Deterministic Random Number Generation (DRNG)
- ▶ True-random number generator (TRNG)
- ▶ Message authentication code
- ▶ Message-Security-Assist extension 9
- ▶ Elliptic Curve Cryptography (ECC) support
- ▶ Hashing algorithms: Secure Hash Algorithm (SHA)-1, SHA-2, and SHA-3

SHA-1, SHA-2, and SHA-3 support are enabled on all IBM Z platforms and do not require the CPACF enablement feature. The CPACF functions are supported by z/OS, z/VM, z/VSE, z/TPF, and Linux on IBM Z.

3.6.2 Crypto Express8S

The Crypto Express8S represents the newest generation of the Peripheral Component Interconnect® Express (PCIe) cryptographic co-processors, which are an optional feature that is available on the IBM z16. These co processors are hardware security modules (HSMs) that provide high-security cryptographic processing as required by banking and other industries.

⁷ Elliptic Curve Cryptography (ECC) algorithms.

⁸ FIPS 140-3 Security Requirements for Cryptographic Modules.

The Crypto Express8S provides quantum-safe APIs that enable you to begin the use of quantum-safe cryptography along with classical cryptography as existing applications are modernized and new applications are built.

This feature provides a secure programming and hardware environment wherein crypto-processes are performed. Each cryptographic coprocessor includes general-purpose processors, nonvolatile storage, and specialized cryptographic electronics. All of these features are contained within a tamper-sensing and tamper-responsive enclosure that eliminates all keys and sensitive data on any attempt to tamper with the device. The security features of the HSM are designed to meet the requirements of FIPS 140-2 Level 4.

The Crypto Express8S (2-port) feature (0908) includes two Peripheral Component Interconnect Express Cryptographic Coprocessors (PCIeCCs), and the Crypto Express8S (1-port) feature (0909) includes one PCIeCC. For availability reasons, a minimum of two features is required for the one-port feature. Up to 30 Crypto Express8S (2-port) features are supported on IBM z16. The maximum number of the 1-port features is 16. The Crypto Express8S feature occupies one I/O slot in a PCIe+ I/O drawer.

Each adapter can be configured as a Secure IBM Common Cryptographic Architecture (CCA) coprocessor, a Secure IBM Enterprise PKCS #11 (EP11) coprocessor, or as an accelerator.

Crypto Express8S provides domain support for up to 85 LPARs.

The accelerator function is designed for maximum-speed Secure Sockets Layer and Transport Layer Security (SSL/TLS) acceleration, rather than for specialized financial applications for secure, long-term storage of keys or secrets. The Crypto Express8S can also be configured as one of the following configurations:

- ▶ The Secure IBM CCA coprocessor includes secure key functions with emphasis on the specialized functions that are required for banking and payment card systems. It is optionally programmable to add custom functions and algorithms by using User Defined-Extensions (UDXs).

A new mode, called *Payment Card Industry PTS HSM* (PCI-HSM), is available in CCA mode. PCI-HSM mode simplifies compliance with Payment Card Industry requirements for HSMs.

- ▶ The Secure IBM EP11 coprocessor implements an industry-standardized set of services that adheres to the PKCS #11 specification v2.20 and more recent amendments. It was designed for extended FIPS and Common Criteria evaluations to meet industry requirements.

This cryptographic coprocessor mode introduced the PKCS #11 secure key function.

When the Crypto Express8S PCIe adapter is configured as a secure IBM CCA coprocessor, it still provides accelerator functions. However, up to 3x better performance for those functions can be achieved if the Crypto Express8S PCIe adapter is configured as an accelerator.

CCA enhancements include the ability to use triple-length (192-bit) Triple Data Encryption Standard (TDES) keys for operations, such as data encryption, PIN® processing, and key wrapping to strengthen security. CCA also extended the support for the cryptographic requirements of the German Banking Industry Committee, Deutsche Kreditwirtschaft, and quantum-safe cryptography.

Several features that support the use of the AES algorithm in banking applications also were added to CCA. These features include the addition of AES-related key management features and the AES ISO Format 4 (ISO-4) PIN blocks as defined in the ISO 9564-1 standard. PIN block conversion is supported and use of AES PIN blocks in other CCA callable services. IBM continues to add enhancements as AES finance industry standards are released.

3.6.3 Crypto Express7S and Crypto Express6S (carry forward only)

The Crypto Express7S feature has one or two PCIeCC (HSM) per feature (Feature Code 0898 has 2-port; Feature Code 0899 has 1-port) and Crypto Express6S feature (0893) has one PCIeCC (HSM) per feature. For availability reasons, a minimum of two features is required. Up to 16 Crypto Express7S or Crypto Express6S features are supported.

Each adapter can be configured as a Secure IBM CCA coprocessor, a Secure IBM EP11 coprocessor, or as an accelerator.

Crypto Express7S and Crypto Express6S provide domain support for up to 85 LPARs on IBM z16.

Trusted Key Entry (TKE) feature: The TKE Workstation feature is required to support the administration of the Crypto Express features when configured as an Enterprise PKCS #11 coprocessor or managing the CCA mode PCI-HSM.

3.7 IBM Virtual Flash Memory

IBM Virtual Flash Memory (VFM) is the replacement for the Flash Express features that were available on earlier IBM Z platforms. With IBM z16, the VFM feature (0644) can be ordered in 512 GB increments up to 12 VFM features for a total of 6 TB.

VFM is designed to help improve availability and handling of paging workload spikes. With this support, z/OS is designed to help improve system availability and responsiveness by using VFM across transitional workload events.

VFM also can be used in CF images to provide extended capacity and availability for workloads that use IBM MQ shared queues. The use of VFM can help availability by reducing latency from paging delays that can occur at the start of the workday or during other transitional periods. It is also designed to eliminate delays that can occur when diagnostic data is collected during failures.

Therefore, VFM can help meet most demanding service level agreements and compete more effectively. VFM is easy to configure and provides rapid time to value.

3.8 Hardware Management Console and Support Element

The HMC and Support Element (SE) are appliances that provide hardware management for IBM Z platforms. Hardware platform management covers a complex set of configuration, operation, monitoring, and service management tasks, and other services that are essential to the operations of the IBM Z platform.

The minimum driver level for HMC and SE for IBM z16 is Driver 51. Driver 51 is equivalent to Version 2.16.0.

Note: The HMC with Driver 51/Version 2.16.0 can manage N-2 generations of IBM Z platforms (IBM z16, IBM z15, and IBM z14).

On IBM z16, two HMCs are delivered with the Hardware Management Appliance (HMA) feature (Feature Code 0129). It is possible to order the HMA feature later. However, only new microcode is delivered without HMC hardware.

Note: The HMC code runs on the two integrated 1U rack-mounted servers on the top of the IBM z16 A frame. Standalone that is outside the IBM z16 HMCs (Tower or Rack Mount) can no longer be ordered.

HMC feature codes (Feature Code 0062, Feature Code 0063, Feature Code 0082, and Feature Code 0083) can be carried forward from previous orders and Driver 51/Version 2.16.0 can be installed to support IBM z16.

Also, Driver 51/Version 2.16.0 can be installed on the two HMCs that are provided with the HMA feature (Feature Code 0100) on IBM z15. The SEs and HMCs are closed systems; therefore, no other applications can be installed on them.

With IBM z16 and HMA, the SE code runs virtualized on the integrated two HMCs on the two integrated 1U rack-mounted servers on the top of the IBM z16 A frame. One SE is the Primary SE (active) and the other is the Alternative SE (backup).

The SEs are connected to Ethernet switches for network connectivity with the IBM Z platform and the HMCs. An HMC can communicate with one or more IBM Z platforms.

When tasks are performed on the HMC, the commands are sent to one or more SEs, which then issue commands to their respective CPCs.

The HMC Remote Support Facility (RSF) provides communication with the IBM support network for hardware problem reporting and service.



IBM z16 system design strengths

Every new generation of the IBM Z platform introduces innovative features and functions to provide more velocity, security, agility, and flexibility for building IT solutions and services.

The IBM Z hardware, firmware, and operating systems always conform to the IBM z/Architecture¹ to ensure support of current and future workloads and services. Whenever new capabilities are implemented, the z/Architecture is extended rather than replaced. This practice helps sustain the compatibility, integrity, and longevity of the IBM Z platform. Thus, protection with an earlier version of workloads and solutions is ensured.

The evolution of the IBM Z platform embodies a proven architecture that is open, secure, resilient, and adaptable. From their microprocessor and memory design to their artificial intelligence (AI), sort, and cryptography capabilities, unparalleled I/O throughput, and rich virtualization, the IBM z16 is built to respond with speed and versatility.

This chapter introduces the IBM z16 system design capabilities and enhancements and includes the following topics:

- ▶ 4.1, “Technology improvements” on page 46
- ▶ 4.2, “Virtualization” on page 50
- ▶ 4.3, “Capacity and performance” on page 57
- ▶ 4.4, “Reliability, availability, and serviceability” on page 63
- ▶ 4.5, “High availability with Parallel Sysplex” on page 66
- ▶ 4.6, “Pervasive encryption” on page 70
- ▶ 4.7, “Quantum-safe technology” on page 74

¹ IBM z/Architecture is the mainframe-computational architecture notation that defines its behavior. For more information, see:

<https://www-05.ibm.com/e-business/linkweb/publications/servlet/pbi.wss?CTY=US&FNC=SRX&PBL=SA22-7832-12>

4.1 Technology improvements

Systems achieve the levels of efficiency that are needed by businesses through an overall balanced design. Processor units (PUs), memory, I/O, and network communications must complement each other to achieve the required levels of performance. Hence, you can have the fastest processors that are available, but your workloads suffer if you cannot feed them.

A balanced system design also incorporates all the enhancements in software, hardware, and firmware to allow you to accelerate specific type of operations; for example, sorting, inferencing, compressing, and encrypting data.

IBM z16 provides high levels of performance, scalability, resiliency, flexibility, and security when serving as a traditional IBM Z platform, a cloud platform, or both. The IBM z16 can host thousands of virtualized environments.

4.1.1 System capacity

Each generation of IBM Z platforms provides more system capacity, which combines various system design enhancements. The IBM z16 with the Max200 feature is designed to offer up to 25% more processing capacity than the previous IBM z15 Model T01. The maximum number of configurable cores also increased from 190 with the IBM z15 T01 to 200 with the IBM z16 A01.

The family of Capacity-on-Demand offerings ensures a flexible addition of capacity when it is most needed; for example, during peak workload periods, scheduled maintenance, or in disaster recovery (DR) scenarios. For more information, see 4.3.2, “Capacity on-Demand offerings” on page 58.

4.1.2 Processor design highlights

The IBM z16 supports 64-bit addressing mode and uses Complex Instruction Set Computer (CISC), including highly capable and complex instructions. Most of the instructions are implemented at the hardware or firmware level for most optimal and effective execution.

PU is the generic term for the z/Architecture CPU. Each PU is a superscalar processor, which can decode up to six complex instructions per clock cycle, running instructions out-of-order. The PU uses a high-frequency, low-latency pipeline that provides robust performance across a wide range of workloads.

z/Architecture addressing modes: The z/Architecture simultaneously supports 24-bit, 31-bit, and 64-bit addressing modes. This feature delivers compatibility with earlier software versions, which in turn provides investment protection.

Compared to its predecessors, the IBM z16 features the following processor design changes, improvements, and architectural extensions:

- ▶ Redesigned processor chip, 7 nm silicon wafer technology
- ▶ New cache structure:
 - L1D(ata) and L1I(nstruction) cache: ON-core
 - L2 - dense SRAM: Outside the core, semi-private to the core
 - Virtual L3 cache (shared victim) = 256 MB
 - Virtual L4 cache (shared victim) = 2 GB

- ▶ New Core-Nest Interface
- ▶ Brand new branch prediction design that uses SRAM
- ▶ Significant architecture changes – COBOL compiler and more
- ▶ Dedicated coprocessors and accelerators for each PU (core):
 - The Central Processor Assist for Cryptographic Functions (CPACF) is for encrypting large amounts of data in real time. With IBM z16, CPACF provides counters that track cryptographic compliance and instruction use, algorithms, bit length, and key security for a specific workload.
CPACF supports Data Encryption Standard (DES), Triple Data Encryption Standard (TDES), AES-128, and AES-256 for data privacy and confidentiality. For data integrity, CPACF supports Secure Hash Algorithm (SHA)-1, SHA-2, SHA-3, and SHAKE. CPACF supports Pseudo Random Number Generation, Deterministic Random Number Generation (DRNG), and True Random Number Generation for key generation.
In addition, CPACF supports Elliptic Curve Cryptography (ECC) clear key, improving the performance of Elliptic Curve algorithms. EdDSA (Ed448, Ed25519), ECDSA (P-256, P-384, P-521), ECDH (P-256, P-384, P521, X25519, X448), and protected key signature creation are also supported.
 - IBM Integrated Accelerator for Artificial Intelligence (AIU)
This on-chip AIU is designed for high-speed, real-time inferencing at scale. The on-chip AI acceleration adds more than 6 TFLOPS of processing power that is shared by all cores on the chip.
This centralized AI design provides high performance and consistent low latency inferencing for processing a mix of transactional and AI workloads at speed and scale.
A robust system of frameworks and open source tools, combined with the new IBM Deep Learning Compiler that generates inferencing programs that are highly optimized for the IBM Z architecture and the AIU, help enable rapid development and deployment of deep learning and machine learning models on IBM Z to accelerate time to market.
For more information see [IBM Telum processor: the next-gen microprocessor for IBM Z and IBM LinuxONE](#)
 - IBM Integrated Accelerator for z Enterprise Data Compression
This on-chip accelerator for compression implements compression as defined by [RFC1951 \(DEFLATE\)](#). It allows you to perform data compression with the improved performance and simplified management on a processor chip level. The on-chip compression is designed to reduce the penalty of storing, transporting, and processing data without changing applications architecture.
 - IBM Integrated Accelerator for IBM Z Sort
This on-chip accelerator for sort uses the sort instruction (SORTL) instruction to accelerate the sorting of data. The IBM Integrated Accelerator for IBM Z Sort feature (ZSORT) helps reduce the CPU costs and improve the elapsed time for eligible workloads by speeding up sorting process and improving database functions.
For more information, see this [IBM Documentation web page](#).

Neural Network Processing Assist instruction

In support of the IBM Z AIU, a new memory-to-memory CISC instruction is used to operate directly on tensor objects that are in client application program memory. AI functions and macros are abstracted by way of Neural Network Processing Assist (NNPA).

The integrated AI accelerator delivers more than 6 TFLOPs per chip and over 200 TFLOPs in the 32-chip system. The AI accelerator is shared by all cores on the chip. The firmware, running on the cores and accelerator, orchestrates and synchronizes the execution on the accelerator.

Guarded Storage Facility

Guarded Storage Facility (GSF) is a hardware feature that Java uses to achieve pause-less garbage collection. GSF was introduced to enable enterprise scale Java applications to run without an extended pause for garbage collection on larger heaps. This facility improves Java performance by reducing program pauses during Java garbage collection.

Simultaneous multithreading

Simultaneous multithreading (SMT) is built into the IBM z16 Integrated Facilities for Linux (IFLs), IBM Z Integrated Information Processors (zIIPs), and System Assist Processors (SAPs). It allows more than one thread to simultaneously run in the same core and share all of its resources. This function improves the use of the cores and increases processing capacity.

When a program accesses a memory location that is not in the cache, it is called a *cache miss*. Because the processor must then wait for the data to be fetched before it can continue to run, cache misses affect the performance and capacity of the core to run instructions. By using SMT, when one thread in the core is waiting (such as for data to be fetched from the next cache levels or from main memory), the second thread in the core can use the shared resources rather than remain idle.

Hardware decimal floating point function

The hardware decimal floating point (HDFP) function is designed to speed up calculations and provide the precision that is demanded by financial institutions and others. The HDFP fully implements the IEEE 754r standard.

Vector Packed Decimal Facility

Vector Packed Decimal Facility allows packed decimal operations to be performed in registers rather than in memory by using new fast mathematical computations. Compilers, such as Enterprise COBOL for z/OS V6.2, Enterprise PL/I for z/OS V5.2, and IBM XL C/C++ V2.5 for z/OS V2R5, are optimized on IBM z16.

Single-instruction, multiple-data

The IBM z16 includes a set of instructions that is called *single-instruction, multiple-data* (SIMD) that can improve the performance of complex mathematical models and analytics workloads. This improvement is realized through vector processing and complex instructions that can process a large volume of data by using a single instruction.

SIMD is designed for parallel computing and can accelerate code that contains integer, string, character, and floating-point data types. This system enables better consolidation of analytics workloads and business transactions on the IBM Z platform.

Runtime Instrumentation Facility

The Runtime Instrumentation Facility provides managed run times and just-in-time compilers with enhanced feedback about application behavior. This capability allows dynamic optimization of code generation as it is being run.

Secure Execution for Linux

Secure Execution for Linux isolates and protects Kernel-based Virtual Machine (KVM) guests from hypervisor access. The Hypervisor administrator can still manage and deploy workloads, but is unable to view data on a guest. Multiple tenants (applications) running in logical partition (LPAR) as second-level guests under KVM have fully isolated environments helps protect intellectual property and proprietary secrets.

4.1.3 Memory

System memory is one of the core design components. Its continuous enhancements contribute to the overall system performance improvements.

Maximum physical memory size is directly related to the number of central processor complex (CPC) drawers in the system. An IBM Z platform has more memory that is installed than was ordered because a portion of the installed memory is used to implement the redundant array of independent memory (RAIM) design (the technology that provides memory protection and excludes memory faults). You are *not* charged for the extra amount of memory that is needed for RAIM.

For example, with the IBM z16, up to 40 TB of memory is for a four-CPC drawer configuration (25% increase per drawer compared to IBM z15).

Hardware system area (HSA) is 256 GB (same as IBM z15). The HSA area is a fixed size and is not included in the memory that is ordered.

Important: z/OS V2R3 and later releases require a minimum of 8 GB of memory (2 GB of memory when running under z/VM). z/OS V2R5 can support up to 16 TB of memory in an LPAR.

Each operating system can allocate the amount of main memory up to the supported limit. The amount of incremental memory is 1 GB with the IBM z16.

Flexible memory

Flexible memory provides the extra physical memory that is needed to support the following scenario: You need activation base memory and HSA on an IBM z16 that has multiple CPC drawers and one CPC drawer that is out of service.

On IBM z16, the extra resources that are required for flexible memory configurations are provided when you configure memory features and memory entitlement. Flexible memory ranges 512 GB - 30464 GB, depending on the feature ordered (Max82, Max125, Max168, and Max200).

Virtual Flash Memory

The Virtual Flash Memory (VFM) feature is offered from the main memory capacity. For IBM z16, up to 12 VFM features can be ordered, each being 512 GB.

VFM can improve availability by reducing latency from paging delays that can occur during peak workload periods. It is also designed to help eliminate delays that can occur when diagnostic data is collected during failures.

VFM also can be used in Coupling Facility (CF) images to provide extended capacity and availability for workloads that use IBM MQ Shared Queues structures.

4.2 Virtualization

Virtualization is a key strength of IBM Z, which is embedded in the hardware, firmware, and operating systems. It virtualizes all the computing resources (such as CPU, memory, and I/O). Each set of the resources can be used independently within separate operating environments (known as *guest systems*).

IBM Z is designed to concurrently run multiple virtual guest systems, providing each system with the required dynamic sharing of the resources with minimal costs and performance overhead.

LPAR technology was introduced more than three decades ago on the IBM Z platform to support virtualization and provide the highest level of isolation between guest systems.

Virtualization management, which is called a *hypervisor*, operates on hardware and software levels on IBM Z. The hardware hypervisor (first level or type 1), is Program Resource System Manager (PR/SM), which is integrated into the firmware. PR/SM runs the control code that manages the hardware resources and builds LPARs that run operating systems, middleware, and software applications.

The supported software hypervisors (type 2) are z/VM and KVM:

- ▶ z/VM supports the simultaneous execution of multiple virtual guest systems within an LPAR and nested (multi-level) virtualization. z/VM is a powerful hypervisor that can emulate various hardware devices to its guests.
- ▶ KVM provides flexibility for your hypervisor choice and the unique combination of enterprise hardware and open source.

z/VM and KVM interconnect with PR/SM and use its functions.

Multiple hypervisors can coexist and run simultaneously on the IBM Z platform so that you can create and build multiple virtualized guest systems that are running various open source applications on the IBM Z platform with high levels of performance and integrated security.

IBM Z development is continuously improving virtualization techniques. It provides highly scalable dynamic platforms that can host traditional and modern solutions (such as cloud, blockchain, and containers) on the same footprint.

Figure 4-1 shows the diverse workload that is supported and virtualized on a single IBM z16, and the co-existence of multiple hypervisors: PR/SM, z/VM, and KVM.

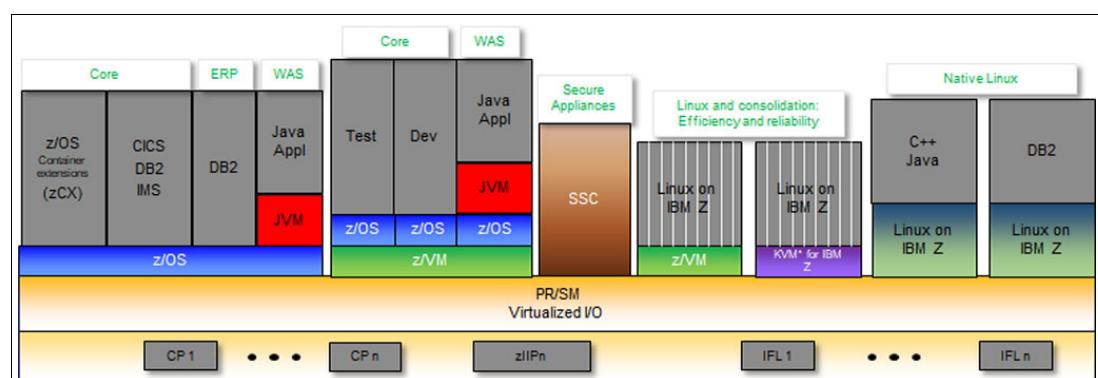


Figure 4-1 Virtualization on the IBM Z platform

Processor Resource/System Manager

PR/SM is a hardware-level hypervisor that is unique to and a vital component of the IBM Z platform.

PR/SM manages and partitions all the computing resources (CPU, memory, and I/O) among the various systems that run on the IBM Z platform. It provides each system with a required share of these resources and dynamically adjusts it, depending on the workload priority. PR/SM is integrated into the platform and runs transparently to the operating systems and applications.

Each operating system runs in its own LPAR that is managed by PR/SM, which allows for a high degree of the virtualization.

The goal of PR/SM is to allocate and assign (and reassign) resources to an LPAR so that a workload can achieve its best performance and throughput. Depending on the type of the workload, each LPAR can be defined as z/VM, Linux on IBM Z, z/OS, z/TPF, or z/VSE and runs one of these operating systems.

Initially, you might allocate a set of resources (CPU, memory, and I/O) and their quantity to the LPAR. Then, PR/SM might dynamically adjust the amount of the resources, according to the defined set of priorities. As a result, the most critical and important workload is allowed to complete within a required timeline.

PR/SM evolved over the decades on IBM Z platforms. It is a proven, secure, and fundamental IBM Z technology. Every generation of the IBM Z platform brings PR/SM improvements that are aimed to demonstrate even better system performance. With the IBM z16, PR/SM is extended to support new features, such as the LPAR support of the System Recovery Boost.

For more information about System Recovery Boost features, see “System Recovery Boost” on page 63.

Dynamic Partition Manager

Dynamic Partition Manager (DPM) is an infrastructure management component of the Hardware Management Console (HMC). It simplifies virtualization and configuration management. DPM is easy to use, especially for users who are new to IBM Z. It does not require you to learn complex syntax or command structures.

DPM provides partition lifecycle and integrated dynamic I/O and Peripheral Component Interconnect Express (PCIe) functions management for Linux on IBM Z that is running in an LPAR, under the z/VM or KVM. By using DPM, an environment can be created, provisioned, and modified without disrupting running workloads. It also can be monitored for troubleshooting.

DPM provides the following capabilities through the HMC:

- ▶ Create and provision an environment (including new partitions), assign processors and memory, and configure I/O adapters to connect the system to network and storage. DPM supports the following storage and network connectivity features:
 - OSA Express
 - FICON Express (Fibre Channel (FC) and Fibre Channel Protocol (FCP) mode)
 - Crypto Express
 - RDMA over Converged Ethernet (RoCE) Express
 - SMC-Dv2
 - HiperSockets
 - NVMe-attached solid-state drives (SSDs)

- ▶ Manage the environment, including the ability to modify system resources without disrupting workloads.
- ▶ Monitor and troubleshoot the environment to identify system events that might lead to degradation.

With its intuitive user interface, DPM also exposes its capabilities through Web Services APIs, which enable the integration of the system into cloud-like management infrastructures.

DPM on IBM z16 enables the use of Shared Memory Communications (SMC)-D V2, which provides a high-performance and low-latency interconnect between the workloads that are running in LPARs within the platform.

Configuration note: The IBM z16 can be configured in DPM mode or in PR/SM mode. It cannot be configured in both modes concurrently. DPM supports Linux on IBM Z, z/VM (only with Linux on IBM Z guests), and KVM. PR/SM mode supports a mixture of z/VM, KVM, z/OS, Linux on IBM Z, z/TPF, and z/VSE.

z/VM

z/VM is a native IBM Z operating system that provides virtualization services. It is a software hypervisor (type 2).

z/VM is a powerful hypervisor, historically being the first virtual machine (VM). z/VM runs in an LPAR and manages the system hardware resources (CPU, memory, and I/O) between its guest systems in a most efficient way.

z/VM supports z/OS, Linux on IBM Z, z/TPF, and z/VSE as its guest systems. It can also enable nested virtualization and can host z/VM as a guest system, allowing highly virtualized complex infrastructures for supporting containerized and cloud workloads.

z/VM can emulate and virtualize different hardware devices, such as virtual tape, and provide it to the operating systems that run under its management. z/VM is tightly coupled with PR/SM and uses its functions for the most optimized workload deployment.

z/VM is a proven, enterprise-grade hypervisor that can scale out horizontally and vertically. The IBM z16 supports up to 85 z/VM LPARs, while each z/VM LPAR can run thousands of guest systems.

KVM hypervisor

The KVM hypervisor is available in recent Linux on IBM Z distributions. It is a type 2 hypervisor that provides simple, cost-effective platform virtualization for Linux workloads that are running on the IBM Z platform. It enables you to share real CPUs (called IFLs), memory, and I/O resources through PR/SM.

KVM can coexist with other operating systems, such as Linux on IBM Z, z/OS, z/VM, z/VSE, and z/TPF that are running in different LPARs on the IBM Z platform.

The KVM hypervisor support information is provided by the Linux distribution partners. For more information, see the documentation for your distribution.

For more information about the use of KVM with IBM Z, see *Virtualization Cookbook for IBM Z Volume 5: KVM*, [SG24-8463](#).

4.2.1 Hardware virtualization

The IBM Z platform is well known for its unique virtualization capabilities. It allows you to deploy various workloads (traditional and modern) to achieve the highest performance and throughput metrics with the lowest costs and overhead.

Workload separation is one of the most important parameters. PR/SM in the IBM z16 is designed to meet the highest level of Common Criteria (EAL5+), similar to previous IBM Z platforms. This level of isolation ensures the integrity and security of the workloads and excludes the contamination of the running applications by other programs.

Logical processors

All physical PUs are virtualized as logical processors on the IBM Z platform and can be characterized as the following types:

- ▶ Central processors (CPs) are standard processors that support all operating systems and user workloads.
- ▶ A zIIP is used under z/OS for designated workloads. These workloads include, but are not limited to, the following examples:
 - IBM z/OS Container Extensions (zCX)
 - IBM Java virtual machine (JVM)
 - Various XML System Services
 - IPsec offload
 - Certain IBM DB2 for z/OS processes
 - DFSMS System Data Mover for z/OS Global Mirror
 - IBM HiperSockets for large messages
 - IBM GBS Scalable Architecture for Financial Reporting (SAFR) enterprise business intelligence reporting
 - IBM Z System Recovery Boost
- ▶ IFL processor is used exclusively for Linux on IBM Z and for running the z/VM and KVM hypervisors in support of Linux VMs.
- ▶ Internal Coupling Facility processor is used for z/OS clustering and supporting the family of Parallel Sysplex solutions. Internal Coupling Facility (ICF) is dedicated to this function and exclusively runs the Coupling Facility Control Code (CFCC).

The characterized PUs are aimed to streamline the specific workload. All engines architecturally and physically are the same.

In addition, the following pre-characterized processors are part of the base system configuration and are always present:

- ▶ SAPs that run I/O operations
- ▶ Integrated Firmware Processors (IFPs) for native PCIe features and other firmware functions

PR/SM accepts requests for work by dispatching logical processors on physical processors. Physical processors can be shared across LPARs or dedicated to an LPAR. The logical processors that are assigned to an LPAR must be all shared or all dedicated.

PR/SM ensures that the processor state is correctly saved and restored (including all registers) when you switch a physical processor from one logical processor to another. Data isolation, integrity, and coherence inside the system are always strictly enforced.

Logical processors can be dynamically added to and removed from LPARs. Operating system support is required to use this capability. z/OS, z/VM, and z/VSE each can dynamically define and change the number and type of reserved PUs in an LPAR profile. No planning is required.

The newly assigned logical processors are immediately available to the operating systems and for z/VM to its guest images. Linux on IBM Z provides the Standby CPU activation and deactivation functions.

Memory

To ensure security and data integrity, memory cannot be concurrently shared by active LPARs. Strict LPAR isolation is maintained to avoid any workload contamination.

An LPAR can be defined with an initial and reserved amount of memory. At activation time, the initial amount is made available to the partition, and the reserved amount can be added later partially or totally. Those two memory zones do not have to be contiguous in real memory, but the addressing area (for initial and reserved memory) is presented as contiguous to the operating system that runs in the LPAR.

z/VM can acquire memory nondisruptively and quickly make it available to guests. z/VM virtualizes this support to its guests, which can also increase their memory nondisruptively. Releasing memory is still a disruptive operation.

LPAR memory is said to be virtualized in the sense that, within each LPAR, memory addresses are contiguous and start at address zero. LPAR memory addresses are different from the system's absolute memory addresses, which are contiguous and have a single address of zero. Do not confuse this capability with the operating system that virtualizes its LPAR memory, which is done through the creation and management of multiple address spaces.

The z/Architecture features a robust virtual storage architecture that allows LPAR-by-LPAR definition of an unlimited number of address spaces and the simultaneous use by each program of up to 1023 of those address spaces. Each address space can be up to 16 EB (1 exabyte = 2^{60} bytes). Thus, the architecture has no real limits. Practical limits are determined by the available hardware resources, including disk storage for paging.

Isolation of the address spaces is strictly enforced by the Dynamic Address conversion hardware mechanism. A program's right to read or write in each page frame is validated by comparing the page key with the key of the program that is requesting access.

Definition and management of the address spaces is under operating system control. Three addressing modes (24-bit, 31-bit, and 64-bit) are simultaneously supported, which provides compatibility with earlier versions and investment protection.

IBM z16 supports 4 KB, 1 MB, and 2 GB pages, and an extension to the z/Architecture that is called Enhanced Dynamic Address Translation-2 (EDAT-2).

Operating systems can allow sharing of address spaces, or parts of them, across multiple processes. For example, under z/VM, a single copy of the read-only part of a kernel can be shared by all VMs that use that operating system. Known as *discontiguous shared segment* (DCSS), this shared memory use for many VMs can result in significant savings of real memory and improvements in performance.

I/O virtualization

The IBM z16 supports six logical channel subsystems (LCSSs), and has four subchannel sets in each LCSS with up to 256 channels for a total of 1536 channels. In addition to the dedicated use of channels and I/O devices by an LPAR, I/O virtualization allows concurrent sharing of channels.

The z/Architecture also allows sharing of the I/O devices that are accessed through these channels by several active LPARs. This function is known as *Multiple Image Facility* (MIF). The shared channels can belong to different channel subsystems (CSSs), in which case they are known as *spanned channels*.

Data streams for the sharing LPARs are carried on the same physical path with total isolation and integrity. For each active LPAR that includes the channel configured online, PR/SM establishes one logical channel path. For availability reasons, multiple logical channel paths must be available for critical devices (for example, disks that contain vital data sets).

When more isolation is required, configuration rules allow restricting the access of each LPAR to specific channel paths and specific I/O devices on those channel paths.

Many installations use the parallel access volume (PAV) function, which allows access to a device through several addresses (normally one base address and an average of three aliases). This feature increases the throughput of the device by using more device addresses.

HyperPAV takes the technology a step further by allowing the I/O Supervisor (IOS) in z/OS (and the equivalent function in the Control Program of z/VM) to create PAV structures dynamically. The structures are created depending on the current I/O demand in the system, which lowers the need for manually tuning the system for PAV use.

SuperPAV is an extension of the HyperPAV architecture and implements multiple logical subsystems (LSSs) within an alias management group (AMG). SuperPAV enables the following solution:

- ▶ Problem: A new I/O request occurs and no alias PAV devices are available in the alias pool for the base PAV device's LSS.
- ▶ Solution: z/OS attempts to use an alias PAV device from another LSS within the AMG subgroup.

SuperPAV can provide relief for systems that experience high I/O queue time (IOSQ) during periods of peak I/O load. When few aliases are defined in an LSS, aliases might not be available during a heavy I/O period. z/OS checks peer LSS alias pools to borrow an alias to start I/O requests. Previously, these I/O requests were left queued when aliases are not available.

In large installations, the total number of device addresses can be high. Therefore, the concept of *channel sets* is part of the z/Architecture.

Subchannel sets

With the IBM z16, up to four subchannel sets of approximately 64,000 device addresses are available. The base addresses² are defined to set 0 (IBM reserves 256 subchannels on set 0), and the aliases addresses are defined to set 1, set 2, and set 3.

Subchannel sets are used by the Metro Mirror (also referred to as *synchronous Peer-to-Peer Remote Copy* [PPRC]) function by having the Metro Mirror primary devices that are defined in subchannel set 0. Secondary devices can be defined in subchannel sets 1, 2 and 3, which provides more connectivity through subchannel set 0.

To reduce the complexity of managing large I/O configurations further, IBM Z introduced extended address volumes (EAVs). EAV provides large disk volumes. In addition to z/OS, z/VM and Linux on IBM Z support EAV.

By extending the disk volume size, potentially fewer volumes are required to hold the same amount of data, which simplifies systems and data management. EAV is supported by the IBM DS8K series.

The dynamic I/O configuration function is supported by z/OS and z/VM. It provides the capability of concurrently changing the active I/O configuration. Changes can be made to channel paths, control units, and devices. A fixed HSA area in the IBM z16 greatly eases the planning requirements and enhances the flexibility and availability of these reconfigurations.

4.2.2 Hybrid cloud environments

Virtualization is critical to the viability of cloud service offerings because it provides the elasticity that allows a platform to deal with the ebbs and flows of demands on IT resources. Because of the extreme integration in the hardware and firmware, virtualization on the IBM z16 is highly efficient (the best in the industry). It delivers up to 100% sustained resource use, and the highest levels of isolation and security. Therefore, the cloud solution costs (whether hardware, software, or management) are minimized.

Cloud elasticity requirements are covered by the IBM z16 granularity offerings, including capacity levels, tailor fit pricing (for unpredictable, high spiking, business-critical workloads), and Capacity on Demand (CoD). These and other technical leadership characteristics make the IBM Z platforms the gold standard for the industry.

In addition, managing a cloud environment requires tools that can take advantage of a pool of virtualized compute, storage, and network resources and present them to the consumer as a service in a secure way.

A Cloud Management system must enable the management of virtualized IT resources to support different types of cloud service models and cloud deployment models. OpenStack can satisfy a wide range of Cloud Management demands. It integrates various components to automate IT infrastructure service provisioning.

The IBM z16 also can be tailored with a choice of IBM Z-backed services that are delivered by way of IBM Cloud to help transform your infrastructure, applications, and data by exposing and connecting assets with simplified and intelligent operations across the infrastructure.

With Red Hat, the hybrid cloud capabilities on IBM Z are extended. Support for running OpenShift on Linux on IBM Z provides expansive cloud capabilities, including open containers, tools, and access to an extensive open community.

The new cloud-native capabilities are delivered as pre-integrated solutions called IBM *Cloud Paks*. The IBM-certified and containerized software provides a common operating model and a common set of services.

For more information about hybrid cloud capabilities, see [Hybrid cloud with IBM Z](#).

² Only a z/OS base device must be in subchannel set 0. Linux on IBM Z supports base devices in the other subchannels sets.

4.3 Capacity and performance

The IBM z16 offers significant increases in capacity and performance over its predecessor, the IBM z15. Several elements contribute to this effect, including the larger number of processors, individual processor performance, memory caches, SMT, and machine instructions, including the SIMD. Subcapacity settings continue to be offered.

Note: Capacity and performance ratios are based on measurements and projections by using standard IBM benchmarks in a controlled environment. Actual throughput can vary depending on several factors, such as the job stream, I/O and storage configurations, and workload type.

4.3.1 Capacity settings

The IBM z16 expands the offer on subcapacity settings. Finer granularity in capacity levels allows the growth of installed capacity to more closely follow the enterprise growth, for a smoother, pay-as-you-go investment profile. Many performance and monitoring tools are available on IBM Z environments that are coupled with the flexibility of the Cod options (see 4.3.2, “Capacity on-Demand offerings” on page 58). These features help to manage growth by making capacity available when needed.

IBM z16 capacity levels

Regardless of the installed model, the IBM z16 offers four distinct capacity levels for the first 39 CPs:

- ▶ One full capacity
- ▶ Three subcapacities

These processors deliver the scalability and granularity to meet the needs of medium-sized enterprises, while also satisfying the requirements of large enterprises that have large-scale, mission-critical transaction and data processing requirements.

A capacity level is a setting of each CP³ to a subcapacity of the full CP capacity. The clock frequency of those processors remains unchanged. The capacity adjustment is achieved by using other means.

Full capacity CPs are identified as CP7. On the IBM z16, up to 200 CPs can be configured as CP7. Up to 39 CPs can have subcapacity. The three subcapacity levels are identified by CP6, CP5, and CP4, and are displayed in hardware descriptions as feature codes on the CPs.

If more than 39 CPs are configured to the system, all must be full capacity because all CPs must be at the same capacity level. Granular capacity adds 117 subcapacity settings to the 200 capacity settings that are available with full capacity CPs (CP7). The 317 distinct capacity settings in the system provide for a range of 1:758 in processing power.⁴

A processor is always set at full capacity when it is characterized as anything other than a CP, such as a zIIP, an IFL, or an ICF. Correspondingly, a separate pricing model exists for non-CPs regarding purchase and maintenance prices and various offerings for software licensing.

³ The CP is the standard processor for use with any supported operating system. It is required to run z/OS.

⁴ This is calculated by dividing the highest capacity (200way full speed) of 212,222 Peripheral Component Express (PCI) by the lowest subcapacity of 280 PCI. $(212,222 \div 280 = 758)$

On IBM z16, the following CP subcapacity levels are a fraction of full capacity:

- ▶ Model 7xx = 100% (2253 PCI)
- ▶ Model 6xx = 66% (1498 PCI)
- ▶ Model 5xx = 41% (118 PCI)
- ▶ Model 4xx = 12% (35 PCI)

For administrative purposes, systems that have only ICFs or IFLs are now given a capacity setting of 400. For either of these systems, having up to 200 ICFs or IFLs (which always run at full capacity) is possible.

To help size a IBM Z platform to fit your requirements, IBM provides a no-cost tool that reflects the latest IBM Large Systems Performance Reference (LSPR) measurements that is called the IBM Z Processor Capacity Reference (zPCR). You can download the tool from [Getting Started with zPCR](#).

For more information about LSPR measurements, see [LSPR for IBM Z](#).

4.3.2 Capacity on-Demand offerings

The IBM z16 continues to provide CoD offerings. They provide flexibility and control and ease the administrative burden in the handling of the offerings. They also give finer control over resources that are needed to meet the resource requirements in various situations.

The IBM z16 can perform concurrent upgrades, which provide an increase of processor capacity with no platform outage. In most cases, with operating system support, a concurrent upgrade can also be nondisruptive to the operating system. It is important to consider that these upgrades are based on the enablement of resources that are physically present in the IBM z16.

Capacity upgrades cover permanent and temporary changes to the installed capacity. The changes can be done by using the Customer Initiated Upgrade (CIU) facility, without requiring the involvement of IBM service personnel. Such upgrades are started through the web by using IBM Resource Link.

Use of the CIU facility requires a special contract between the customer and IBM. This contract specifies the terms and conditions for online CoD buying of upgrades, and other types of CoD upgrades are accepted. For more information, see the [IBM Resource Link](#).

For more information about the CoD offerings, see *IBM z16 (3931) Technical Guide*, SG24-8951.

Permanent upgrades

Permanent upgrades of processors (CP, IFLs, ICF, zIIP, and SAP) and memory, or changes to a platform's Model-Capacity Identifier (up to the limits of the installed processor capacity on an existing IBM z16) can be performed by customers through the IBM Online Permanent Upgrade offering by using the CIU facility.

Temporary upgrades

Temporary upgrades of an IBM z16 can be done by On/Off CoD, Capacity Backup (CBU), or Capacity for Planned Event (CPE) that is ordered from the CIU facility.

On/Off CoD function

On/Off CoD is a function that enables concurrent and temporary capacity growth of the CPC. On/Off CoD can be used for peak workload requirements for any length of time. It includes a daily hardware charge, and can include an associated software charge. On/Off CoD offerings can be prepaid or post-paid.

When you use the On/Off CoD function, you can concurrently add processors (CP, IFLs, ICF, zIIP, and SAP), increase the CP capacity level, or both.

Prepaid OOCoD tokens: New prepaid OOCoD tokens do *not* carry forward to future systems.

Capacity Backup function

CBU allows you to perform a concurrent and temporary activation of extra CP, ICF, IFLs, zIIP, and SAP, an increase of the CP capacity level, or both. This function can be used during an unforeseen loss of IBM Z capacity within the enterprise, or to perform a test of your disaster recovery (DR) procedures. The capacity of a CBU upgrade cannot be used for peak workload management.

CBU features are optional and require unused capacity to be available on CPC drawers of the backup system as unused PUs, as a possibility to increase the CP capacity level on a subcapacity system, or both. A CBU contract must be in place before the Licensed Internal Code Configuration Control (LICCC) code that enables this capability can be loaded on the system.

An initial CBU record provides for one test for each CBU year (each up to 10 days) and one disaster activation (up to 90 days). The record can be configured to be valid for up to five years. You can also order more tests for a CBU record in quantities of five tests up to a maximum of 15.

Suitable use of the CBU capability does not incur any other software charges from IBM.

Flexible Capacity for Cyber Resiliency

Flexible Capacity (FC 9933 together with FC 0376) dynamically shifts production capacity cross sites between IBM z16 machines for flexibility and elasticity in case of DR testing, planned maintenance, proactive outage avoidance, and actual DR scenarios.

Flexible Capacity works with other temporary record types; for example, On/Off CoD, and Tailor Fit Pricing for Hardware.

Flexible Capacity allows capacity to be transferred remotely without requiring on-site personnel (IBM or customer) after initial set-up and provides the following benefits:

- ▶ Flexible duration of capacity transfer (up to one year)
- ▶ Fully automated by using solutions, such as GDPS
- ▶ Simplify compliance and improve confidence DR scenarios, including test
- ▶ No need for CBU records by using this solution

Capacity for Planned Event function (carry forward only)

CPE allows you to perform a concurrent and temporary activation of extra CPs, ICFs, IFLs, zIIPs, and SAPs, an increase of the CP capacity level, or both. This function can be used during a planned outage of IBM Z capacity within the enterprise (for example, data center changes or system or power maintenance). CPE cannot be used for peak workload management and can be active for a maximum of three days.

The CPE feature is optional and requires unused capacity to be available on CPC drawers of the backup system as unused PUs, as a possibility to increase the CP capacity level on a subcapacity system, or both. A CPE contract must be in place before the LICCC that enables this capability can be loaded on the system.

z/OS capacity provisioning

Capacity provisioning helps you manage the CP and zIIP capacity of IBM z16 that is running one or more instances of the z/OS operating system. By using the z/OS Capacity Provisioning Manager (CPM) component, On/Off Cod temporary capacity can be activated and deactivated under control of a defined policy. Combined with functions in z/OS, the IBM z16 provisioning capability gives you a flexible, automated process to control the configuration and activation of On/Off Cod offerings.

System Recovery Boost upgrade

System Recovery Boost upgrade can optionally enable the temporary activation of more physical zIIP processors on the IBM z16 by way of a priced Boost temporary capacity record. This record requires the use of feature codes 6802 and 9930.

Note: System Recovery Boost functions are embedded in the IBM z16 firmware. It can be used without ordering extra zIIP capacity (Feature Code 6802 and Feature Code 9930).

Activation of these processors uses unused processing cores in the IBM z16 to provide more zIIP processing capacity that accelerates execution of their workload (general-purpose workload and workload that is zIIP-eligible). After the Boost temporary capacity record is activated for use during maintenance (for example, a planned maintenance window or for a planned site-switch activity), up to 20 other zIIP engines can become available for up to 6 hours for use on the IBM z16. This extra zIIP capacity is then shared across images in accordance with PR/SM management controls, which makes more zIIP capacity available to individual system images.

Images that want to use this extra zIIP capacity predefine reserved logical zIIP capacity in their PR/SM image profiles. That way, the operating system can then bring those extra logical zIIP processors (with physical backing from the added physical zIIPs that were activated) online for use during the boost period. This configuration provides the image with increased zIIP capacity and parallelism to accelerate the workload.

Tailored Fit Pricing for IBM Z Hardware

The new Tailored Fit Pricing for IBM Z - Hardware Consumption Solution provides an always-on, consumption-based capacity corridor that provides hybrid cloud flexibility and control for unpredictable workload spikes throughout the day. It helps to scale IT demands and control behavior with a pay-for-use buffer and granular usage measurements.

For more information about the CoD offerings, see *IBM z16 (3931) Technical Guide*, SG24-8951.

4.3.3 IBM z16 performance

The IBM Z microprocessor chip of the IBM z16 has a high-frequency design that uses IBM leading microprocessor technology and offers more cache per core than other chips. In addition, an enhanced instruction execution sequence, along with processing technologies (such as SMT) delivers world-class per-thread performance. z/Architecture is enhanced by providing more instructions (including SIMD) that are intended to deliver improved CPU-centric performance and analytics.

For CPU-intensive workloads, more gains can be achieved by multiple compiler-level improvements. Improved performance of the IBM z16 is a result of the enhancements that are described in Chapter 2, “IBM z16 hardware overview” on page 13, and in 4.1, “Technology improvements” on page 46.

LSPR workload suite: IBM z16 changes

To help you better understand workload variations, IBM provides a no-cost tool, zPCR, which is available at the [IBM Presentation and Tools](#) website.

IBM continues to measure performance of the systems by using various workloads and publishes the results in the [Large Systems Performance Reference \(LSPR\) report](#).

IBM also provides a list of [millions of service units \(MSU\) ratings](#) for reference. Capacity performance is closely associated with how a workload uses and interacts with a specific processor hardware design. Workload capacity performance is sensitive to the following major factors:

- ▶ Instruction path length
- ▶ Instruction complexity
- ▶ Memory hierarchy

The CPU Measurement Facility (CPUMF) data offers insight into the interaction of workload with the hardware design. CPUMF data helps LSPR to adjust workload capacity curves that are based on the underlying hardware sensitivities, in particular the processor access to caches and memory. The workload category is determined by the Level 1 Misses per 100 instructions (L1MP) and the relative nest intensity (RNI).

With IBM Z, the LSPR introduced the following workload capacity categories that replace all prior primitives and mixes:

- ▶ LOW (RNI): A workload category that represents light use of the memory hierarchy.
- ▶ AVERAGE (RNI): A workload category that represents average use of the memory hierarchy. This category is expected to represent most production workloads.
- ▶ HIGH (RNI): A workload category that represents heavy use of the memory hierarchy.

These categories are based on the RNI, which is influenced by many variables, such as application type, I/O rate, application mix, CPU usage, data reference patterns, LPAR configuration, and the software configuration that is running. CPU MF data can be collected by z/OS System MF on SMF 113 records or z/VM Monitor.

In addition to low, average, and high categories, the latest zPCR provides the low-average and average-high mixed categories, which allow better granularity for workload characterization.

The LSPR tables continue to rate all z/Architecture processors that are running in LPAR mode and 64-bit mode. The single-number values are based on a combination of the default mixed workload ratios, typical multi-LPAR configurations, and expected early-program migration

scenarios. In addition to z/OS workloads that are used to set the single-number values, the LSPR tables contain information that pertains to Linux on IBM Z and z/VM environments.

The LSPR contains the internal throughput rate ratios (ITRRs) for the IBM z16 and the previous generations of processors. The report is based on measurements and projections by using standard IBM benchmarks in a controlled environment. The actual throughput that any user might experience varies depending on several factors, such as the amount of multiprogramming in the job stream, the I/O configuration, and the workload that is processed.

Experience demonstrates that IBM Z platforms can run at up to 100% usage levels, sustained. However, most users prefer to leave some white space and run at 90% or slightly under. For any capacity comparison, the use of “one number” (such as the MIPS or MSU metrics) is not a valid method. Therefore, use zPCR and involve IBM Support when you are planning for capacity.

For more information about IBM z16 performance, see *IBM z16 (3931) Technical Guide*, SG24-8951.

Throughput optimization with IBM z16

The memory and cache structure implementation in the CPC drawers of the IBM z16 were significantly enhanced compared to previous generations to provide sustained throughput and performance improvements. The memory is distributed throughout the CPC drawers and the CPC drawers have individual levels of cache that are private to the cores and shared by the cores. Nonetheless, all processors can access the highest level of cache and all of the memory. Therefore, the system is managed as a memory-coherent symmetric multiprocessor (SMP).

Processors within the IBM z16 CPC drawer structure have different distance-to-memory attributes. CPC drawers are fully interconnected to minimize the distance. Other non-negligible effects result from data latency when grouping and dispatching work on a set of available logical processors. To minimize latency, the system attempts to dispatch and later redispatch work to a group of physical CPUs that share cache levels.

PR/SM manages the use of physical processors by LPARs by dispatching the logical processors on the physical processors. However, PR/SM is not aware of which workloads are being dispatched by the operating system in what logical processors. The Workload Manager (WLM) component of z/OS has the information at the task level, but is unaware of physical processors.

This disconnect is solved by enhancements that enable PR/SM and WLM to work more closely together. They can cooperate to create an affinity between task and physical processor rather than between LPAR and physical processor, which is known as *HiperDispatch*.

HiperDispatch

HiperDispatch combines two functional enhancements: in the z/OS dispatcher and in PR/SM. This function is intended to improve computing efficiency in the hardware, z/OS, and z/VM.

In general, the PR/SM dispatcher assigns work to the minimum number of logical processors that are needed for the priority (weight) of the LPAR. On IBM z16, PR/SM attempts to group the logical processors into the same logical cluster or in the neighboring logical cluster in the same CPC drawer and, if possible, in the same chip. This configuration results in reduction of multi-processor effects, maximizing use of shared cache, and lowering the interference across multiple partitions.

The z/OS dispatcher is enhanced to operate with multiple dispatching queues, and tasks are distributed among these queues. Specific z/OS tasks can be dispatched to a small subset of logical processors. PR/SM ties these logical processors to the same physical processors, which improves the hardware cache reuse and locality of reference characteristics, such as reducing the rate of cross communication.

To use the correct logical processors, the z/OS dispatcher obtains the necessary information from PR/SM through interfaces that are implemented on the IBM z16. The entire IBM z16 stack (hardware, firmware, and software) tightly collaborates to obtain the full potential of the hardware. z/VM HiperDispatch provides support similar to the one in z/OS. It is possible to dynamically turn on and off HiperDispatch without requiring an initial program load (IPL).

The IBM z16 includes several HiperDispatch algorithm enhancements, including the following examples:

- ▶ Improved memory affinity
- ▶ Improved LPAR placement based on IBM z15 experience
- ▶ Exploitation of new chip configuration

Note: HiperDispatch is required if SMT is enabled. All IBM Z LSPR measurements are provided for z/OS environments with HiperDispatch on. The general recommendation is to turn on HiperDispatch for production workloads.

4.4 Reliability, availability, and serviceability

The IBM Z platform is known for its reliability, availability, and serviceability (RAS) capabilities. RAS is built into the hardware and software stacks of the IBM z/Architecture, where mean time between failures (MTBF) is measured in decades. The RAS strategy is to manage change by learning from previous generations of IBM Z and investing in new RAS functions to eliminate or minimize all sources of outages.

The IBM Z family presents numerous enhancements in RAS. Focus was given to reducing the planning requirements, while continuing to reduce planned, scheduled, and unscheduled outages. One of the contributors to scheduled outages are Licensed Internal Code (LIC) driver updates that are performed in support of new features and functions. Firmware updates can be performed by IBM remotely through Remote Code Load upgrades. Enhanced Driver Maintenance (EDM) can help reduce the necessity and eventual duration of a scheduled outage.

When suitably configured, the IBM z16 can concurrently activate a new LIC Driver level. Concurrent activation of the select new LIC Driver level is supported at released synchronization points. However, a concurrent update or upgrade might not be possible for specific LIC updates.

IBM z16 builds on the RAS characteristics of the IBM Z family, with the following RAS improvements:

- ▶ System Recovery Boost

System Recovery Boost is delivered with the IBM z16 to maximize service availability by using tailored short-duration boosts to mitigate the impact of these recovery processes:

- IBM SAN Volume Controller Dump boost boosts the system on which IBM SAN Volume Controller memory dump is taken to reduce system impact and expedite diagnostic capture. It is possible to enable, disable, or set thresholds for this option.

- Middleware restart, or recycle boost, boosts the system on which a middleware instance is being restarted to expedite resource recovery processing, release retained locks, and so on. It applies to planned restarts or restarts after failure, automated, or ARM-driven restarts. System Recovery Boost does not boost any system address spaces by default and must be configured by the WLM policy specification.
- HyperSwap configuration load boost boosts the system in which the HyperSwap configuration and policy information are being loaded or re-loaded. This boost applies to Copy Services Manager (CSM) and GDPS. HyperSwap Configuration Load boost is enabled by default. No thresholds or criteria are applied to the boost request based on the size or number of devices that is present in the HyperSwap configuration.

Through System Recovery Boost, the IBM z16 continues to offer more CP capacity during particular system recovery operations to accelerate system (operating system and services) start when the system is started or shutdown. System Recovery Boost is operating system-dependent. No other hardware, software, or maintenance charges are required during the boost period for the base functions of System Recovery Boost.

System Recovery Boost can be used during LPAR IPL or LPAR shutdown to make the running operating system and services available in a shorter period.

System Recovery Boost provides the following options for the capacity increase:

- Subcapacity Boost: During the boost period, subcapacity engines are being transparently activated at their full capacity (for CP engines only).
- zIIP Capacity Boost: During the boost period, all active zIIPs that are assigned to an LPAR are used to extend the CP capacity.

For more information about the optional temporary capacity upgrade, see “System Recovery Boost upgrade” on page 60.

System Recovery Boost can also be used for recovery processes, such as IBM HyperSwap⁵ by using a Recovery Process Boost. Recovery Process Boosts are short-term accelerations for specific sysplex recovery events in z/OS. Sysplex recovery events often cause short-duration workload impacts or workload spikes that can affect the normal running of workloads in the sysplex until recovery processing completes.

With Recovery Process Boosts, boosted processor capacity is made available to mitigate short-term recovery impacts and restore normal steady-state sysplex operation as quickly as possible after the recovery events.

Also, boosted processor capacity is provided for a short period after the restoration of steady-state operation for workload “catch-up”.

At the time of this writing, the main System Recovery Boost users are z/OS, z/VM, z/VSE, and z/TPF. z/VM uses System Recovery Boost if it runs on subcapacity CP processors only (IFLs are always at their full clock speed). Second-level z/VM guest operating systems can inherit the boost if they are running on CPs.

z/OS configured as a guest system under z/VM management does not use the boost. Inheritance of the boost applies only during z/VM workload initialization and shutdowns. Starts and shutdowns of the second-level guests, in isolation from z/VM, are not boosted.

System Recovery Boost support is available with GDPS V4.2⁶ and newer versions by way of firmware enhancements that support greater parallelism and performance improvements in the hardware API services. These enhancements are used by GDPS to speed up the orchestration of shutdown and restart activities. The boost of CP capacity does not contribute to other software license charges.

⁵ IBM HyperSwap is a high availability (HA) feature that provides dual-site, active-active access to a volume. HyperSwap functions are available on systems that can support more than one I/O group.

⁶ SRB does not require GDPS V4.2. GDPS V4.2 provides additional enhancements that are considered part of SRB.

For more information, see *Introducing IBM Z System Recovery Boost*, REDP-5563.

- ▶ IBM z16 Level 3 and Level 4 cache structures are virtualized; the physical level of shared cache is implemented in a robust SRAM wipe out correction and sparing design that benefits the virtualization levels. The cache allocation is fluid, dynamically changing the cache size as needed, which in turn benefits processor cores, CBU, and OOCoD.
- ▶ Two PU chips are packaged in a dual-chip module (DCM), which enhances thermal conductivity and improves reliability. The PU chip uses 7 nm technology and consists of 22.5 billion transistors (compared to 9.1 billion for IBM z15). Up to 8 active cores per chip that run at 5.2 GHz.
- ▶ VFM: Flash Express PCIe feature replacement with memory dual inline memory modules (DIMMs), which is more robust solution that uses RAIM protection against memory faults.

IBM z16 continues to support Enhanced Drawer Availability (EDA), which minimizes the effects of CPC drawer repair and upgrade actions. In a multiple CPC drawer system, a single CPC drawer can be concurrently removed and reinstalled for an upgrade⁷ or repair. To ensure that the IBM z16 configuration supports removal of a CPC drawer with minimal effect to the workload, consider the flexible memory option (see “Flexible memory” on page 49).

IBM z16 implements a new RAIM⁸ design that provides a method to increase memory availability where a fully redundant memory system can identify and correct memory errors without stopping. The implementation is similar to the RAID concept that is used in storage systems for several years. For more information about RAS features, see *IBM z16 (3931) Technical Guide*, SG24-8951.

IBM z16 can be configured with a maximum of four CPC drawers that are designed as a field-replaceable unit (FRU). Connections among the CPC drawers are established by using SMP cables. Each CPC drawer consists of four PU DCM and up to 48 DIMMs (protected by RAIM). In addition to the DCMs and memory, CPC drawers host memory connectors for I/O, STP interface, and manifolds.

IBM z16 inherits I/O infrastructure reliability improvements from IBM z15, including Forward Error Correction (FEC) technology that enables better recovery of FICON channels. FICON Express32S features continue to provide a new standard for transmitting data over 32 Gbps links by using 256b/257b encoding.

The IBM z16 configuration includes an improved front to rear radiator-cooling system. The radiator pumps, blowers, controls, and sensors are N+1 redundant. In normal operation, one active pump supports the system. A second pump is turned on and the original pump is turned off periodically, which improves reliability of the pumps. The replacement of pumps or blowers is concurrent with no effect on performance.

RAS also includes the following enhancements:

- ▶ Integrated sparing
- ▶ Error detection and recovery improvements in caches and memory
- ▶ 25 GbE RoCE Express3 (Optics as FRU)
- ▶ PCIe coupling links (improved diagnostics)
- ▶ Enhanced channel logging
- ▶ OSA-Express firmware changes to increase the capability of concurrent maintenance change level (MCL) updates

⁷ Adding a fourth drawer to the IBM z16 configuration is not supported in the field (manufacturing only).

⁸ Meaney, P.J., et al. “IBM zEnterprise redundant array of independent memory subsystem,” IBM Journal of Research and Development, vol.56, no.1.2, pp.4:1.4:11, Jan.-Feb. 2012, doi: 10.1147/JRD.2011.2177106.

- ▶ System power cycle management (servicing capability)
- ▶ CFCC level 25 (various enhancements for improving CF resiliency)
- ▶ IBM RMF reporting improvements

The IBM z16 continues to support concurrent addition of resources, such as processors or I/O cards, to an LPAR to achieve better serviceability. If another SAP is required on an IBM z16 (for example, as a result of a DR situation), the SAPs can be concurrently added to the CPC configuration.

It is possible to concurrently add CP, zIIP, IFL, and ICF processors to an LPAR. This function is supported by z/VM, and (with suitable program-temporary fixes [PTFs]) by z/OS and z/VSE. It is possible to concurrently add memory to an LPAR as well. This feature is supported by z/OS and z/VM.

The IBM z16 supports adding Crypto-Express features to an LPAR dynamically by changing the cryptographic information in the image profiles. Users can also dynamically delete or move Crypto-Express features. This enhancement is supported by z/OS, z/VM, and Linux on IBM Z.

4.4.1 RAS capability for the Support Element and Hardware Management Appliance

Two 1U trusted servers are inside the IBM z16 A frame: one is always the primary Support Element (SE) and the other is the alternative SE. The primary SE is the active SE. The alternative acts as the backup. Information is mirrored once per day. The SE servers include N+1 redundant power supplies.

SEs offer RAS improvements, such as ECC memory, redundant physical networks for SE networking requirements, redundant power modules, and better thermal characteristics.

The optional Hardware Management Appliance (HMA) (Feature Code 0129) feature provides HMC functions by using the same physical two 1U servers that run the SE code. The HMA feature provides two HMCs.

4.5 High availability with Parallel Sysplex

The Parallel Sysplex technology is an IBM Z clustering technology that allows users to build highly resilient, highly scalable, dynamic, and robust IBM Z environment to achieve near-continuous services and application availability. Hardware, middleware, and software tightly cooperate to achieve this result.

Parallel Sysplex is an active-active cluster with up to 32 members (z/OS systems). The underlying structure of the Parallel Sysplex remains transparent to users, networks, and applications.

The Parallel Sysplex features the following minimum components:

- ▶ CF

The CF is the cluster management center that enables workload distribution, inter-communications, and other system tasks. It can be implemented as an LPAR of a dedicated IBM Z, or within IBM Z, running alongside other LPARs. PUs that are characterized as CPs or ICFs are used to configure CF LPAR. ICFs are preferred because of software licensing reasons. Two or more Coupling Facilities (CFs) are recommended for high availability (HA).

- ▶ CFCC

This IBM LIC runs inside CF (no other code runs there). The code is used to create and maintain the CF structures. These structures are used under z/OS by software components, such as z/OS, DB2 for z/OS, CICS TS, and WebSphere MQ for synchronizing the access to the shared data and resources.

z/VM can emulate CFCC as a guest VM, which allows users to build a z/OS sysplex that consists of z/OS instances (images). Such a setup is useful for testing and developing purposes, but not suitable for the production environments.

- ▶ Coupling links

These high-speed links interconnect the several system images (each running in its own LPAR) that participate in the Parallel Sysplex. At least two connections between each physical platform and the CF must exist. Internal coupling (IC) links are used when all the system images run on the same physical platform.

On the software side, z/OS components participate in building the Parallel Sysplex.

z/OS and CF are highly connected. For example, they provide CF structure duplexing, which is a general-purpose, hardware-assisted, easy-to-use mechanism for duplexing structure data held in CFs. This function provides a robust recovery mechanism for failures, such as loss of a single structure on CF or loss of connectivity to a single CF. The recovery is done through rapid failover to the other structure instance of the duplex pair.

For more information about deploying system-managed CF structure duplexing, see the technical paper *System-Managed CF Structure Duplexing*, ZSW01975USEN. The paper is available by clicking **Learn more** at the [Parallel Sysplex website](#).

Normally, two or more z/OS images are clustered to create a Parallel Sysplex. Multiple clusters can span several IBM Z platforms, although a specific image (LPAR) can belong to only one Parallel Sysplex.

A z/OS Parallel Sysplex implements shared-all access to data. This configuration is facilitated by IBM Z I/O virtualization capabilities, such as MIF. MIF allows several LPARs to share I/O paths in a secure way, which maximizes use and greatly simplifies the configuration and connectivity.

A suitably configured Parallel Sysplex cluster is designed to maximize availability at the application level. Quick recovery after a failure is an essential part of Sysplex recovery, and that's why SRB boosts Sysplex recovery events. Sysplex also provides redundancy so that the workload can continue to execute on other systems in the sysplex. Rather than a quick recovery from a failure, the Parallel Sysplex design objective is zero application downtime.

Parallel Sysplex includes the following features:

- ▶ Data sharing with integrity

The CF is key to the implementation of share-all access to data. Every z/OS system image can access all of the data. Subsystems in z/OS declare resources to the CF. The CF accepts and manages lock and unlock requests on those resources, which helps to ensure the data integrity. A duplicate CF further enhances the availability. Key users of the data-sharing capability are Db2, IBM WebSphere MQ, IBM WebSphere ESB, IMS, and CICS.

Because these components are major infrastructure components, applications that use them inherently benefit from sysplex characteristics. For example, many large SAP implementations have the database component on DB2 for z/OS in a Parallel Sysplex.

- ▶ Near-continuous (application) availability

Changes, such as software upgrades and patches, can be introduced to one image at a time, while the remaining images continue to process the workload. For more information, see *Improving z/OS Application Availability by Managing Planned Outages*, SG24-8178.

- ▶ High capacity

Parallel sysplex scales up to 32 images. The scalability is near linear as z/OS images are added to a sysplex. This structure contrasts with other forms of clustering that use n-to-n messaging, which leads to rapidly degrading performance with a growing number of nodes.

- ▶ Dynamic workload balancing

The incoming workload can be automatically directed to any of the Parallel Sysplex cluster operating system images where capacity is available transparently to the applications. z/OS WLM component is a key workload distributor, ensuring that the required Service Level Agreement (SLA) goal is achieved.

- ▶ Systems management

This architecture provides the infrastructure to satisfy a requirement for continuous availability and enables techniques for achieving simplified systems management consistent with this requirement.

- ▶ Resource sharing

Global Resource Serialization (GRS) component of z/OS manages the access to the shared resources (such as CPU, memory, network, and storage) across all members of Parallel Sysplex.

- ▶ Single system image (SSI)

The collection of system images in the Parallel Sysplex is displayed as a single entity to the operator, user, database administrator, and others. A single-system image ensures reduced complexity from operational and definition perspectives. You can rapidly scale out your workload without any added infrastructure costs by adding members to the Parallel Sysplex.

- ▶ N-2 support⁹

Three hardware generations often are supported in the same Parallel Sysplex. IBM z16 can coexist and connect with IBM z15 and IBM z14 systems.

Software support for multiple releases or versions is provided.

⁹ Provided coupling and timing links are not InfiniBand.

- ▶ CF encryption support

Supports encrypted data while it is being transferred to and from the CF while it is in the CF Structure. Consider the following points:

- z/OS Systems must have the cryptographic hardware configured and activated to perform cryptographic functions and hold Advanced Encryption Standard (AES) master keys within a secure boundary. Feature Code 3863 CPACF DES and TDES Enablement must be installed to use the Crypto-Express6 Coprocessor (CEX6C), or the Crypto-Express7 Coprocessor (CEX7C), or the Crypto-Express8 Coprocessor (CEX8C) feature.

- Support provided can be enabled only when all systems are z/OS 2.3 or higher.

- ▶ Dynamic activation of I/O configurations for stand-alone CFs

Dynamic I/O configuration changes can be made to a stand-alone CF without requiring a disruptive power on reset. (A stand-alone CF does not have any running instances of z/OS or z/VM).

An LPAR with a firmware-based appliance that contains an activation service is used to apply the I/O configuration changes. The LPAR on an IBM z16 is driven by an updated HCD instance that is running in a z/OS LPAR on a remote IBM z16, IBM z15, or IBM z14.

- ▶ Improved performance and resilience¹⁰

- Fair Latch Manager 2 is an enhancement to the internals of the CFCC dispatcher. It provides CF work management efficiency and processor scalability improvements, and improves the “fairness” of arbitration for internal CF resource latches across tasks, which results in CF efficiency.
- The CF provides more information to z/OS about every message path that appears active. Namely, the current SYID (system ID) with which the message path is registered in the CF. Whenever z/OS interrogates the state of the message paths to the CF, z/OS checks this SYID information for currency and correctness. This feature improves the delivery of signals between CF and z/OS.

¹⁰ The two enhancements listed were initially implemented on the IBM z15.

The components of a Parallel Sysplex as implemented within the IBM z/Architecture are shown in Figure 4-2. The configuration is one of many possible Parallel Sysplex configurations.

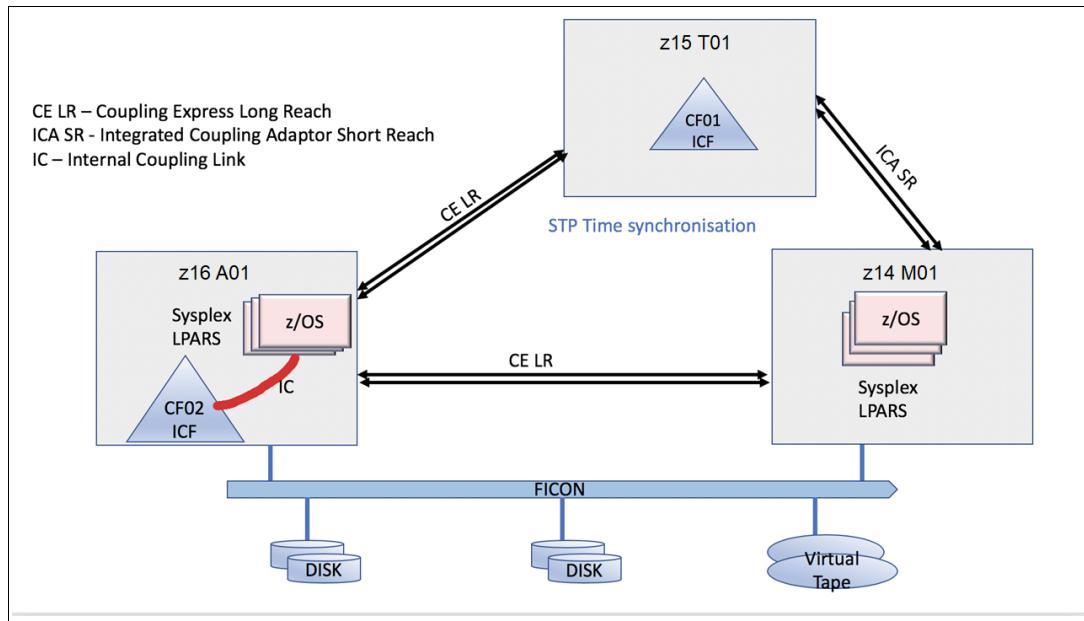


Figure 4-2 A sample Parallel Sysplex deployment

Server Time Protocol (STP) over coupling links provide time synchronization to all systems in the sysplex.

For more information about coupling link options, see 3.4, “Clustering connectivity” on page 38.

4.6 Pervasive encryption

Cryptography and corporate security always were a fundamental aspect of IBM Z platform development. IBM Z continues to enhance and introduce new cryptography features and functions. These changes ensure the highest level of protection of your data and applications, making the platform compliant with the mandatory industry and regulatory standards.

The corporate security consists of many levels, with the strategies and policies for all components of the infrastructure: applications, databases, network, storage, and others. The traditional approach lays in defining the data perimeters and applying encryption selectively only to those perimeters. Because the data is almost never static in the system as it flows between various systems and applications, this selective approach has a significant disadvantage: after the data leaves the defined perimeter, it becomes exposed.

The selective paradigm presumes complex management of the overall infrastructure as well, where the failure to protect one of the components might lead to the security breach and compromise of the whole landscape.

Today, businesses demand a more comprehensive approach because applications might be subject to various cyberthreat attacks (both external and internal). Regulations around data privacy and protection also are becoming more demanding, such as European Union (EU)

General Data Protection Regulation (GDPR), Payment Card Industry Data Security Standard (PCI-DSS), and Health Insurance Portability and Accountability Act (HIPAA).

Pervasive encryption shifts this paradigm to the data-centric one: the data is becoming the new perimeter, and the encryption applies to all of the data, regardless of its origin and location. At the same time, this approach does not require costly application changes, being transparent to the applications and their service consumers.

Pervasive encryption provides 360 degrees of data encryption, for data at-rest (stored in persistent storage) and data in-flight (transactions). This approach reduces the risks of a security breach and financial losses that are associated with it and adheres to the standards and compliance.

Pervasive encryption uses the hardware cryptography acceleration in the IBM z16, which is proven to be more effective, performant, and stable compared to the software encryption.

Pervasive encryption is enabled by way of tight integration between IBM Z hardware and software, and includes the following features:

- ▶ Integrated cryptographic hardware:
 - CPACF is a coprocessor on every PU that accelerates symmetric encryption operations.
 - Crypto-Express features are hardware security modules (HSMs)¹¹ with the following features:
 - Complies with Federal Information Processing Standards (FIPS) 140-2 Level 4 (achieving the highest level of compliance within this standard).
 - Accelerates various cryptographic algorithms (digital signature sign/verification and many others).
 - Acting as tamper-proof storage for private keys and other highly sensitive information.
 - The CPACF and Crypto-Express usage is implemented on the hardware level, and supported natively by all IBM Z operating systems, which provides the highest encryption performance.
- ▶ Data set and file (also known as volume) encryption: Linux on IBM Z volumes and z/OS data sets are protected by using policy-controlled encryption, without any need to change or modify the applications.
- ▶ Network encryption: Network data traffic is protected by using standards-based encryption from endpoint to endpoint.
- ▶ Storage encryption: Encrypting the storage subsystem disks and its file systems.
- ▶ CF encryption: This encryption secures the Parallel Sysplex infrastructure, including the CF links and data that stored in the CF, by using policy-based encryption.
- ▶ Secure Execution for Linux on IBM Z is a capability that helps protect against cyberthreats in multitenanted cloud environments. It ensures that users and system administrators cannot access sensitive data in Linux based virtual environments.

Secure Execution for Linux protects the confidentiality and integrity of data at enterprise scale. To achieve this goal, it isolates data at the VM level, and ensures that only the people within the organization who have a need to know are allowed to access to data in the clear.

¹¹ An HSM is a hardware computing device that safeguards and manages digital keys for strong authentication and accelerated crypto-operations and algorithms.

- ▶ Secure Boot is an enhancement that secures the booting process of an open source operating system, such as Linux on IBM Z. With the increased number of public open source repository attacks, the extra step of verifying that the operating system kernel version was introduced. Secure Boot integrity checks validate that an operating system kernel is from an official provider and is not compromised. Secure Boot can be used by Linux on IBM Z running in z/VM or KVM environments.

A complete chain of trust can be established from a trusted source to a boot loader. The process enforces Common Criteria compliance, which becomes a mandatory requirement.

4.6.1 IBM Fibre Channel Endpoint Security

IBM Fibre Channel Endpoint Security adds endpoint authentication and encryption to data in-flight. It can help reduce insider threats of unauthorized access to the data by using traces, switch logs, or technicians who use FC analyzers to examine the packets during problem determination to name a few.

IBM Fibre Channel Endpoint Security is designed to provide a means to help ensure the integrity and confidentiality of all data that flows on FC links between trusted entities within and across data centers. The trusted entities are the IBM z16 and the IBM Storage subsystem (select DS8000 storage systems). No application or middleware changes are required. Fibre Channel Endpoint Security supports all data in-flight from any operating system.

IBM Z Feature code 1146, Endpoint Security Enablement, along with CPACF enablement (Feature Code 3863) and FICON Express32S (Feature Code 0461 and Feature Code 0462) and for FICON Express16SA (Feature Code 0436 or Feature Code 0437, carry forward only), turn on the Fibre Channel Endpoint Security panels on the HMC so setup can be done.

IBM Security Guardium Key Lifecycle Manager (SKLM) acts as a trusted authority for key generation operations and authentication server. It provides shared secret key generation in a relationship between an FC initiator (IBM Z) and the IBM Storage target. The solution implements authentication and key management called IBM Secure Key Exchange (SKE).

Before establishing the connection, each link must be authenticated, and if successful, then becomes a trusted connection. A policy sets the rules; for example, enforcing the trusted connections only. If the link goes down, the authentication process starts again. The secure connection can be enabled automatically, if both the IBM Z and IBM Storage endpoints are encryption-capable.

Data in flight (from and to IBM Z and IBM Storage) is encrypted when it leaves either endpoint (source) and decrypted at the destination. Encryption/decryption is done at the FC adapter level. The operating system that is running on the host (IBM Z) is not involved in Endpoint Security-related operations. Tools are provided at the operating system level for displaying information about encryption status.

4.6.2 IBM Hyper Protect Data Controller

Data is almost never static in the system. It flows between various applications and system components, completes an extract, transform, and load (ETL) process that moves the data to another platform for further analysis and reporting, and other actions.

Today, data privacy (controlling the use of the data) is as important as data protection (the use of secure protocols or other means to encrypt and protect the data). Data protection ensures

a secure flow of the data from a starting point to an endpoint with data always remaining protected and encrypted. However, data protection capabilities are not intended to provide data flow auditing and access management for the data, which is where *IBM Hyper Protect Data Controller* can help.

Hyper Protect Data Controller provides a data-centric audit and protection (DCAP) approach for the protection of eligible data across the enterprise. It is part of the IBM Z pervasive encryption strategy to protect data that is on IBM Z and as it moves throughout the enterprise and beyond.

The concept of DCAP is a change from the current model. Before the data is moved around the enterprise, it is repackaged into a secure object. In Hyper Protect Data Controller, this object is called the Encrypted Data Object (EDO). The Hyper Protect Data Controller feature does this protection at a field-level, which means that a level of granularity to this protection exists that cannot be obtained from more broad protection techniques.

Important: The Hyper Protect Data Controller feature supports data sources that can be accessed through a secure API (or a JDBC driver).

Hyper Protect Data Controller is composed of a component that is known as the *Data Controller* that provides all the protection, enforcement, policy, and key management for the solution. The Data Controller provides an intercept point to transform *raw* eligible data to enforce data protection. The data is protected at the point of extraction and enforced at the point of consumption. The flexible policy defines the pool of trusted users and their access to the data based on their role. The key lifecycle management (generation, revocation, and other actions) is done within Data Controller.

The data is encrypted with standard AES-256 keys, which are managed by the Data Controller. Future access to sensitive data can be revoked remotely by using Hyper Protect Data Controller and can even be made unusable by destroying its encryption key.

For more information, see *Getting Started with IBM Hyper Protect Data Controller*, SG24-8495.

4.6.3 Secure Service Container

In a production environment, applications are subject to any number of external (cyberattacks) or internal (malicious software, system administrators who use their privileged rights for unauthorized access, and many others) security risks. Secure Service Containers provide trusted execution environments for applications by way of tamper protection during installation and runtime, restricted administrator access, and encryption of data in-flight and at-rest.

A Secure Service Container is an integrated IBM Z appliance and hosts the most sensitive workloads and applications. They act as a highly protected and secured digital vault and enforce security by encrypting the entire stack. The application that is running inside the Secure Service Container is isolated and protected from outsider and insider threats.

Secure Service Containers combine hardware, software, and middleware and is unique to the IBM Z platform. Although it is called a container, it should not be confused with purely open source containers (such as Docker).

An LPAR is defined as a Secure Service Container through the HMC.

A Secure Service Container features the following key advantages:

- ▶ Existing applications require zero changes to use Secure Service Container. Software developers do not need to write any Secure Service Container specific programming code.
- ▶ End-to-end encryption of data-in-flight and data at-rest:
 - Automatic Network Encryption (TLS, IPsec): Data in-flight.
 - Automatic volume encryption (Linux Unified Key Setup [LUKS]): Data at-rest. LUKS is the standard way in Linux to provide volume encryption. A Secure Service Container encrypts all data with a key that is stored within the appliance.
 - Protected memory: Up to 16 TB can be defined per Secure Service Container LPAR.
- ▶ Encrypted Diagnostic Data.

All diagnostic information (debug dump data and logs) are encrypted and do not contain any user or application data.
- ▶ No operating system access.

After the Secure Service Container appliance is built, Secure Shell (SSH) and command-line interface (CLI) are unavailable. This configuration ensures that even system administrators cannot access the contents of a Secure Service Container and do not know what application is running there.
- ▶ Applications that run inside a Secure Service Container are accessed externally by REST APIs only.
- ▶ Tamper-proof Secure Boot for a Secure Service Container.

Eligible applications are booted into a Secure Service Container by using verified booting sequence, in which only software code that is trusted and digitally signed and verified by IBM is uploaded into the Secure Service Container.
- ▶ Vertical workload isolation is provided by PR/SM. PR/SM in the IBM z16 is designed to meet the highest level of Common Criteria (EAL5+), similar to previous IBM Z platforms.
- ▶ Horizontal workload isolation: Separation from the rest of the host environment.

A Secure Service Container is a powerful IBM technology for providing the extra protection of the most sensitive workloads.

IBM Hyper Protect Crypto-Services offerings use the Secure Service Container technology as a core layer to provide hyper-protected services in IBM Cloud and on-premises. For more information, see [IBM Cloud Hyper Protect Crypto Services](#).

For more information about IBM Secure Service Container offerings, see [IBM Hyper Protect Virtual Servers](#).

4.7 Quantum-safe technology

IBM recognizes that with any new technology, new threats exist, and as such, suitable counter measures must be taken.

Quantum technology can be used for incredible good, but in the hands of an adversary, it has the potential to weaken or break core cryptographic primitives that were used to secure systems and communications. This potential leaves the foundation for digital security at risk.

The National Institute of Standards and Technology (NIST) started a process to solicit, evaluate, and standardize quantum-safe public-key cryptographic algorithms to address

these issues. Quantum-safe cryptography aims to provide protection against attacks that can be started by quantum computers.

The IBM z16 uses quantum-safe technologies to help protect your business-critical infrastructure and data from potential attacks.

IBM z16 Secure Boot technology protects system firmware integrity by using quantum-safe and classical digital signatures to perform a hardware-protected verification of the Initial Machine Load (IML) firmware components. This protection is anchored in a hardware-based root of trust to help ensure that the system starts safely and securely by keeping unauthorized firmware (or malware) from taking over the system during startup.

The IBM z16 enables the following quantum-safe capabilities:

- ▶ Key generation
- ▶ Encryption
- ▶ Key encapsulation mechanisms
- ▶ Hybrid key exchange schemes
- ▶ Dual digital signature schemes

In addition to the quantum-safe cryptographic capabilities, tools such as IBM Application Discovery and Delivery Intelligence (ADDI), Integrated Cryptographic Service Facility (ICSF), and IBM Crypto Analytics Monitor (CAT) can help you discover where and what cryptography is used in applications. These tools can aid in developing a cryptographic inventory for migration and modernization planning.



Operating system support

This chapter describes the operating system requirements and support considerations for the IBM z16 and its features.

Support and use of hardware functions depend on the operating system version and release. The information in this chapter is subject to change. Therefore, for the most current information, see *Preventive Service Planning (PSP)* bucket for 3931DEVICE (IBM z16 A01) at [Preventive Service Planning buckets for mainframe operating environments](#).

This chapter describes the following topics:

- ▶ 5.1, “Software support summary” on page 78
- ▶ 5.2, “Support by operating system” on page 82
- ▶ 5.3, “Software licensing” on page 85
- ▶ 5.4, “References” on page 86

5.1 Software support summary

The software portfolio for the IBM z16 includes various operating systems and middleware that support the most recent and significant technologies. The following major operating systems are supported:

- ▶ z/OS
- ▶ z/VM
- ▶ z/VSE
- ▶ z/TPF
- ▶ Linux on IBM Z and the Kernel-based Virtual Machine (KVM) hypervisor

5.1.1 Operating system summary

The current and minimum operating system levels that are required to support the IBM z16 are listed in Table 5-1. Operating system levels that are no longer in service are not covered in this publication.

Table 5-1 Operating system requirements

Operating system	End of service	Notes
z/OS V2R5	Not announced	
z/OS V2R4	Not announced.	
z/OS V2R3	September 2022. ^a	
z/OS V2R2 ^b	September 2020. ^c	
z/VM V7R3 ^d	Not announced.	
z/VM V7R2	Not announced.	
z/VM V7R1	March 2023.	
z/VSE V6R2	Not announced.	
z/TPF V1R1	Not announced.	
Linux on IBM Z ^e	Support information is available for SUSE ^f , Red Hat ^g , and Canonical. ^h	
KVM hypervisor	For more information about minimal and recommended distribution levels, see the Linux distributors' websites.	

a. Planned date. All statements regarding IBM plans, directions, and intent are subject to change or withdrawal without notice. Any reliance on these Statements of Direction is at the relying party's sole risk and will not create liability or obligation for IBM.

b. Toleration support only; must have purchased IBM Software Support Services offering.

c. The IBM Software Support Services offering provides the ability for customers to purchase extended defect support service for those z/OS releases, which are end of service.

d. Preview announcement at the time of this writing.

e. For more information, see the [Linux on IBM Z page](#) of the IBM Z website.

f. For more information, see the [Support page](#) of the SUSE website.

g. For more information, see the [Red Hat Enterprise Linux Life Cycle page](#) of the Red Hat website.

h. For more information, see the [Ubuntu for IBM Z page](#) of the Ubuntu website.

Program temporary fixes (PTFs) and FIXCATs: The use of several features depend on a particular operating system level. In all cases, PTFs might be necessary with the operating system level indicated.

Review the IBM Z hardware fix categories before the operating system is installed.

PTFs for z/OS, z/VM, and z/VSE can be ordered electronically from [IBM Shop](#).

For more information about obtaining access to download the z/TPF and z/TPFD APAR packages, contact TPFQA@us.ibm.com.

For Linux on IBM Z distributions and the KVM hypervisor, see the distributor's support information.

Fix packs for IBM software products that are running on Linux on IBM Z can be downloaded from [IBM Fix Central](#).

5.1.2 Application development and languages

Software developers can take advantage of the multiple programming language environments that run on IBM Z. Compilers and development tool support for the IBM Z platform are continuously extended to provide developers with agile and modern development methods.

Linux on IBM Z application development support is similar to the Linux on distributed platforms; therefore, this chapter focuses on z/OS environment.

In addition to the traditional COBOL, PL/I, Fortran, and assembly languages, IBM Z platforms support C, C++, Java (including Java Platform, Enterprise Edition, and batch environments), Go, Swift, Python, JavaScript, and Node.js.

IBM actively embraces open source projects to extend z/OS functions. For example, the Zowe open source project brings together industry experts to drive innovation for the community of next-generation mainframe developers. This framework enables an ecosystem of software solutions that are intended to provide a simple, intuitive environment for various IT professionals that are performing administrative, development, test, and operation tasks on z/OS¹.

For more information, see the [Zowe community page](#).

The IBM z/OS Container Extensions (zCX) feature allows you to run Docker containers natively under z/OS. This feature requires z/OS V2.R4 or higher and IBM z14 (or higher) hardware. For more information, see the [z/OS Container Extensions \(zCX\) web page](#).

An extensive set of advanced integrated development environments (IDEs) and integration tools are available for continuous development, testing, and deployment of application code.

IBM Z embraces emerging concepts, such as DevOps. *DevOps* is the process of bringing Development and Operations together to share processes and procedures to reduce the risk of change and improve the speed of deployment.

Organizations are embarking on their journey with digital transformation and entering the API economy. Therefore, it becomes essential to connect business-critical applications that run on IBM Z platforms with mobile and cloud applications to better engage with customers. A key step in this evolution is to understand which assets exist in the enterprise.

¹ <https://www.openmainframeproject.org/projects/zowe#>

The IBM DevOps offerings, such as IBM Application Delivery Foundation for z and IBM Rational® Team Concert®, can be coupled with IBM Application Discovery and Delivery Intelligence (ADDI) to enable developers to understand the applications, gain cognitive insights into the process, and evolve those valuable older assets at speed with reduced risk to the enterprise.

Modern development practices are supported by [IBM Rational Team Concert](#) and open source-based Git Version Control Tools for IBM z/OS (ported by Rocket Software), which are modern source code managers that run on and support z/OS.

For more information about software for IBM Z platforms, see the [Products catalog web page](#).

Note: The use of the most recent versions of the compilers is of utmost importance. The compilers use the latest technologies on IBM Z platform and the performance benefits that are introduced. Examples of benefits include new cache structures, new machine instructions, and instruction execution enhancements.

The IBM z16 inherits and the features and functions from its predecessor, the IBM z15, such as on chip compression and sort, and single-instruction multiple-data (SIMD) architectural notation, which provides efficient vector processing.

Java applications benefit from Guarded Storage Facility (GSF), which enables pause-less garbage collection.

Operating systems that run on IBM z16 can use System Recovery Boost to accelerate recovery after an outage.

The following security functions were introduced to complement the IBM Z security stack:

- ▶ Secure Execution: Provides better isolation and security for second-level guest systems that are running under the KVM hypervisor for IBM Z.
- ▶ Secure Boot: A feature for verifying the open source operating systems' kernel to ensure that it comes from the trusted provider.
- ▶ Quantum-safe cryptography algorithms (Kyber & Dilithium 8,7)
- ▶ Fully homomorphic encryption
- ▶ Processor Activity Instrumentation to count cryptographic operations

5.1.3 Supported IBM compilers

Each new version of the following IBM z/OS compilers underscores the continuing IBM commitment to the COBOL, PL/I, and C/C++ programming languages on the z/OS platform:

- ▶ Enterprise COBOL

The most recent version of Enterprise COBOL delivers improved performance with IBM z16 use and advanced optimization. It supports:

- COBOL to Java Interoperability (for example, Java can call COBOL and vice versa)
- UTF-8
- 64-bit JSON support
- JSON Boolean support for Parse and Generate

On the IBM z16, it optimizes:

- BCD to HFP conversions
- Numeric editing operation
- Zoned decimal operations

► **IBM Automatic Binary Optimizer for z/OS**

The Automatic Binary Optimizer for z/OS improves the performance of compiled COBOL programs. The Optimizer does not require source code, source code migration, or the tuning of performance options. It uses modern optimization technology to accelerate the performance of COBOL objects that are compiled by VS COBOL II V1.3 and later.

► **Enterprise PL/I**

The latest version of Enterprise PL/I on IBM z16 provides:

- More hardware use: PTFF instruction
- Enhanced diagnostics for SUBSCRIPTRANGE
- Modernization enhancements:
 - Enhanced COMPARE for XML and JSON
 - Support for EBCDIC JSON

► **z/OS XL C/C++**

The z/OS XL C/C++ enables developing high performance-oriented applications through the services that are provided by IBM Language Environment® and Runtime Library extension base elements. It also works with z/OS Problem Determination Tools.

The latest version features:

- High-performance math libraries:
 - MASS
 - Replace Atlas with OpenBLAS
 - Metal C for modernization of HLASM applications
 - Neural Network Processing Assist (NNPA) Facility
- **Java**
- The latest version of Java supports:
- On-chip z Enterprise Data Compression support
 - Crypto: ECDSA / ECDH acceleration
 - Zoned Decimal operations in DAA library for enhance interoperability
 - Java enablement of DLC models that use IBM Z Integrated Accelerator for Artificial Intelligence (AIU)

IBM Enterprise COBOL and Enterprise PL/I support are strategic components (separately orderable products) for IBM Rational Developer for IBM Z software. These features provide a robust IDE for COBOL and PL/I and connecting web services, Java Platform, Enterprise Edition (Java EE) applications, and traditional business processes.

z/OS XL C/C++ programmers can also use [IBM Developer for z/OS](#) to help boost productivity by editing, compiling, and debugging z/OS XL C and XL C++ applications from the workstation.

- ▶ IBM Open Enterprise SDK for Python

Also available on z/OS is the IBM Open Enterprise SDK for Python (Current Version 3.10), which is based on the popular Python interpreter from Python Software Foundation (PSF):

- z/OS LE-based, 64 bit only
- Runs on z/OS UNIX System Services environment with no prerequisites
- Supports ASCII, EBCDIC, and Unicode (UTF-8)
- Includes selected PyPI packages

For more information, see this [IBM Documentation web page](#).

5.2 Support by operating system

This section lists the support of in-service operating systems for functions of the IBM z16.

For more information about the IBM z16 and its features, see *IBM z16 (3931) Technical Guide*, SG24-8951.

For more information about all of the I/O features, see *IBM Z Connectivity Handbook*, SG24-5444.

5.2.1 z/OS

z/OS is a core IBM Z operating system that supports IBM z16 use. IBM z16 capabilities differ depending on the z/OS release.

The z/OS release cycle was extended with IBM Software Support Services to provide the ability for customers to purchase extended defect support service for previous versions of the operating system.

The minimum required version of z/OS to run on IBM z16 is V2R2 with PTFs (IBM Extended Software Support Services offering must be purchased). Use support on z/OS:

- ▶ z/OS V2.R3 + PTFs
- ▶ z/OS V2.R4 + PTFs
- ▶ z/OS V2.R5 + PTFs

This z/OS release supports toleration only and does not support new functions.

z/OS supports the following select (but not limited to) new functions:

- ▶ Coupling Facility Control Code (CFCC) Level 25
- ▶ HiperDispatch Enhancements
- ▶ New CPU MF Counters
- ▶ System Recovery Boost enhancements
- ▶ zDNN library enablement for IBM Z AIU
- ▶ Up to 16 TB of real memory for z/OS image (not IBM z16 specific)
- ▶ Compilers and Automatic Binary Optimizer for z/OS use
- ▶ Use of new hardware instructions: XL C/C++ ARCH(14)
- ▶ Integrated Cryptographic Support Facility
- ▶ zSort hardware sort instruction (SORTL)

- ▶ Integrated on-chip IBM zEnterprise Data Compression (zEDC) compression
- ▶ zDNN library enablement for IBM Z AIU
- ▶ Compliance-ready Central Processor Assist for Cryptographic Functions (CPACF)
Counters support to track crypto compliance and instruction usage

Before the IBM z16 migration process is started, see the IBM z16 workflows that are provided with each release of z/OS. This information is available in the z/OS IBM z16 Upgrade Workflow for z/OSMF, which is provided with APAR OA62703 on V2R2 and higher. The z/OSMF workflow contains only the z/OS steps for upgrading to IBM z16 and installs into the /usr/lpp/bcp/upgrade directory.

z/OSMF is recommended because it offers interactive assistance and runs associated health checks.

z/OS zCX enablement on the IBM z16 is provided by IBM Container Hosting Foundation for z/OS (5655-HZ1). On IBM z14 and IBM z15, this enablement is provided by the hardware Feature Code 0104. Feature Code 0104 is *not* available on IBM z16.

For more information, see this [IBM Support web page](#).

For more information about z/OS downloads, see this [z/OS Downloads web page](#).

5.2.2 z/VM

z16 support is provided with PTFs for z/VM 7.1 and 7.2, and included in the z/VM 7.3 base.

Note: At time of this writing, z/VM 7.3 is planned for general availability in September 2022.

Compatibility support enables guest use for several new facilities, including the following examples:

- ▶ Embedded Artificial Intelligence Acceleration
Designed to reduce the overall time that is required to run CPU operations for neural networking processing functions, and help support real-time applications, such as fraud detection.
- ▶ Compliance-ready CPACF Counters support
Means for guests to track crypto compliance and instruction use.
- ▶ Breaking Event Address Register (BEAR) Enhancement Facility
Facilitates debugging wild branches.
- ▶ Vector Packed Decimal Enhancements 2
Instructions that are intended to provide performance improvements.
- ▶ Reset DAT protection Facility
Provides a more efficient way to disable DAT protection, such as during copy-on-write or page change tracking operations.
- ▶ RDMA over Converged Ethernet (RoCE) Express3 feature
Allows guests to use Routable RoCE, Zero Touch RoCE, and Shared Memory Communications (SMC)-R V2 support.
- ▶ Guest enablement for the Crypto Express8S feature and assorted crypto enhancements

- Including quantum-safe API guest use support that is available to dedicated guests.
- ▶ CPU/Core topology location information within z/VM monitor data
 - Provides a better picture of the system for diagnostic and tuning purposes.
- ▶ Consolidated Boot Loader for guest IPL from SCSI

z/VM logical partitions (LPARs): IBM z16 central processors (CPs) and Integrated Facilities for Linux (IFLs) feature increased capacity over the capacity of their predecessors. Therefore, we suggest that you review and adjust the capacity of z/VM LPARs and of any guests in terms of the *number* of IFLs and CPs (real or virtual) to achieve the capacity that you require.

For more information about PTF availability, see the [z/VM Continuous Delivery News web page](#).

For more information about for IBM z16 migration, see the hardware PSP buckets for 3931DEVICE, and 3931DEVICE z/VM subset.

For more information about all IBM z16 features and functions that are supported by the z/VM releases, see *IBM z16 (3931) Technical Guide*, SG24-8951.

5.2.3 z/VSE

The IBM z16 support is provided by z/VSE V6R2. Consider the following points:

- ▶ z/VSE runs in z/Architecture mode only
- ▶ z/VSE V6.2 supports High-Performance FICON for IBM Z (zHPF) and SIMD
- ▶ System Recovery Boost (subcapacity CP speed boost only)

For more information about all IBM z16 features and functions that are supported by the z/VSE releases, see *IBM z16 (3931) Technical Guide*, SG24-8951.

5.2.4 VSE

IBM plans to support 21st Century Software VSEn V6.3 on IBM z16. For more information, see [this web page](#).

5.2.5 z/TPF

IBM z16 support is provided by z/TPF V1R1 with PTFs.

For more information about all IBM z16 features and functions that are supported by the z/TPF, see *IBM z16 (3931) Technical Guide*, SG24-8951.

5.2.6 Linux on IBM Z

The Red Hat, SUSE, and Ubuntu releases that are supported on the IBM z16 are listed in Table 5-2.

Table 5-2 *Linux on IBM Z distributions*

Linux on IBM Z distribution	Version and release
SUSE Linux Enterprise Server	SLES 15 SP3 with service
SUSE Linux Enterprise Server	SLES 12 SP5 with service (not as a Secure Execution KVM host)
Red Hat Enterprise Server	RHEL 8.4 with service
Red Hat Enterprise Server	RHEL 7.9 with service (not as a KVM host)
Canonical	Ubuntu 22.04 LTS with service
Canonical	Ubuntu 20.04.1 LTS with service

For more information about all IBM z16 features and functions that are supported by the Linux on IBM Z distributions, see *IBM z16 (3931) Technical Guide*, SG24-8951.

5.2.7 Kernel-based Virtual Machine hypervisor

For the IBM z16, the KVM is delivered and supported by the Linux distribution partners. For more information about KVM support for the IBM Z platform, see the following resources:

- ▶ The documentation for your distribution
- ▶ *The Virtualization Cookbook for IBM Z Volume 5: KVM*, SG24-8463

5.3 Software licensing

The IBM Z software portfolio includes operating system software (that is, z/OS, z/VM, z/VSE, and z/TPF) and middleware that runs on these operating systems. The portfolio also includes middleware for Linux on IBM Z environments. For the IBM z16, the following metric groups for software licensing are available from IBM (depending on the software product):

- ▶ Monthly license charge (MLC)

MLC pricing metrics feature a recurring monthly charge. In addition to the permission to use the product, the charge includes access to IBM product support during the support period. MLC pricing applies to z/OS, z/VSE, and z/TPF operating systems. Charges are based on processor capacity, which is measured in millions of service units (MSU) per hour.

- ▶ IBM Z Tailored Fit pricing for software²

Tailored Fit Pricing is a flexible software pricing model that dramatically simplifies the pricing landscape through flexible deployment options that are tailored to your IBM Z environment.

Two new pricing solutions, Enterprise Consumption and Enterprise Capacity, offer alternatives to the rolling four-hour average (R4HA)-based pricing model for new and existing workloads.

² Tailored Fit Pricing for IBM Z Hardware Consumption Solution is also available for IBM z16 systems. For more information, see <https://www.ibm.com/it-infrastructure/z/pricing>.

- ▶ IBM International Program License Agreement (IPLA)

IPLA metrics feature a single, up-front charge for an entitlement to use the product. An optional and separate annual charge, called *subscription and support*, entitles you to access IBM product support during the support period. With this option, you can also receive future releases and versions at no extra charge.

Software Licensing References

For more information about software licensing, see the following resources:

- ▶ [Learn about Software licensing](#)
- ▶ [Base license agreements](#)
- ▶ [IBM Z Software Pricing reference guide](#)
- ▶ [The IBM International Passport Advantage® Agreement](#) can be downloaded from the Learn about Software licensing website
- ▶ [IBM Z Tailored Fit Pricing](#) for software

Subcapacity pricing terms for z/VM and select z/VM-based programs

Subcapacity pricing is available to clients running on the z/VM Version 7 platform. Software pricing at less than full machine capacity can provide more flexibility and improved cost of computing as a client manages the volatility and growth of new workloads.

For more information about subcapacity pricing terms for z/VM and z/VM-based programs, see announcement letter 217-267, dated July 17, 2017.

For more information about software licensing options that are available for IBM z16, see *IBM z16 (3931) Technical Guide*, SG24-8951.

5.4 References

For current planning information, see the following operating system web pages:

- ▶ [z/OS](#)
- ▶ [z/VM](#)
- ▶ [z/VSE](#)
- ▶ [z/TPF](#)
- ▶ [Linux on IBM Z](#)

Abbreviations and acronyms

ADDI	Application Discovery and Delivery Intelligence	DCM	dual-chip module
AES	Advanced Encryption Standard	DCSS	discontiguous shared segment
AI	artificial intelligence	DES	Data Encryption Standard
AIU	IBM Integrated Accelerator for Artificial Intelligence	DHCP	Dynamic Host Configuration Protocol
AMG	alias management group	DIMM	dual inline memory module
ASHRAE	American Society of Heating, Refrigerating, and Air-Conditioning Engineers	DPM	Dynamic Partition Manager
BEAR	Breaking Event Address Register	DR	disaster recovery
BMC	Base Management Card	DRAM	dynamic random access memory
BNC	Bayonet Neill-Concelman	DRNG	Deterministic Random Number Generation
BPA	Bulk Power Assembly	EAV	extended address volume
BPR	Bulk Power Regulator	ECC	Elliptic Curve Cryptography
BTS	Backup Time Server	EDA	Enhanced Drawer Availability
CAT	Crypto Analytics Monitor	EDM	Enhanced Driver Maintenance
CBU	Capacity Backup	EDO	Encrypted Data Object
CCA	Common Cryptographic Architecture	EP11	Enterprise PKCS #11
CEX6C	Crypto-Express6 Coprocessor	EPO	Emergency Power Off
CEX7C	Crypto-Express7 Coprocessor	ETL	extract, transform, and load
CEX8C	Crypto-Express8 Coprocessor	ETS	External Time Source
CF	Coupling Facility	EU	European Union
CFCC	Coupling Facility Control Code	FC	Fibre Channel
CISC	Complex Instruction Set Computer	FEC	Forward Error Correction
CIU	Customer Initiated Upgrade	FID	Function Identifier
CLI	command-line interface	FIPS	Federal Information Processing Standards
CoD	Capacity on Demand	FRU	field replaceable unit
CPACF	Central Processor Assist for Cryptographic Functions	GDPR	General Data Protection Regulation
CPC	central processor complex	GRS	Global Resource Serialization
CPE	Capacity for Planned Event	GSF	Guarded Storage Facility
CPM	Capacity Provisioning Manager	HA	high availability
CP	central processor	HADR	high availability and disaster recovery
CPUMF	CPU Measurement Facility	HDFP	hardware decimal floating point
CSM	Copy Services Manager	HIPAA	Health Insurance Portability and Accountability Act
CSS	channel subsystem	HMA	Hardware Management Appliance
CST	Coordinated Server Time	HMC	Hardware Management Console
CTC	channel-to-channel	HSA	hardware system area
CTN	Coordinated Timing Network	HSM	hardware security module
DCAP	data-centric audit and protection		

HVDC	High-Voltage DC	PAV	parallel access volume
IBM	International Business Machines Corporation	PCI-HSM	Payment Card Industry PTS HSM
IC	internal coupling	PCI	Peripheral Component Express
ICF	Integrated Coupling Facility	PCIe	Peripheral Component Interconnect Express
ICFs	Integrated Coupling Facilities	PCIeCC	Peripheral Component Interconnect Express Cryptographic Coprocessor
ICSF	Integrated Cryptographic Service Facility		
IDE	integrated development environment	PDU	Power Distribution Unit
IFLs	Integrated Facilities for Linux	POR	power-on reset
IFP	Integrated Firmware Processor	PPC	Processor Power Card
IML	Initial Machine Load	PRNG	pseudo-random number generation
IOS	I/O Supervisor	PSF	Python Software Foundation
IOSQ	I/O queue time	PSP	Preventive Service Planning
iPDU	Intelligent Power Distribution Unit	PSU	Power Supply Unit
IPL	initial program load	PTF	program temporary fix
IPLA	IBM International Program License Agreement	PTP	Precision Time Protocol
ISA	Instruction Set Architecture	PTS	Preferred Time Server
ISM	Internal Shared Memory	PU	processor unit
ITRR	internal throughput rate ratio	R4HA	rolling four-hour average
JVM	Java virtual machine	RAIM	redundant array of independent memory
KVM	kernel-based virtual machine	RAS	reliability, availability, and serviceability
LAN	local area network	RDMA	Remote Direct Memory Access
LCSS	logical channel subsystem	RNI	relative nest intensity
LIC	Licensed Internal Code	RoCE	RDMA over Converged Ethernet
LICCC	Licensed Internal Code Configuration Control	RSF	Remote Support Facility
LPAR	logical partition	SAFR	Scalable Architecture for Financial Reporting
LR	Long Reach	SAP	System Assist Processor
LSPR	Large Systems Performance Reference	SE	Support Element
LSS	logical subsystem	SHA	Secure Hash Algorithm
MAC	Media Access Control	SIMD	single-instruction, multiple-data
MCL	maintenance change level	SKE	Secure Key Exchange
MCU	Memory Controller Unit	SKLM	Secure Guardium Key Lifecycle Manager
MIF	Multiple Image Facility	SMC	Shared Memory Communications
MLC	monthly license charge	SME	subject matter expert
MSU	millions of service units	SMP	symmetric multiprocessor
MTBF	mean time between failures	SMT	simultaneous multithreading
MTP	multi-fiber termination push-on	SORTL	sort instruction
NNPA	Neural Network Processing Assist	SR	Short Reach
NTP	Network Time Protocol	SSH	Secure Shell
OLTP	online transaction processing	SSI	single system image
OSC	Oscillator Card		

STP	Server Time Protocol
TDES	Triple Data Encryption Standard
TKE	Trusted Key Entry
TRNG	true-random number generator
UDX	User Defined-Extension
UIFL	Unassigned Integrated Facilities for Linux
VFM	Virtual Flash Memory
VM	virtual machine
WLM	Workload Manager
zCX	z/OS Container Extensions
zEDC	zEnterprise Data Compression
zHPPF	High-Performance FICON for IBM Z
zIIP	IBM Z Integrated Information Processor

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