EECS 470 Worksheet: Lab 1

Due on Gradescope by Friday, 9/6 at 11:59pm

This worksheet is your deliverable for the lab assignment. Answer the questions, then talk to an instructor during lab or office hours to get the check-off and submit it on Gradescope. In Gradescope we will only be checking the signature, not the answers.

Feel free to download this worksheet from the website if you want to work on it with a tablet.

1. Combinational

Which basic logic gate does this module implement?

AND OR NAND NOR XOR

2. For-loop

Why does the break statement in the loop not create a dependency from one iteration of the loop to the next?

This doesn't create a dependency because no other iterations rely on data from the break and the break doesn't rely on data from previous iterations

3. State Machine

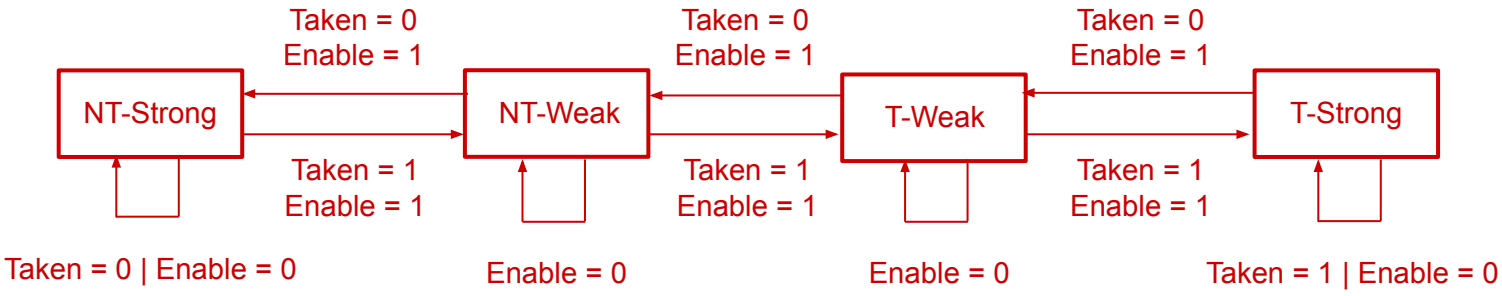
3.1. Sequential Clock/Reset

Why do we need a clock and reset in this module but not the previous modules?

This state machine needs a clock and a reset so that it can make progressive decisions based on the results of previous iterations, and the reset allows it to return to a base state.

3.2. State Diagram

Draw the state transition diagram for this module.
Include the enable signal as an input and write the prediction output at each state.



4. Register File

4.1. `read_out`

The `read_out` signal is driven by multiple branches in an if-statement. What common hardware block could you use to implement this?

An if with multiple branches can commonly be implemented in hardware with a multiplexer

4.2. Signals

Which signals in this module are wires, which are registers (flip-flops)?
(Assume that input data signals are register-driven)

clock	read_idx	write_idx	write_en	write_data	read_out	register_data	internal_forward
wire / reg	wire / reg	wire / reg	wire / reg	wire / reg	wire / reg	wire / reg	wire / reg

5. Accessing CAEN

Show the instructor that you can access CAEN and download Project 1 from GitHub.

Instructor signature and date:
(or unique code if virtual)