Product Specification

Product Name: ZX2000
Document Number:
PCB Part #: 600-0105-001
Document Revision: 2.10
Product Description: Shelf/Switch for 6 Slot ATCA
Date: 2011/12/14
Distribution: Standard
Lead OEM: Pentair Schroff

Revision History

Date	Revision	Editor	Description
2010/11/15	1.0	AW	Original.
2010/12/10	1.03	AW	Changed design for 6 10GE SFP+ ports and Micrel KS8873 3-port switch. Added IPMI addesssing tables.
2010/12/13	1.04	AW	Changed ShMC backplane connector J2. Merged ShMC J1 into ShMC J2
2010/12/17	1.05	AW	Changed Hardware Addressing.
2011/1/5	2.00	AW	Changes from Pentair Schroff Meeting.
2011/4/7 2011/4/19 2011/4/25 2011/4/28 2011/5/30 2011/6/23 2011/7/15 2011/8/24 2011/8/30 2011/12/14	2.01 2.02 2.03 2.04 2.05 2.06 2.07 2.08 2.09 2.10	AW	Final Changes prior to Pentair Schroff Meeting April 19, 2011. -Dual Star Backplane. -New Backplane Connector (J2); Computer Telephony Requirements -Modified J2 Pinout – Removed FAN_SPEED pin & ADM1024. -New Power Connector. -New Cross Connector changed in Port Mapping section. -ShMM Connector changes -Changed ShMM Ethernet Connections to follow PPS recommendation. -Document Updates -Software Port Numbering Changes (Backplane does not change)

The ZX2000 is an ATCA 6 Node chassis in a 5U form factor. It has provisions for the ZX2010 Shelf Manager/Switch Combination board and a custom backplane that uses ATCA 3.1 compliant signals to provide service to the 6 Node Slots. Features include:

- Six 10/100/1000BASE-TX link connections to Base in Physical Slots 1-6.
- Six Option 1, Opt 9, Opt 9+ links connections to Fabric in Physical Slots 1-6.
- Shelf Manager (ShMC) functions for the ATCA 3.0 enclosure.
- On board CPU for intelligent media control with out-of-band RS-232 and Ethernet.
- Thermal & Voltage sensors.

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Product Scope

Many 5U chassis enclosures exist on the market today, but are limited to a maximum of 4 Node Slots in the 5U form factor and needing two expensive hub cards. The ZX2000 is a product innovation bringing to market an ATCA chassis with 6 Node Slots in the same 5U form factor. The ZX2000 product will require a change to the ATCA backplane to accept a new dual purpose Shelf Manager/Switch Board providing both ShMC and Hub capabilities to the linecards populated within the 6 Node Slots. This specification will define the changes needed to each system to ensure the finished product can be delivered to the market in a timely and cost effective manner.

The scope of this Product Specification is limited to PICMG 3.1 Option 1 (GE), Option 9 (10GE) and Option 9+ (40GE). The changes made to the backplane are media independent and transportable to other PICMG standards (3.1 FibreChannel, 3.2 Infiniband, 3.3 StarFabric, 3.4 PCI_Express and 3.5 RapidIO).

The use of the Shelf/Switch concept beyond PICMG 3.1 Ethernet for Znyx is forbidden without the express written consent of Znyx Networks. Znyx Networks plans to apply for trademark and patent rights on the concept and use of the Shelf/Switch.

Feature Set

- Open Standard PICMG 3.0 (AdvancedTCA) compliance
- Dual Purpose Shelf Manager/Switch providing PICMG 3.0 ATCA ShMC and Hub capability
- Six 10/100/1000BASE-TX link connections to Base in Physical Slots 1-6.
- Six PICMG 3.1 Fabric Opt1, Opt9, Opt9+ link connections to Fabric in Physical Slots 1-6.
- HiGig Serial Interface for Inter-Switch Link via Update Channel
- ShMC cross capable according to the PICMG Engineering Change Notice ECN3.0-2.0-001
- Six 1G/10G SFP+ ports.
- Embedded Power PC microprocessor
- Two Fast Ethernet Ports for Out Of Band (OOB) Network Management (Shelf & Switch)
- Two Serial RS-232 for Command Line Interface to microprocessor (Shelf & Switch)
- Industry Standard ShMC controller (Pigeon Point ShMM-500)

Product Set

- **ZX2000** – 5U 6-Slot ATCA Chassis and Backplane
  - Dual -48V PEMs
  - Dual Fan Trays
  - EMI Fan filter tray
- **ZX2010** – Shelf/Switch 10Gbe for 6-Slot Node Chassis
- **ZX2040** - Shelf/Switch 40Gbe for 6-Slot Node Chassis
- **ZX7300** – 24 port 1Ge + 2 port 10Gbe Node Switch
- **ZX2000PE** – Node Egress board for ATCA PICMG 3.1
  - Egress both 1G/10Ge Fabric connections to slot (SFP+)
  - Egress option for 40Ge switch fabrics
  - Egress both Base slot connections (RJ45)

The Schroff 11596-160 ATCA Chassis chassis has been identified as a candidate to achieve the needs of the Znyx ZX2000, 5U 6 Node Slot ATCA Chassis. The Schroff 11596-160 is a 6 slot chassis in a 5U form factor designed for use in either 19" or 23 " width rack or on the lab bench.

Standard Schroff Zephyr chassis

Figure 1: Shelf Front and Rear View

1	Slot for Shelf Manager 1	8	ESD Wrist Strap Terminal
2	Slot for Shelf Alarm Panel (SAP)	9	Air Filter
3	Fan Tray left	10	Slot for Shelf Manager 2
4	Front Card Cage	11	ATCA 6-Slot Backplane
5	Ground Terminal	12	Fan Tray right
6	PEM B	13	Rear ESD Wrist Strap Terminal
7	Rear Card Cage	14	PEM A

The current off-the-shelf 11596-160 is shipped with the following components:

- 5U High Chassis for 19" rack mount
- Six slots AdvancedTCA slots
- Bused IPMI
- 8U x 280mm Front Module Board Support
- 8U x 70mm Rear Transition Board Support
- Dual -48VDC Input with redundant removable PEMs
- EMI Filtered and fuse protection input
- 350W/Slot
- Optimized Fan Cooling; Two fan systems provide a Push-Pull cooling arrangement
- Optimized airflow for >350W/board
- Fault Tolerant airflow scheme
- Two ShMC controller slots providing Shelf Management for fail-over redundancy capability in Fault Tolerant/High Availability Systems. **(Modified for ZX2000)**
- Shelf Alarm Panel Slot providing audible minor, major and critical Telco alarming with DB-15 connection. **(Not required for ZX2000)**
- Triple Replicated Mesh Backplane **(Not required for ZX2000)**

Delivery comprises of (1) 5U ATCA chassis in black powdercoat for six 280mm deep blades and RTMs, (1) ATCA backplane for 6 slot Dual Star Configuration, (2) Fan tray FRU with 6 fans, (1) Presence monitored Air Filter, (2) Redundant -48V-60VDC Power Entry Modules (PEMs).

For the Schroff 11596-160 to perform the functionality of the ZX2000, the Backplane, the Shelf Manager and the Switch slots must be modified. The following sections will define the changes needed to transform the Schroff 11596-160 into the ZX2000.

Industry Standards

Standard	Revision	Description	Status
PICMG 3.0	3.0	AdvancedTCA Base Specification	
PICMG 3.1	1.0	Ethernet/Fibre Channel for ATCA	
Pigeon Point (ShMM-500R)	1.0.9	Pigeon Point Shelf Management Mezzanine Hardware Architecture	
Schroff (ShMM-CB-V)	1.0	Schroff Shelf Manager User's Manual ShMM-ACB_V (21596-291)	
Schroff (ATCA Shelf)	1.0	Schroff AdvancedTCA Shelf, 6-Slot User's Manual (11596-160)	

Schroff Shelf Manager

The Schroff Shelf Manager is a 78mm x 280mm form factor that fits into a dedicated Shelf Manager slot in the Schroff ATCA enclosure. The Shelf management is based on the Pigeon Point Shelf management solution for AdvancedTCA products. The Shelf management executes on the Shelf Management Mezzanine 500 (ShMM-500), a compact SO-DIMM form-factor module, installed on a Schroff carrier board called the ATCA Carried Board version V (ACB-V). The SHMM-500 and the ACB-V together form the ShMM-ACB-V, the Shelf Manager for Schroff ATCA enclosures.

The ACB-V carrier board includes several on-board devices that enable different aspects of the Shelf management based on the ShMM-500. These facilities include I2C-based hardware monitoring/control and GPIO expander devices. The ShMM-ACB-V provides individual Ethernet connections to both Base Hubs (ShMC cross connect), according to the PICMG Engineering Change Notice ECN3.0-2.0-001. Hardware jumpers provide for the first Ethernet (ETH0) to be routed either to the RJ45 on the front panel or to the ATCA Backplane connector J2 (default setting). See Schroff ATCA_11596-160 User Manual sec 9.5 for reference. The Ethernet ports on the ShMM-ACB-V support both 10Mb (10BASE-T) and 100Mb (100BASE-TX) operations.

The Shelf Manager RS-232 Console serial interfaces to a RJ45 connector on the Shelf Alarm Panel. The serial console default configuration is 115200 baud, no parity, 8 data bits, 1 stop bit. The ZX2000 does not implement the Shelf Alarm Panel.

Other functions of the ShMM-ACB-V are pull-ups to IPMB bus interface by the active ShMC, four I2C bus interfaces to off board devices, hardware address, System Management of Fan control and Voltage monitoring, Reset push button, Hot Swap Interface, Redundancy Control Interface, RTC backup battery(option), Command Line Interface, (through Telnet, SSH or the Shelf Manager serial port on the SAP), Firmware Update.

Backplane & Chassis Modifications

For the Schroff 11596-160 to perform the functionality of the ZX2000, the Backplane will need the following modifications:

- ATCA Physical Slot 1 & Slot 2 are converted from a Hub Slot into a Node Slot.
- Shelf Alarm Panel connector and trace routes are removed from the backplane.
- Two ATCA compliant Data Transport connectors(J22, J23) are added to the Shelf Mgr slots.
- -48V Power Connector added to each Shelf Manager slot.
- The Triple Replicated Mesh is modified to Dual Star. See Backplane Routing Table.

The chassis enclosure will need the following modifications:

- Relocate one of the rails for the ShMC to the center of the chassis.
- Remove part of the Top Chassis Flange to allow for taller components into the ShMC slots.

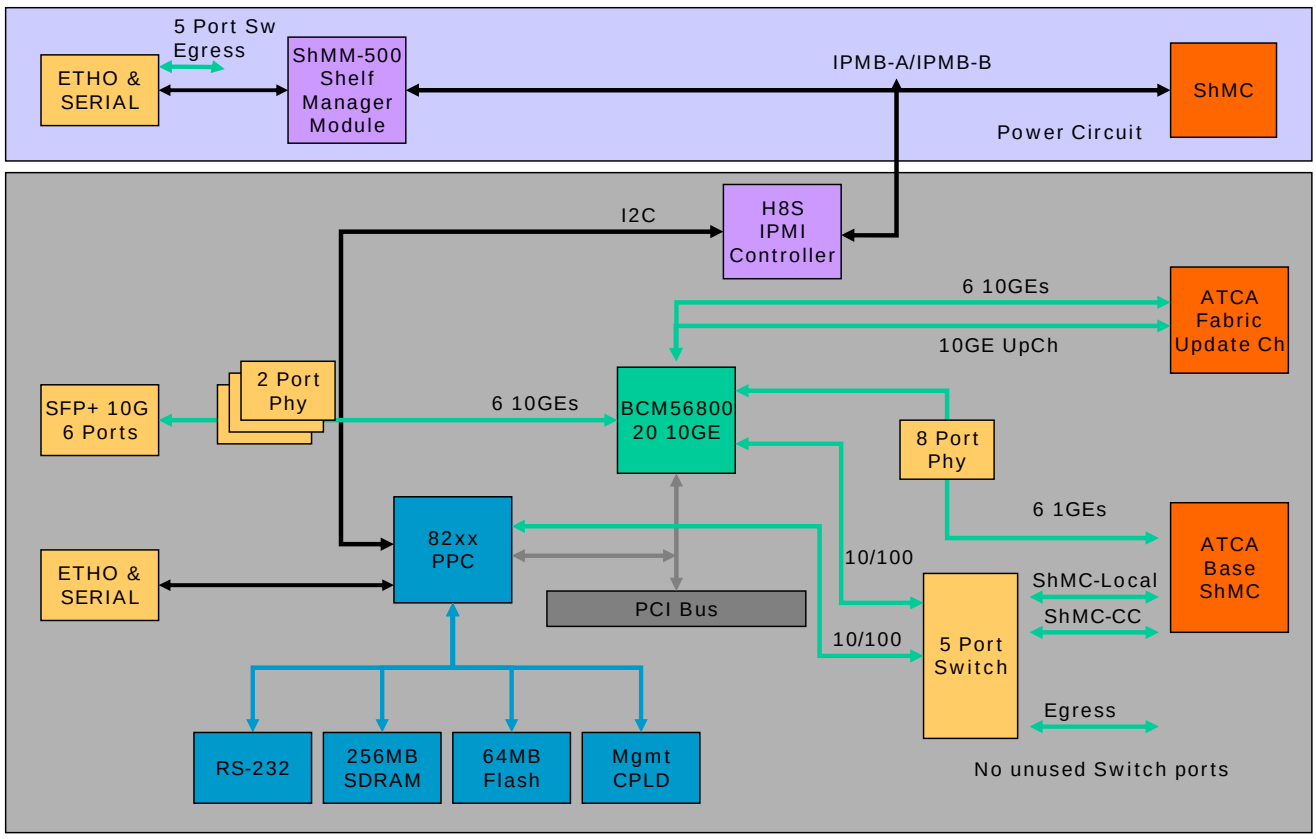
Backplane Routing Table (BASE)

LOGICAL SLOT#		SWA	SWB	S1	S2	S3	S4	S5	S6
CONNECTOR	BASE CHANNEL								
P24	CH1	S1-CH1	S1-CH2	SA-CH1	SA-CH2	SA-CH3	SA-CH4	SA-CH5	SA-CH6
P24	CH2	S2-CH1	S2-CH2	SB-CH1	SB-CH2	SB-CH3	SB-CH4	SB-CH5	SB-CH6
P24	CH3	S3-CH1	S3-CH2						
P24	CH4	S4-CH1	S4-CH2						
P24	CH5	S5-CH1	S5-CH2						
P23	CH6	S6-CH1	S6-CH2						
~~P24~~	~~CH7~~								
~~P24~~	~~CH8~~								
~~P24~~	~~CH9~~								
~~P24~~	~~CH10~~								
~~P24~~	~~CH11~~								
~~P24~~	~~CH12~~								
~~P24~~	~~CH13~~								
~~P24~~	~~CH14~~								
~~P24~~	~~CH15~~								
~~P24~~	~~CH16~~								
UPDATE CH		SWA	SWB	S1	S2	S3	S4	S5	S6
		↔		↔		↔		↔	

Backplane Routing Table (FABRIC)

LOGICAL SLOT#		SWA	SWB	S1	S2	S3	S4	S5	S6
CONNECTOR	FABRIC CHANNEL								
~~P20~~	~~CH15~~	~~MESH 3~~		~~S6-CH11~~	~~S6-CH12~~	~~S6-CH13~~	~~S6-CH14~~	~~S6-CH15~~	~~S5-CH15~~
~~P20~~	~~CH14~~			~~S5-CH11~~	~~S5-CH12~~	~~S5-CH13~~	~~S5-CH14~~	~~S4-CH14~~	~~S4-CH15~~
~~P20~~	~~CH13~~			~~S4-CH11~~	~~S4-CH12~~	~~S4-CH13~~	~~S3-CH13~~	~~S3-CH14~~	~~S3-CH15~~
~~P21~~	~~CH12~~			~~S3-CH11~~	~~S3-CH12~~	~~S2-CH12~~	~~S2-CH13~~	~~S2-CH14~~	~~S2-CH15~~
~~P21~~	~~CH11~~			~~S2-CH11~~	~~S1-CH11~~	~~S1-CH12~~	~~S1-CH13~~	~~S1-CH14~~	~~S1-CH15~~
~~P21~~	~~CH10~~	~~MESH 2~~		~~S6-CH6~~	~~S6-CH7~~	~~S6-CH10~~	~~S6-CH10~~	~~S6-CH10~~	~~S5-CH10~~
~~P21~~	~~CH9~~			~~S5-CH6~~	~~S5-CH7~~	~~S5-CH9~~	~~S5-CH9~~	~~S4-CH9~~	~~S4-CH10~~
~~P21~~	~~CH8~~			~~S34-CH6~~	~~S4-CH7~~	~~S4-CH8~~	~~S3-CH8~~	~~S3-CH9~~	~~S3-CH10~~
P22	CH7	SB-UP	SA-UP	~~S3-CH6~~	~~S3-CH7~~	~~S2-CH7~~	~~S2-CH8~~	~~S2-CH9~~	~~S2-CH10~~
P22	CH6	S6-CH1	S6-CH2	~~S2-CH6~~	~~S1-CH6~~	~~S1-CH7~~	~~S1-CH8~~	~~S1-CH9~~	~~S1-CH10~~
P22	CH5	S5-CH1	S5-CH2	~~MESH 1~~		~~S6-CH3~~	~~S6-CH4~~	~~S6-CH5~~	~~S5-CH5~~
P22	CH4	S4-CH1	S4-CH2			~~S5-CH3~~	~~S5-CH4~~	~~S4-CH4~~	~~S4-CH5~~
P22	CH3	S3-CH1	S3-CH2	~~S2-CH3~~	~~S1-CH3~~	~~S4-CH3~~	~~S3-CH3~~	~~S3-CH4~~	~~S3-CH5~~
P23	CH2	S2-CH1	S2-CH2	SB-CH1	SB-CH2	SB-CH3	SB-CH4	SB-CH5	SB-CH6
P23	CH1	S1-CH1	S1-CH2	SA-CH1	SA-CH2	SA-CH3	SA-CH4	SA-CH5	SA-CH6

Backplane is to be comprised of a Dual Star Fabric Channel Configuration design with Serial Ethernet links routed to the appropriate Shelf Manager/Switch slots: SWA and SWB.



Notes:

- Power circuits not shown
- Clock circuits not shown
- Reset button not shown

Design Considerations

The Schroff backplane and enclosure modifications will be outsourced to Schroff to complete. The design of the Shelf/Switch card will be performed by Znyx. A documentation release of the ShMM-ACB-V will be necessary to gain a complete overview of the scope of the design work for the Shelf/Switch. The documents needed are: schematics of the ACB-V, BOM, mechanical PCB drawing, Fab drawings, Assembly drawings, bracket drawings, programmable logic source files (if any), ShMM-ACB-V test records and test procedures.

The Shelf/Switch design will be optimized for time to market without sacrificing any current ShMC functionality and minor modifications to existing software base (ShMC and Switch). The Znyx Switch and the Schroff Shelf Manager currently operate as independent entities within the chassis. How the Shelf/Switch integrates these separate entities into a cohesive product is a matter left for the engineering design teams (HW, SW, ShMC, etc).

Backplane Shelf Manager Slot Connectors for Slot A and Slot B

Connector	Location	Connector Type	Function
ShMC	Backplane – J2	Z-Pack 2mm HM	IPMB ShMC Interface
ATCA Zone 2	Backplane – J22	Z-Pack HM-ZD connector	ATCA Base/Fabric Channels
ATCA Zone 2	Backplane – J23,J24	Z-Pack HM-ZD connector	ATCA Base/Fabric Channels
Power	Backplane – P10	Universal Power connector	Dual -48V Power Rails

ShMC connector – ERNI 114154 or Tyco 5646574-1 (Type AB, 25 pos, 5 row, without shield)

ATCA Zone 2 connector:
(J22) – Tyco 6469001-1 or ERNI 973032; 40 Pair HM-ZD
(J23 & J24) – Tyco 6469028-1; 20 Pair HM-ZD

Power connectors (P10) - Tyco 5646954-3 (Backplane Mate = Tyco 522395-1 or Tyco 120953-1)

ShMC J2 (J2) - Backplane ShMC Connector pin assignment

This Backplane Signal connector merges the ACB-V J1and J2 pins into a single connector. ShMC Connector provides Clock and IPMB Connections to Payload Boards and Update port from ShMC/Switch to ShMC/Switch. It also has HotSwap, Presence Detection and Fan Tachometer Control from the J1 connector.

Pin	Pin Name	Description (ShMC Specific) J2 Connector
1A	GND	Logic Ground
2A	ETH1_TX+	Ethernet interface (ETH1) Positive Output (Micrel Switch)
3A	ETH1_RX+	Ethernet interface (ETH1) Positive Input (Micrel Switch)
4A	GND	Logic Ground
5A	SWR_Input#	Switchover signal from the other Shelf Manager

Pin	Pin Name	Description (ShMC Specific) J2 Connector
6A	SWR_Output#	Switchover signal to the other Shelf Manager
7A	IPMB_SDA_A	Backplane Serial Data, IPMB A
8A	Reserved	Future Use
9A	N/A	Not Available
10A	FAN_TACH0	Tachometer signal from Fan Tray
11A	N/A	Not Available
12A	FAN_TACH5	Tachometer signal from Fan Tray
13A	N/A	Not Available
14A	GND	Logic Ground
15A	ETHCC_TX+	Ethernet interface (ETHCC) Positive (Cross Connect Partner)
16A	ETHCC_RX+	Ethernet interface (ETHCC) Positive (Cross Connect Partner)
17A	GND	Logic Ground
18A	SDA_CH1	Master Only-I2C-bus Channel 1
19A	SCL_CH3	Master Only-I2C-bus Channel 3
20A	GND	Logic Ground
21A	CLK1A+	Synchronization Clock (unused)
22A	CLK2A+	Synchronization Clock (unused)
23A	CLK3A+	Synchronization Clock (unused)
24A	GND	Logic Ground
25A	TX4[UP]+	Update Channel (unused)
1B	GND	Logic Ground
2B	ETH1_TX-	Ethernet interface (ETH1) Negative Output
3B	ETH1_RX-	Ethernet interface (ETH1) Negative Input
4B	GND	Logic Ground
5B	HLY_Input#	Health of the other Shelf Manager
6B	HLY_Output#	Health of this Shelf Manager
7B	IPMB_SCL_A	Backplane Serial Clock, IPMB_A
8B	Reserved	Future Use
9B	N/A	Not Available
10B	FAN_TACH1	Tachometer signal from Fan Tray
11B	N/A	Not Available
12B	PWM_C	Opto-isolated PWM signal for fan speed control; collector pin (max 70V, 2mA)
13B	N/A	Not Available
14B	GND	Logic Ground
15B	ETHCC_TX-	Ethernet interface (ETHCC) Negative (Cross Connect Partner)
16B	ETHCC_RX-	Ethernet interface (ETHCC) Negative (Cross Connect Partner)
17B	GND	Logic Ground
18B	SCL_CH1	Master Only-I2C-bus Channel 1
19B	SDA_CH3	Master Only-I2C-bus Channel 3
20B	GND	Logic Ground
21B	CLK1A-	Synchronization Clock (unused)
22B	CLK2A-	Synchronization Clock (unused)
23B	CLK3A-	Synchronization Clock (unused)
24B	GND	Logic Ground
25B	TX4[UP]-	Update Channel (unused)
1C	GND	Logic Ground
2C	FAN_PRES0	Fan Tray present (grounded when present)

Pin	Pin Name	Description (ShMC Specific) J2 Connector
3C	PRES_OUT#	GND Connection for PRES_1# of other Shelf Manager
4C	GND	Logic Ground
5C	HA[0]	Hardware Address of Shelf Manager, bit 0
6C	HA[7]	Hardware Address of Shelf Manager, bit 7 (Parity)
7C	IPMB_SDA_B	Backplane Serial Data, IPMB B
8C	Reserved	Future Use
9C	N/A	Not Available
10C	FAN_TACH2	Tachometer signal from Fan Tray
11C	N/A	Not Available
12C	FAN_24V	Aux 24VDC (max 100A) generated on Fan Trays (V-Supply for ShM opto-couplers)
13C	N/A	Not Available
14C	GND	Logic Ground
15C	GND	Logic Ground
16C	GND	Logic Ground
17C	GND	Logic Ground
18C	SDA_CH2	Master Only-I2C-bus Channel 2
19C	SCL_CH4	Master Only-I2C-bus Channel 4
20C	GND	Logic Ground
21C	GND	Logic Ground
22C	GND	Logic Ground
23C	GND	Logic Ground
24C	GND	Logic Ground
25C	GND	Logic Ground
1D	GND	Logic Ground
2D	FAN_PRES1	Fan Tray present (grounded when present)
3D	AIR_FILT_PR	Air filter presence (connected to switch to detect a missing air filter)
4D	Reserved	Future Use
5D	PRES_IN#	Board presence signal from other Shelf Manager to this Shelf Manager
6D	HS_EN#	Tells the Shelf Manager that it is plugged in
7D	IPMB_SCL_B	Backplane Serial Clock, IPMB_B
8D	Reserved	Future Use
9D	N/A	Not Available
10D	FAN_TACH3	Tachometer signal from Fan Tray
11D	N/A	Not Available
12D	FAN_24V_RTN	Return path (Gnd) 24VDC generated on Fan Trays (Ref Gnd for fan control voltage)
13D	N/A	Not Available
14D	Reserved	Future Use
15D	S2_TX+	USB interface to other Shelf Manager
16D	S2_RX+	USB interface to other Shelf Manager
17D	GND	Logic Ground
18D	SCL_CH2	Master Only-I2C-bus Channel 2
19D	SDA_CH4	Master Only-I2C-bus Channel 4
20D	GND	Logic Ground
21D	CLK1B+	Synchronization Clock (unused)
22D	CLK2B+	Synchronization Clock (unused)
23D	CLK3B+	Synchronization Clock (unused)
24D	GND	Logic Ground

Pin	Pin Name	Description (ShMC Specific) J2 Connector
25D	RX4[UP]+	Update Channel (unused)
1E	GND	Logic Ground
2E	PEM_PRES_A	PEM [A] presence (grounded when present)
3E	PEM_PRES_B	PEM [B] presence (grounded when present)
4E	Reserved	Future Use
5E	Reserved	Future Use
6E	Reserved	Future Use
7E	Reserved	Future Use
8E	Reserved	Future Use
9E	N/A	Not Available
10E	FAN_TACH4	Tachometer signal from Fan Tray
11E	N/A	Not Available
12E	PWM_E	Opto-isolated PWM signal for fan speed control (backplane connect to FAN_24V_RTN)
13E	N/A	Not Available
14E	Reserved	Future Use
15E	S2_TX-	USB interface to other Shelf Manager
16E	S2_RX-	USB interface to other Shelf Manager
17E	GND	Logic Ground
18E	I2C_PWR_B	3.3V power redundant path B for Shelf I2C devices
19E	I2C_PWR_A	3.3V power redundant path A for Shelf I2C devices
20E	GND	Logic Ground
21E	CLK1B-	Synchronization Clock (unused)
22E	CLK2B-	Synchronization Clock (unused)
23E	CLK3B-	Synchronization Clock (unused)
24E	GND	Logic Ground
25E	RX4[UP]-	Update Channel (unused)

Sw J22 Backplane Signal Connector pin assignment

This Backplane Signal connector provides Fabric and Update Channel Connections to Payload Boards.

Pin	Pin Name	Description (ATCA Zone 2) J22 Connector
1A	TX2[UP]+	Update Channel; Inter Switch Link (ISL)
1B	TX2[UP]-	
1C	RX2[UP]+	
1D	RX2[UP]-	
1E	TX3[UP]+	
1F	TX3[UP]-	
1G	RX3[UP]+	
1H	RX3[UP]-	
2A	TX0[UP]+	
2B	TX0[UP]-	
2C	RX0[UP]+	
2D	RX0[UP]-	
2E	TX1[UP]+	
2F	TX1[UP]-	
2G	RX1[UP]+	
2H	RX1[UP]-	

Pin	Pin Name	Description (ATCA Zone 2) J22 Connector
3A	TX2[6]+	Fabric Interface Ch 6
3B	TX2[6]-	
3C	RX2[6]+	
3D	RX2[6]-	
3E	TX3[6]+	
3F	TX3[6]-	
3G	RX3[6]+	
3H	RX3[6]-	
4A	TX0[6]+	
4B	TX0[6]-	
4C	RX0[6]+	
4D	RX0[6]-	
4E	TX1[6]+	
4F	TX1[6]-	
4G	RX1[6]+	
4H	RX1[6]-	
5A	TX2[5]+	Fabric Interface Ch 5
5B	TX2[5]-	
5C	RX2[5]+	
5D	RX2[5]-	
5E	TX3[5]+	
5F	TX3[5]-	
5G	RX3[5]+	
5H	RX3[5]-	
6A	TX0[5]+	
6B	TX0[5]-	
6C	RX0[5]+	
6D	RX0[5]-	
6E	TX1[5]+	
6F	TX1[5]-	
6G	RX1[5]+	
6H	RX1[5]-	
7A	TX2[4]+	Fabric Interface Ch 4
7B	TX2[4]-	
7C	RX2[4]+	
7D	RX2[4]-	
7E	TX3[4]+	
7F	TX3[4]-	
7G	RX3[4]+	
7H	RX3[4]-	
8A	TX0[4]+	
8B	TX0[4]-	
8C	RX0[4]+	
8D	RX0[4]-	
8E	TX1[4]+	
8F	TX1[4]-	
8G	RX1[4]+	

Pin	Pin Name	Description (ATCA Zone 2) J22 Connector
8H	RX1[4]-	
9A	TX2[3]+	Fabric Interface Ch 3
9B	TX2[3]-	
9C	RX2[3]+	
9D	RX2[3]-	
9E	TX3[3]+	
9F	TX3[3]-	
9G	RX3[3]+	
9H	RX3[3]-	
10A	TX0[3]+	
10B	TX0[3]-	
10C	RX0[3]+	
10D	RX0[3]-	
10E	TX1[3]+	
10F	TX1[3]-	
10G	RX1[3]+	
10H	RX1[3]-	

Sw J23 (J23A & J23B)– Backplane Signal Connector pin assignment

This Backplane Signal connector provides Base and Fabric Connections to Payload Boards. The Base port sequence for J23 is different from the normal ATCA port sequence. This is by design for improved port routing to the Switch chip.

Pin	Pin Name	Description (ATCA Zone 2) J23 Connector
1A	TX2[2]+	Fabric Interface Ch 2
1B	TX2[2]-	
1C	RX2[2]+	
1D	RX2[2]-	
2A	TX3[2]+	
2B	TX3[2]-	
2C	RX3[2]+	
2D	RX3[2]-	
3A	TX0[2]+	
3B	TX0[2]-	
3C	RX0[2]+	
3D	RX0[2]-	
4A	TX1[2]+	
4B	TX1[2]-	
4C	RX1[2]+	
4D	RX1[2]-	
5A	TX2[1]+	Fabric Interface Ch 1
5B	TX2[1]-	
5C	RX2[1]+	
5D	RX2[1]-	
6A	TX3[1]+	
6B	TX3[1]-	
6C	RX3[1]+	
6D	RX3[1]-	

Pin	Pin Name	Description (ATCA Zone 2) J23 Connector
7A	TX0[1]+	
7B	TX0[1]-	
7C	RX0[1]+	
7D	RX0[1]-	
8A	TX1[1]+	
8B	TX1[1]-	
8C	RX1[1]+	
8D	RX1[1]-	
9A	BI_DA[6]+	Base Interface Ch 6
9B	BI_DA[6]-	
9C	BI_DB[6]+	
9D	BI_DB[6]-	
10A	BI_DC[6]+	
10B	BI_DC[6]-	
10C	BI_DD[6]+	
10D	BI_DD[6]-	

Sw J24 Backplane Signal Connector pin assignment

This Backplane Signal connector provides Base and Fabric Connections to Payload Boards. The Base port sequence for J24 is different from the normal ATCA port sequence. This is by design for improved port routing to the Switch chip.

Pin	Pin Name	Description (ATCA Zone 2) J24 Connector
1A	BI_DA[5]+	Base Interface Ch 5
1B	BI_DA[5]-	
1C	BI_DB[5]+	
1D	BI_DB[5]-	
2A	BI_DC[5]+	
2B	BI_DC[5]-	
2C	BI_DD[5]+	
2D	BI_DD[5]-	
3A	BI_DA[4]+	Base Interface Ch 4
3B	BI_DA[4]-	
3C	BI_DB[4]+	
3D	BI_DB[4]-	
4A	BI_DC[4]+	
4B	BI_DC[4]-	
4C	BI_DD[4]+	
4D	BI_DD[4]-	
5A	BI_DA[3]+	Base Interface Ch 3
5B	BI_DA[3]-	
5C	BI_DB[3]+	
5D	BI_DB[3]-	
6A	BI_DC[3]+	
6B	BI_DC[3]-	
6C	BI_DD[3]+	
6D	BI_DD[3]-	
7A	BI_DA[2]+	Base Interface Ch 2

Pin	Pin Name	Description (ATCA Zone 2) J24 Connector
7B	BI_DA[2]-	
7C	BI_DB[2]+	
7D	BI_DB[2]-	
8A	BI_DC[2]+	
8B	BI_DC[2]-	
8C	BI_DD[2]+	
8D	BI_DD[2]-	
9A	BI_DA[1]+	Base Interface Ch 1
9B	BI_DA[1]-	
9C	BI_DB[1]+	
9D	BI_DB[1]-	
10A	BI_DC[1]+	
10B	BI_DC[1]-	
10C	BI_DD[1]+	
10D	BI_DD[1]-	

Sw P10 – Backplane Power Connector pin assignment

This Backplane Power connector provides dual -48VDC Power Connections to Shelf/Switch Board.

Pin	Pin Name	Description (ATCA Zone 1 like) P10 Connector
A(Long)	VRTN_A	Voltage Return supply A
B	-48V_A	-48 Volt DC supply A
C(Long)	VRTN_B	Voltage Return supply B
D	-48V_B	-48 Volt DC supply B

Backplane Routing Requirements

The Backplane provides the signal mirroring connections to each Shelf/Switch Board. Ports defined with the [TX]/[RX] are to be connected through the backplane such that the [TX] of one transmission pair is routed to the [RX] of the other transmission receiver pair.

The Backplane will support Redundancy Control as outlined in the Schroff 6Slot User Manual for 11596-160. The ZX2000 Shelf/Switches support redundant operation with automatic switchover using redundant Shelf Managers. In the configuration where two Shelf Managers are present, one acts as the active Shelf Manager and the other as a standby. The Shelf Managers monitor each other and either can trigger a switchover if necessary. The Switch Management software will also follow the Shelf Manager switchover accordingly.

Hardware Redundancy interfaces of the Shelf Manager are as follow: (See Figure 32 in 6Slot User Manual)

- Cross Connected Shelf Manager present input (PRES_1#) and output (PRES_GND#)
- Cross Connected Shelf Manager health input (HLY_Input#) and output (HLY_Output#)
- Cross Connected negotiation input (SWR_Input#) and output (SWR_Output#)
- Active output from the ShMM-500 (ACTIVE#) that is used by the Shelf Manager to enable interfaces that must be exclusively driven the the active Shelf Manager, specifically PWM and tan tachometer buffers.
- Two status LEDs using the SWSLED_G# (Green) and SWS_LED_R# (Red) signals.
- The PRES_1# signal is grounded on the redundant Shelf Manager. This indicates to both Shelf Managers the presence of the other.

ZX2010 Port Mapping

Device	Software Device Port #	Backplane Connection	PHY Transceiver [Phy Addr]	Media Protocol	END TERMINATION
MPC8270					
0	uP-eth0	EGRESS	KS8721 [10H]	10/100	FRONT PANEL RJ45
1	uP-eth1	Local	MII	10/100	Micrel Switch
2	uP-eth2	NC			NC
ShMM-500					
0	Sh-eth0	Local Switch		10/100	Local Micrel Switch
1	Sh-eth1	Cross Connect		10/100	ShMM Backplane Connector
BCM56800					
1	zre0	ShMC/Local	BCM54980.8 [08H]	10/100	Micrel Switch
2	zre1	BASE CH 3	BCM54980.1 [01H]	1000 BaseT	Physical Slot 1
3	zre2	BASE CH 4	BCM54980.2 [02H]	1000 BaseT	Physical Slot 2
4	zre3	BASE CH 5	BCM54980.3 [03H]	1000 BaseT	Physical Slot 3
5	zre4	BASE CH 6	BCM54980.4 [04H]	1000 BaseT	Physical Slot 4
6	zre5	BASE CH 7	BCM54980.5 [05H]	1000 BaseT	Physical Slot 5
7	zre6	BASE CH 8	BCM54980.6 [06H]	1000 BaseT	Physical Slot 6
8	zre7	FABRIC CH 2		SERIAL 1G/10G	Physical Slot 1
9	zre8	FABRIC CH 3		SERIAL 1G/10G	Physical Slot 2
10	zre9	FABRIC CH 4		SERIAL 1G/10G	Physical Slot 3
11	zre10	FABRIC CH 5		SERIAL 1G/10G	Physical Slot 4
12	zre11	FABRIC CH 6		SERIAL 1G/10G	Physical Slot 5
13	zre12	FABRIC CH 7		SERIAL 1G/10G	Physical Slot 6
14	zre13	UPDATE CH		SERIAL 1G/10G	Inter Switch Link
15	zre14	EGRESS	BCM8727.1 [10H]	1G/10G SFP+	FRONT PANEL SFP+
16	zre15	EGRESS	BCM8727.2 [11H]	1G/10G SFP+	FRONT PANEL SFP+
17	zre16	EGRESS	BCM8727.1 [12H]	1G/10G SFP+	FRONT PANEL SFP+
18	zre17	EGRESS	BCM8727.2 [13H]	1G/10G SFP+	FRONT PANEL SFP+
19	zre18	EGRESS	BCM8727.1 [14H]	1G/10G SFP+	FRONT PANEL SFP+
20	zre19	EGRESS	BCM8727.2 [15H]	1G/10G SFP+	FRONT PANEL SFP+
Micrel Switch					
1		EGRESS		10/100	FRONT PANEL RJ45
2	Sh-eth0	ShMM-500(1)		10/100	Local ShMM eth0
3	ETHCC	BACKPLANE		10/100	Cross Connect Partner
4	zre0	BCM56800(0)		10/100	Local BCM Switch
5	uP-eth1	MPC8270(1)		MII	Local MPC CPU

PCI Device ID

Device	PCI IDSEL Addr #
MPC82xx	20
BCM Switch Device	21

Power

The ZX2000 draws bulk current from the dual -48V rails of P10 connector only. On-board voltage regulators provide requirements for other voltages. Overall power budget is estimated to be 100W max.

Power	Max Current	Tolerance	IPMC A_Input	Comments
+1.5V	6A	+/- 5%	AN0	Converted from main +3.6V
+1.0VA	30A	+/- 5%	AN1	Converted from main +3.6V; For BCM56800
+1.0VB	10A	+/- 5%	AN2	Converted from main +3.6V; For BCM8727s
+2.5V	6A	+/- 5%	AN3	Converted from main +3.6V
+3.3V	6A	+/- 5%	AN4	Converted from main +3.6V
+3.6V	22A	+/- 5%	AN5	Main Voltage from -48VDC converter (1/16 Brick)
+3.3VSB	8A	+/- 5%	AN6	Standby +3.3V from PIM300 module

Hardware Address

The PCA9554 on the ACB-V reads the hardware address and parity bit from the backplane connector on the Shelf Manager slot. Geographic address pins (HA[0], HA[7]) determine bit 0 and 7 with bits 1 and 6 **hardcoded in BOLD** for both the Shelf Manager and the Switch. The ShMM-500 software determines the hardware address by reading the input port register of the PCA9554 at address 0x46. HW Addresses are modified from existing standard 11596-160 chassis. While the Shelf Manager and the Switch are both located on the same physical card, it is necessary to have each respond to a different address space to ensure compatibility with existing standard 14 slot chassis configurations. HA[7] is set for ODD Parity.

Device/Physical/Logical Slot	HW Addr #	IPMB Addr #	Update Ch
Shelf Manager Slot A	**0x08**	10	-
Shelf Manager Slot B	**0x09**	12	-
Switch Slot A	**0x41**	82	↕
Switch Slot B	**0x42**	84	
Node 6	0x48	90	↕
Node 5	0x47	8E	
Node 4	0x46	8C	↕
Node 3	0x45	8A	
Node 2	0x44	88	↕
Node 1	0x43	86	

I²C Address of the Shelf

The master-only I²C bus is used internally on the ShMM-500 for the RTC and SEEPROM devices. The Shelf Manager ShMM-ACB-V also has a number of onboard I²C devices connected to the master–only I²C bus. These devices read the slot's hardware address, communicate with the System Management controllers ADM1024/1026 and monitor the presence signals from the PEMs and Fan Trays. The 'Active' signal of the ShMM-500 is used to enable the I²C switch and the LTC4300 buffer, so that only the active Shelf Manager has access to the Shelf I²C-bus devices.

I²C Address	ShMM	ACB-V	CH 1	CH 2	CH 3	CH 4
0x46 / 23		PCA9554 HW-ADDR				
0x48 / 24					PCA9555 Fan Tray 0	PCA9555 PEM A
0x4A / 25					PCA9555 Fan Tray 1	PCA9555 PEM B
0x4C / 26					~~PCA9555 Fan Tray 2~~	
0x4E / 27		PCA9555 GPIO				
0x58 / 2C		~~ADM1024~~				
0x5C / 2E		ADM1026				
0x90 / 48					~~LM75 temp sensor~~	
0x92 / 49					~~LM75 temp sensor~~	
0x94 / 4A					~~LM75 temp sensor~~	
0x98 / 4C					LM75 temp sensor	LM75 PEM A
0x9A / 4D					LM75 temp sensor	LM75 PEM B
0x9C / 4E					~~LM75 temp sensor~~	
0xA0 / 50	SEEPROM					
0xA4 / 52			SEEPROM 1 CDM	SEEPROM 2 CDM		
0xA8 / 54					SEEPROM Fan Tray 0	SEEPROM PEM A
0xAA / 55					SEEPROM Fan Tray 1	SEEPROM PEM B
0xAC / 56					~~SEEPROM Fan Tray 2~~	
0xE0/ 70		PCA9545 I²C bus switch				
0xD0 / 68	RTC DS1337					

I²C Address of the Switch

The ZX2010 uses I²C for both ATCA compliance and on-board communication. The architecture provides for an I²C bus for the main embedded processor (MPC8270) and the IPMC system management processor (H8S).

The MPC8270 processor acts as an I²C bus master for the devices shown in the following table.

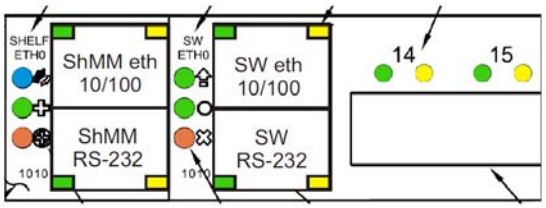
Device	Mux Bit	I²C Addr #	Comment
SEEPROM		0xA6	Stores ZMON ZFS and VPD
I²C PCA9548 MUX		0xE0	Required to access SFP+ modules
SFP+	0	0xA0	PCA9548A Mux port 0
SFP+	1	0xA0	PCA9548A Mux port 1
SFP+	2	0xA0	PCA9548A Mux port 2
SFP+	3	0xA0	PCA9548A Mux port 3
SFP+	4	0xA0	PCA9548A Mux port 4
SFP+	5	0xA0	PCA9548A Mux port 5
MICREL	6	0xA0	MICREL 5 PORT SW

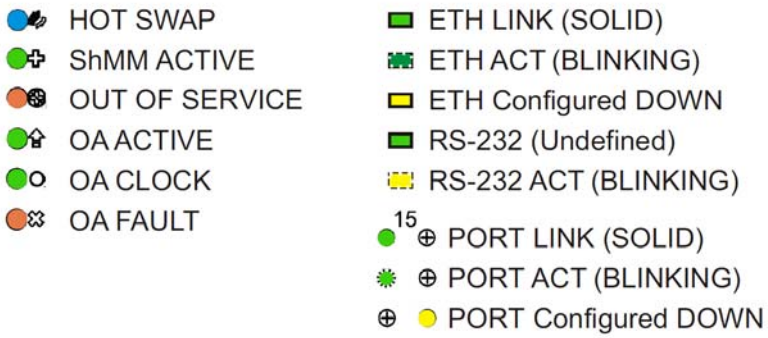
The H8S processor (as the system IPMC) acts as an I²C bus master for its own local.

Device	I²C Addr #	Comment
SEEPROM	0XA0	Stores FRU information
Thermal Sensor	0x90	Sensor 0
Thermal Sensor	0x92	Sensor 1

LED/Displays

Name	Color	Graphic	Location	Description
HOTSWAP	Blue		Front Bracket	Driven by the Shelf Manager.
ShMM ACTIVE	Green		Front Bracket	Driven by either Shelf Manager.
SM/SW OOS	Orange		Front Bracket	Driven by either Shelf Manager & H8S IPMC.
OA ACTIVE	Green		Front Bracket	Driven by Znyx OA software.
OA CLOCK	Green		Front Bracket	Driven by Znyx OA software.
OA FAULT	Orange		Front Bracket	Driven by Znyx OA software.
SM-OOB LINK/ACT	Green	N/A	RJ45	Driven by Micrel 5 port Sw.
	Amber	N/A	RJ45	
SW-OOB LINK/ACT	Green	N/A	RJ45	Driven by Znyx OA software for uP-eth0.
SW-OOB DOWN	Amber	N/A	RJ45	Driven by Znyx OA software for uP-eth0.
SFP+ Port Leds	Green Amber	N/A	Front Bracket Port 14-19 SFP+	Dual LED per SFP+ Port for Link and Activity Green Steady = 1G/10G Port Link Green Blink = 1G/10G Port Activity Amber Steady = Link Software Configured Down Amber OFF = Link Software Configured Up





LED Behavior

This section documents how the LEDs that are not associated with network ports behave during all defined conditions, described from the point of view of the system operator. Beyond the reset state, all LEDs are under control of software running in one or more of the IPMC, ShMC, and PowerPC processors. Although the software specifications are outside the scope of this document, the end result of how the LED functions are defined here.

Lamp-Test Behavior

The ZX2010 provides a register bit accessible by the PowerPC that implements a lamp test. When set, all the LEDs on the ZX2010 front panel and RJ45s will be in the ON state regardless of other inputs. When not set, the LEDs operate as described below.

HotSwap LED

The behavior of the HotSwap LED will be consistent with the ATCA specification. The LED and its corresponding HotSwap switch is connected to and driven by the ShMM-500 device, which will operate it as if it were hosted on a conventional CMM carrier. The behavior summary is as follows:

LED Condition	Meaning
OFF	This indicates one of the following conditions: 1. The ZX2010 does not have power. 2. The ZX2010 ShMC firmware has failed to boot. 3. The ZX2010 is in normal operation. This condition will be corroborated by other LEDs.
Blinking	The ZX2010 is in a transitional state. This has two sub modes as defined by the manufacturer's specification: 1. Long blink cycle means the transition is from deactivated to active. 2. Short blink cycle means the transition is from activated to deactive.
ON	The ZX2010 may be extracted.

ShMM Active LED

This LED is provided to indicate the Active/Standby state of the ShMM-500. In a properly functioning ZX2000 system, only one ShMM-500 can be active at one time. If the Active LEDS on both ZX2010s in a single ZX2000 chassis are on at the same time for more than a brief tranisitional period, this should be considered an error condition requiring software diagnostics.
This LED has one color, and is driven by the ShMM-500 device.

LED Condition	Meaning
OFF	This indicates one of the following conditions: 1. The ZX2010 does not have power. 2. ShMM-500 is not in the Active State.
Blinking	The ZX2010 is in the Standby mode.
ON	The ZX2010 is in the Active State.

OOS LED

The Out-Of-Service (OOS) LED is conventionally active when the FRU is not in service for one reason or another. In the case of the ZX2000, it represents the logical OR of the OOS state of the ShMM-500 and the payload. This table shows the resulting interpretation.

LED Condition	Meaning
OFF	This indicates one of the following conditions: 1. The ZX2010 does not have 48V input power. This will not be the case if any other LEDs are on. 2. The ZX2010 is in service.
ON	This indicates one of the following conditions are true: 1. The ShMM-500 is Out of Service. 2. The payload power on the ZX2010 has been turned off by the IPMC.

Examining the other LEDs may refine the significance of the OOS LED when it is in the ON state. For example, if the OA CLK LED is blinking when the OOS LED is ON, then it can be inferred that the ShMM-500 is out of service instead of the ZX2010 payload section.

OA Active LED

This LED is driven by the OA Software to indicate Active state according to the following table:

LED Condition	Meaning
OFF	The OA instance is either not booted or is not in an Active state.
ON	The OA instance is in the Active state.

Unlike the ShMM-5000, it is not an error state for both OA Active LEDs to be ON at the same time, since this is a supported configuration.

OA Clock LED

After the reset this LED is blinked by a software routine within the OpenArchitect at roughly 1Hz to indicate that the software (and processor it is running in) is operating normally. This function is identical to all prior implementations of OpenArchitect.

OA Fault LED

The OA Fault LED is driven by software within OpenArchitect. This software can have any number of user-settable fault conditions that can be reported. For example prior implementations have defined the "EXT FAULT" LED to indicate the condition where some configured link does not have link-up status.

In addition, the Watch Dog Timer (WDT) circuit may drive this bit if enabled by OpenArchitect. If the WDT is enabled, and if the WDT-Fault indicator is enabled, this LED will be turned on if the WDT resets the OA Processor. This allows the LED to indicate that the OA software crashed and let the WDT expire.

LED Condition	Meaning
OFF	The OA instance is either not booted or no Fault condition is detected.
ON	OpenArchitect has determined that one or more of the configured fault conditions is true, or the WDT-Fault indicator feature was enabled and the WDT expired.

The list of supported fault conditions and how they are configured can be found in the OpenArchitect reference manual.

User Controls

Marking	Type	Location	Description
Reset	3-Pin Header	Front bracket, upon customer request. Connector would be used to provide cabling of reset button to front panel.	Reset/Lamp test. When depressed, the ZX2010 Shelf/Switch is placed in the reset state, and all LEDs will be lit. When released, the ZX2010 Shelf/Switch is released from reset state. **Design constraints limited the Reset button to a 3 pin connector near the front panel. If needed, a wired reset button will be added to the front panel.
(none)	Ejector Handle	Single Handle located at bottom/right of Front bracket.	A microswitch is connected to the ejector latch and is opened when the tab is moved from its locked state. Connected to both ShMM-500 and H8S IPMC.

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Safety Standards

Standard	Description	Status
UL 1950 3rd Edition	United States	Test Pending
CAN/CSA 22.2 No 950 - 95	Canadian	Test Pending
IEC 950(1991) 2nd Edition with Amendments No. 1 (1992), No. 2 (1993), No 3 (1995), and No. 4 (1996) / CB Scheme	International	Test Pending

EN 60950 (1992) Amendments 1, 2, 3, 4, & 11	European Union	Test Pending

See ZNYX Networks document control for test results

RF Emission/Immunity

Standard	Class	Agency/Report Format	Description	Status
CFR 47, Part 15, Subpart B 1998 (ANSIC63.4 1992)	A	FCC	United States	
EN300-386-2 VI.1.3 (1997-12)	A	EN55022 (1998) EN50082-1 (1996)	European Union	
VCCI (ANSI C63.4-1992/ CISPR 22-1997)	A	VCCI	Japan/International	
AS/NZS 3548 (1997)	A	AS/NZS 3548	Australia/New Zeland	
ICES-003, Issue 3	A	ICES 003	Canada	
CNS 13438	A	BSMI	Taiwan	

See ZNYX Networks document control for test results.

Environmental

Specification	Unit Measure	Lower Limit	Upper Limit	Status/Comments
Ambient Temperature, Operating				
Ambient Temperature, Storage				
Ambient Humidity				
Vibration				
Altitude				
Flammability				

PCB Information

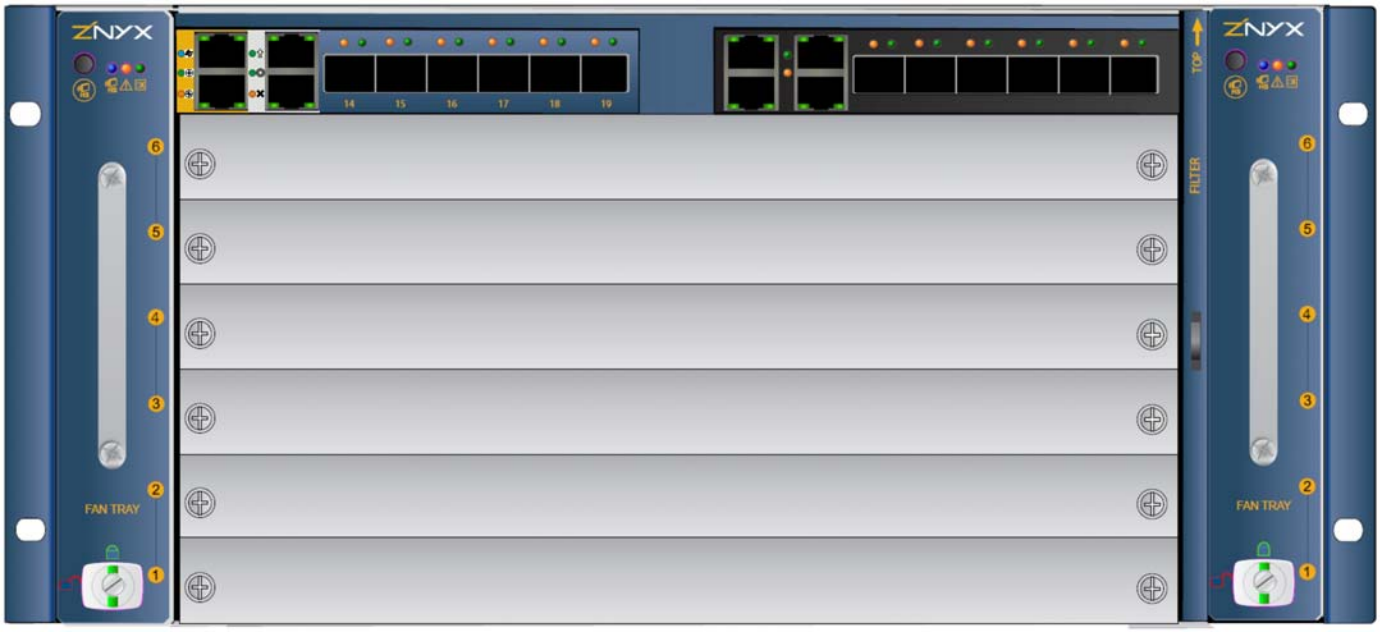
PCB Max Thickness is to be 2.4mm.

PCB Material is to be FR408HR.

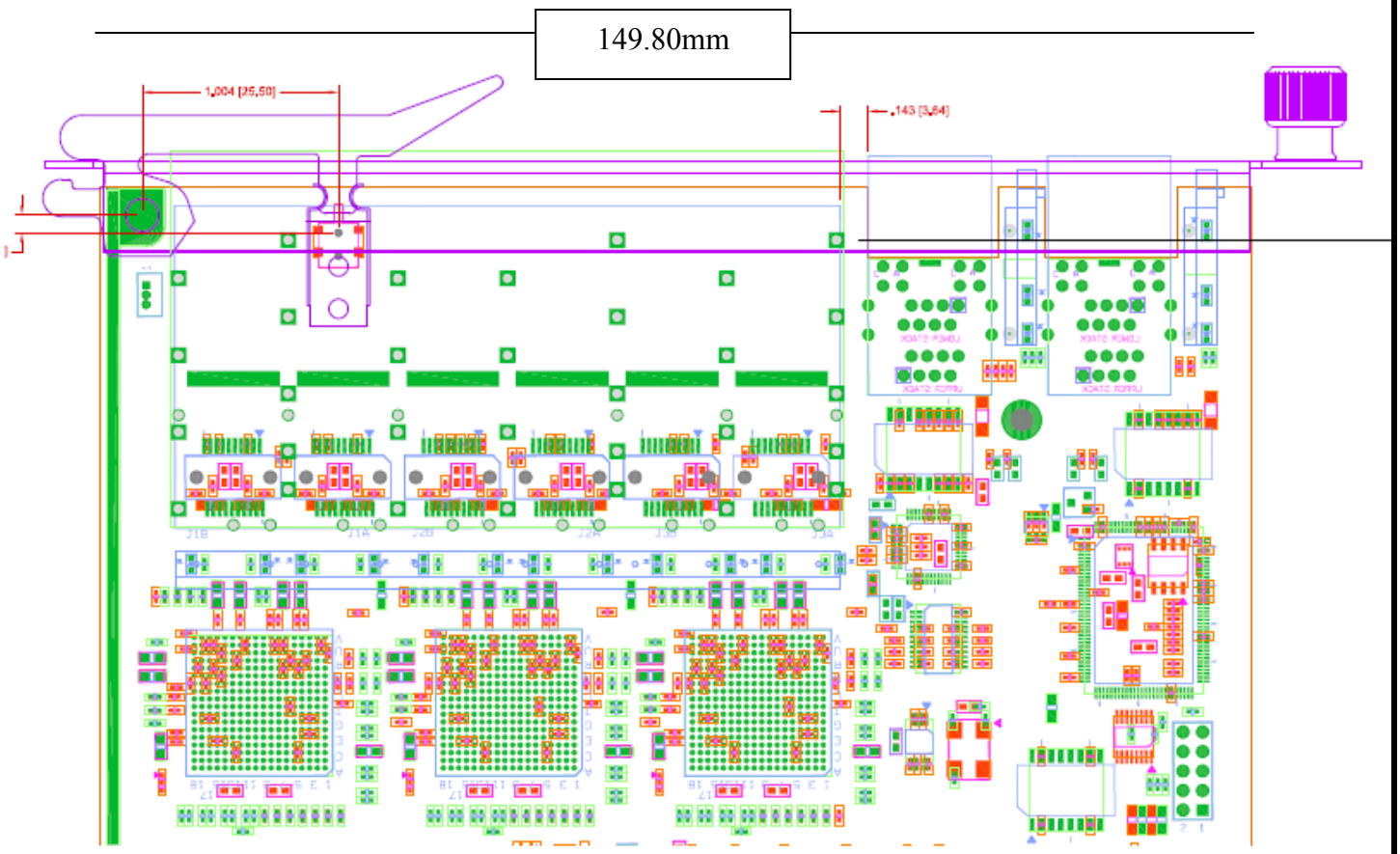
Stack-up Information is 16 LAYERS.

Appendix A

ZX2000 MockUp



Appendix B
ZX2000 Mechanical Drawing (Preliminary)



Full ATCA length [280.00m]