ANALOG DEVICES

ADV7612

Register Settings Recommendations

Revision 1.5

May 2014

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INTRODUCTION

This document describes ADI register setting recommendations and adjustments for the ADV7612. This document must be used in conjunction with the latest Hardware Manual / User Guide and Software Manual.

LEGAL TERMS AND CONDITIONS

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REVISION HISTORY

5/14—Rev. 1.4 to Rev. 1.5
Section 2.1 updated; write: 68 6F 0C changed to: 68 6F 08
Renamed all instances of 'ADI recommended setting' to 'ADI required setting'

1/14—Rev. 1.3 to Rev. 1.4
Section 2.1 updated; new write: 68 9B 03 write added
Low Frequency Formats section added (2.2.6)

08/13—Rev. 1.2 to Rev. 1.3
Pages 1-4 updated
Formatting updated throughout
Section 1 renamed ADV7612 I2C Addresses
Sections 1.2-1.3 renumbered 2.1-2.2 and grouped under
section 2 HDMI Receiver Register Settings

11/11—Rev. 1.1 to Rev. 1.2
HDMI Receiver Register Settings section modified :
new writes: 44 6C 00; 68 03 98; 68 4C 44
Equalizer Settings section modified

11/10—Rev. 1.0 to Rev. 1.1
Added recommended writes for non-fast switching scripts
Write removed from equalizer settings: 68 9D 02 ; ADI
Equalizer Setting

11/10—Revision 1.0: Initial Version

1   ADV7612 I2C ADDRESSES

The ADV7612includes the following programmable I²C map addresses :

I²C Addresses	
98 F4 80	CEC Map I²C address
98 F5 7C	INFOFRAME Map I²C address
98 F8 4C	DPLL Map I²C address
98 F9 64	KSV Map I²C address
98 FA 6C	EDID Map I²C address
98 FB 68	HDMI Map I²C address
98 FD 44	CP Map I²C address

The I²C addresses are programmed in the IO Map at the registers shown above.

The ADV7612 IO I²C Map address is non-programmable and its address is fixed to 0x98 or 0x9A depending on the configuration of the VS/ALSB/FIELD and SAMPLE_ALSB control (IO Map, Reg. 0x1B[0]). Refer to the ADV7612 Hardware User Guide (UG-216) for further information.

The I²C map addresses listed above are used throughout this document.

2   RECOMMENDED INITIALIZATION SETTINGS

2.1   INITIALIZATION SETTINGS FOR HDMI MODE

ADI recommends that these register settings are programmed to setup the ADV7612 correctly in HDMI mode.

CP Map	
44 6C 00	ADI required setting

HDMI Map	
68 9B 03	ADI required setting
68 6F 08	ADI required setting (optimized DVI detection)
68 85 1F	ADI required setting
68 87 70	ADI required setting
68 57 DA	ADI required setting
68 58 01	ADI required setting
68 03 98	Set DIS_I2C_ZERO_COMPR 0x03[7]=1
68 4C 44	Set NEW_VS_PARAM 0x4C[2]=1

For non-fast switching applications, the following settings are recommended :

HDMI Map	
68 C1 01	ADI required setting
68 C2 01	ADI required setting
68 C3 01	ADI required setting
68 C4 01	ADI required setting
68 C5 01	ADI required setting
68 C6 01	ADI required setting
68 C7 01	ADI required setting
68 C8 01	ADI required setting
68 C9 01	ADI required setting
68 CA 01	ADI required setting
68 CB 01	ADI required setting
68 CC 01	ADI required setting

2.2   DYNAMIC SETTINGS FOR HDMI

The following register settings and processes are required for the best performance.

2.2.1   Hot Plug Assert

To manually assert a hot plug, e.g. to replicate a down-stream hot plug in a repeater application, the following write should be used :

IO Map	
98 20 F8	Manually assert hot plug on port A
98 20 F4	Manually assert hot plug on port B

Following a manual assertion of the hot plug, the hot plug must also be manually de-asserted.

2.2.2   Free-run Operation

For best free-run performance, the following steps should be employed :

- Set PRIM_MODE to the desired free-run standard (IO Map, 0x01[3:0])
- Set VID_STD to the desired free-run standard (IO Map, 0x00[5:0])
- Set VFREQ to the frequency of the desired free-run standard (IO Map, 0x01[6:4])
- Set DIS_AUTO_PARAM_BUFF (CP Map, 0xC9[0]) to slave free-run parameters from PRIM_MODE and VID_STD
- Enable free-run mode (CP Map, 0xBF[0])

2.2.3   Power Down modes

The ADV7612 has two power down modes – power down mode 0 and power down mode 1.

- In power down mode 0 and power down mode 1, chassis supply is available.
- In power down mode 1 - CEC is powered up.
- In power down mode 0 - CEC is powered down.

To correctly power down the ADV7612, the following steps should be used :

- Set POWER_DOWN bit (98 0C 62)
- In case of POWER_DOWN mode 0 – power down CEC (80 2A 3E)
- In case of POWER_DOWN mode 1 – power up CEC (80 2A 3F)

When returning from low power mode, to correctly power up the ADV7612, the following steps should be used :

- Put the RX section into power down mode (98 0C 42)
- If CEC should be powered up (80 2A 3F)
- If CEC should be powered down (80 2A 3E)

Note: In power down modes additional power-savings can be achieved using following writes :

- Ring Oscillator powered down (68 48 01)
- DDC Pads off (68 73 03)

2.2.4   Packet Detection

The ADV7612 does not generate an interrupt when a source stops sending the following infoframes :

- Audio infoframe
- Source Prod infoframe
- MPEG Source infoframe
- Vendor Specific infoframe
- ACP infoframe
- ISRC1 infoframe
- ISRC2 infoframe
- Gamut infoframe

To detect when a source has stopped sending an infoframe :

- Clear infoframe interrupt RAW bit
- If RAW bit does not get set during max allowed packet repeat time, the source has stopped sending the infoframe

For example, 3D content is indicated using the Vendor Specific (VS) infoframe. It has been observed that some 3D sources stop sending the VS infoframe should their output be switched from 3D to 2D. For this reason, the application must detect when the VS infoframe has stopped being received.

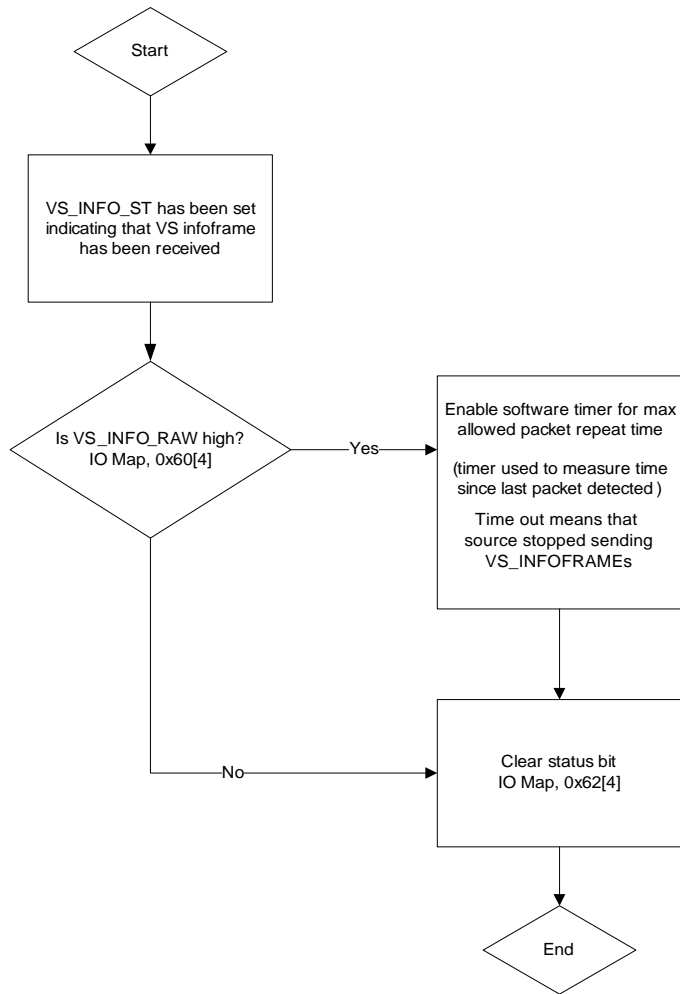A suggested ISR Routine that could be employed is as follows :
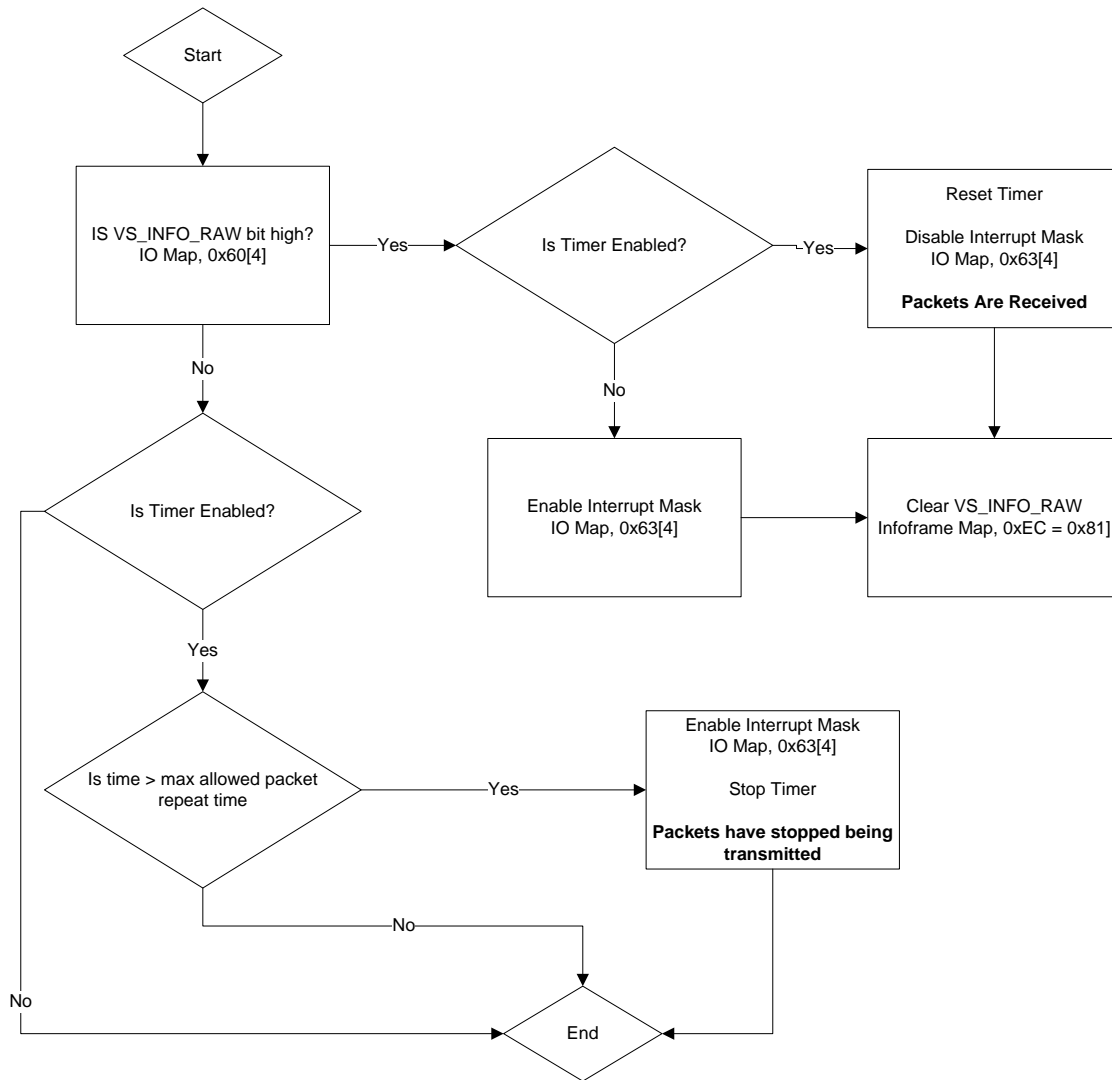

Figure 1. ISR Routine

Figure 2. Infoframe Task

2.2.5   Equalizer Settings

During HDMI compliance tests maximum resolution is taken into consideration. Therefore there are two sets of settings depending on maximum video resolution device can support. There is no need to dynamically change settings depending on currently received video standard. These settings should be chosen basing only on maximum supported resolution by device.

Device can support video modes above 480p/576p:

HDMI Map	
68 8D 04	LFG Port A
68 8E 1E	HFG Port A
68 90 04	LFG Port B
68 91 1E	HFG Port B

Device can support video modes only up to 480p/576p:

HDMI Map	
68 8D 04	68 8D 04 ; LFG Port A
68 8E 35	HFG Port A
68 90 04	LFG Port B
68 91 35	HFG Port B

2.2.6   Low Frequency Formats

To process the low frame rate video formats such as 720p24, 720p25, 720p30, 1080p23, 1080p24, 1080p30 and similar the NEW_VS_PARAM bit should be set. Refer to Figure 3.
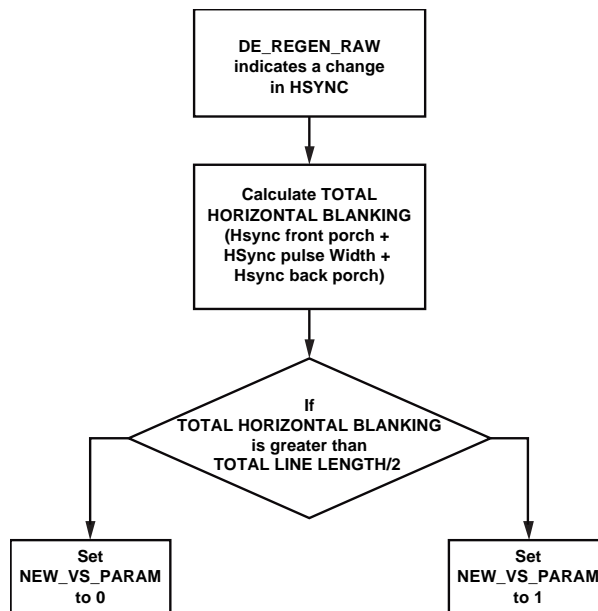

Figure 3. Low frame rate algorithm

NEW_VS_PARAM, HDMI, Address 0x4C[2]

Enables a new version of vertical parameter extraction. For evaluation purposes. That is the version in the background port measurement blocks.

Function

NEW_VS_PARAM	Description
0	NEW_VS_PARAM disabled
1	NEW_VS_PARAM enabled

NOTES

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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