CSE205 Spring 2021 Homework 4

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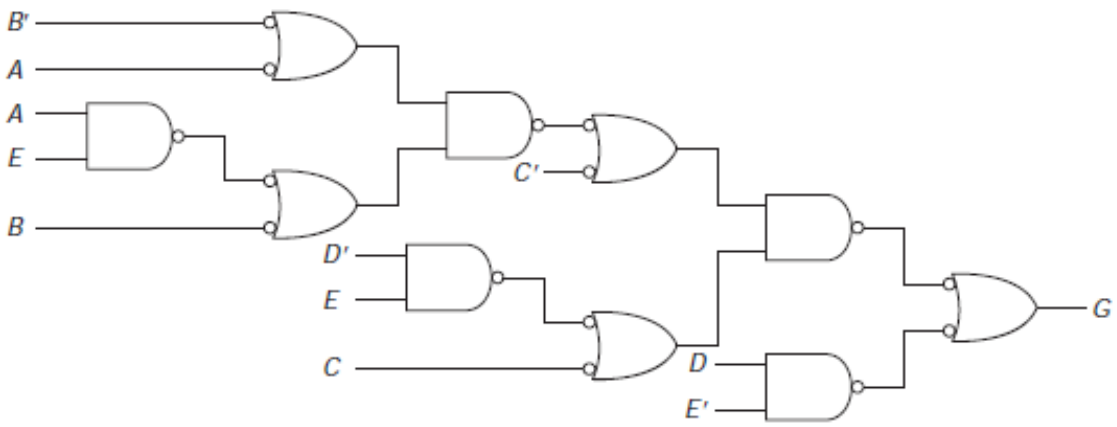
Problem 1

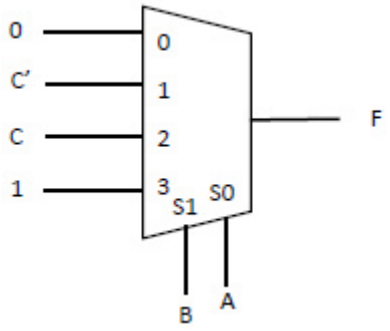
Compute the maximum delay, assume every gate (gate includes the attached negation bubbles) has a delay of Δ. Assume only uncomplemented inputs are available and an additional gate must be added to complement any input marked X'.



Solution: Since we can see that inputs A and E will have to go through 6 logic gates and we assumed every gate has a delay of Δ, the maximum delay is 6Δ.

Problem 2

Create the truth table that belongs to the following multiplexer implementing function F(A, B, C).



Solution:

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Problem 3

Given the following functions,

$$F(A, B, C) = \sum m(1, 4, 5, 7)$$

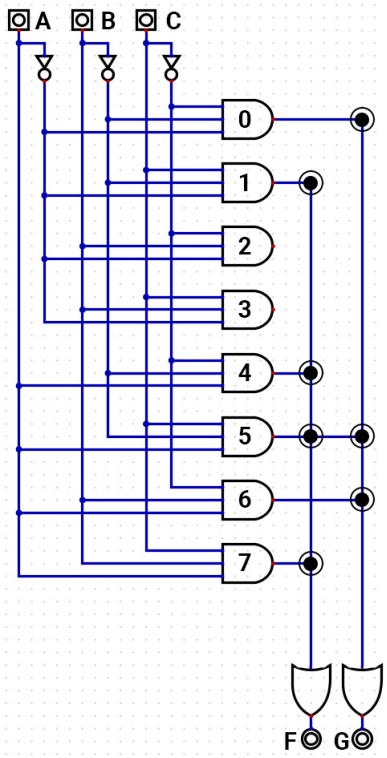
$$G(A, B, C) = \Pi M(1, 2, 3, 4, 7)$$

a. Implement both functions using a PROM chip (draw full grid)

Solution:

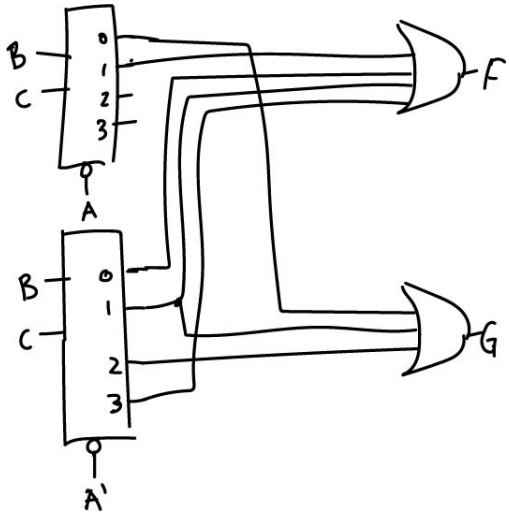
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

A	B	C	G
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



b. Implement both function using as many 2:4 decoders chips (with a single active lowenable) and any other logic gates needed

Solution:



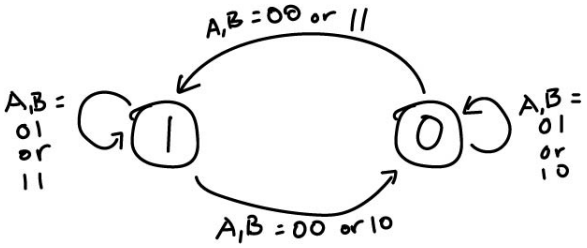
Problem 4

We have a new type of flip flop with inputs A and B. If A = 0, then Q^+ = B' + Q If A = 1, then Q^+ = (AB)'.

a. Show the state diagram for this flip flop.

Solution:

A	Q	Q^+	B
	0	0	1
	0	1	0
0	1	0	0
	1	1	1
	0	0	0
	0	1	1
1	1	0	0
	1	1	1



b. Write a single equation for Q+ in terms of A, B and Q.

Solution:

A \ BQ	00	01	11	10
0	1	0	1	0
1	0	1	1	0

$\boxed{Q^+ = Q(A+B)+A'B'Q'}$

Problem 5

Answer the following short answer questions:

a. Why is a NOT inverter logic gate faster than an open-collector buffer gate?

Solution: An open-collector buffer gate consists of two transitors. This, by default, would mean that the NOT inverter logic gate is faster than an open-collector buffer gate since a NOT inverter gate only contains one transitor.

b. What happens when a tri-state buffer has an enable input equal to 0?

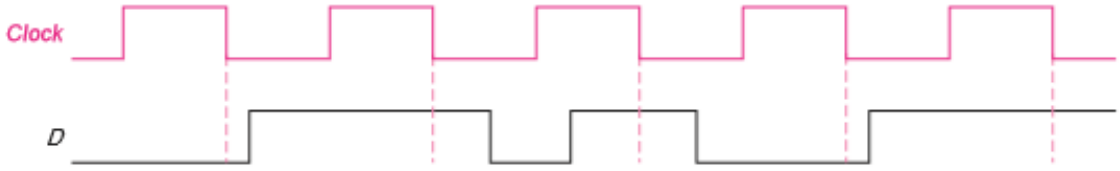
Solution: When the tri-state buffer has an enable input equal to 0, the buffer behaves as an open circuit – the output is no longer connect to anything. This is called the High-Impedance state (Hi-Z).

c. A latch and a flip flop differ in what way?

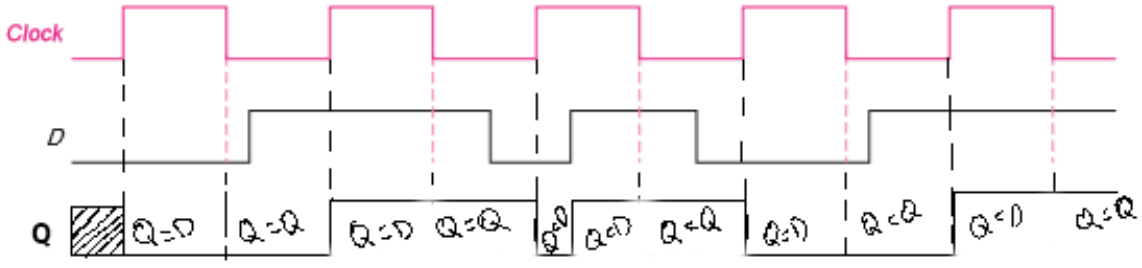
Solution: Latches are asynchronous – the outputs changes soon after the input changes – however, most appliances and eletronics operate with an internal clock signal. And so the flip-flop is a synchronout version of the latch meaning it incorporates a clock signal so that the outputs changes simultaneously according to the clock.

Problem 6

For the input D show below, show the D-latch output (Q) assuming the latch is activated when the enable signal is high.



Solution:



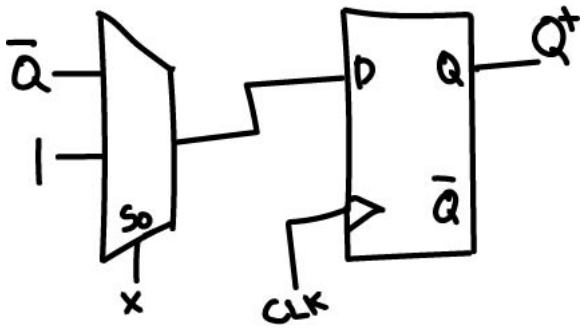
Problem 7

Create the schematic for a new flip flop with the behavior defined by the function below. Use a single D flip flop (positive edge triggered), a single 2:1 multiplexer, and any complemented or uncomplemented variables or additional logic gates needed.

$$Q^+(x, y, Q) = (Q' + x) + (y'Q')$$

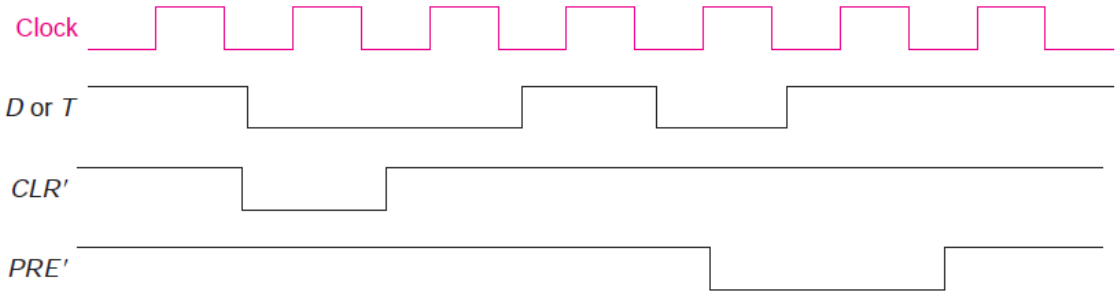
Solution:

x	y	Q	Q^+
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



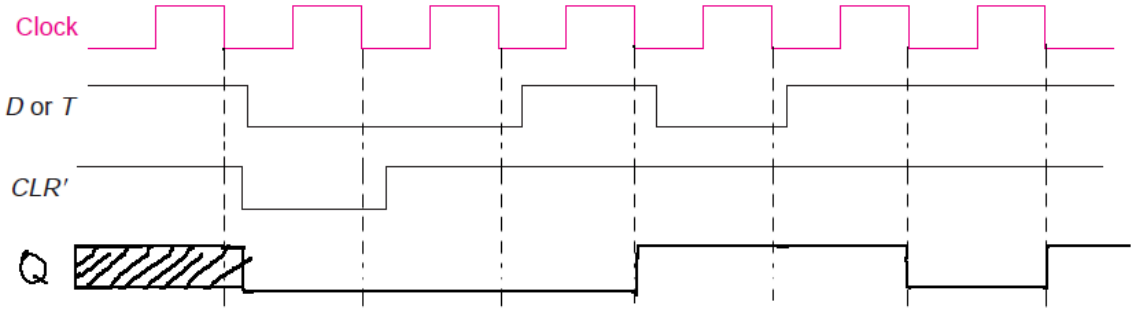
Problem 8

For the input shown below, show the flip flop outputs assuming a negative edge trigger.



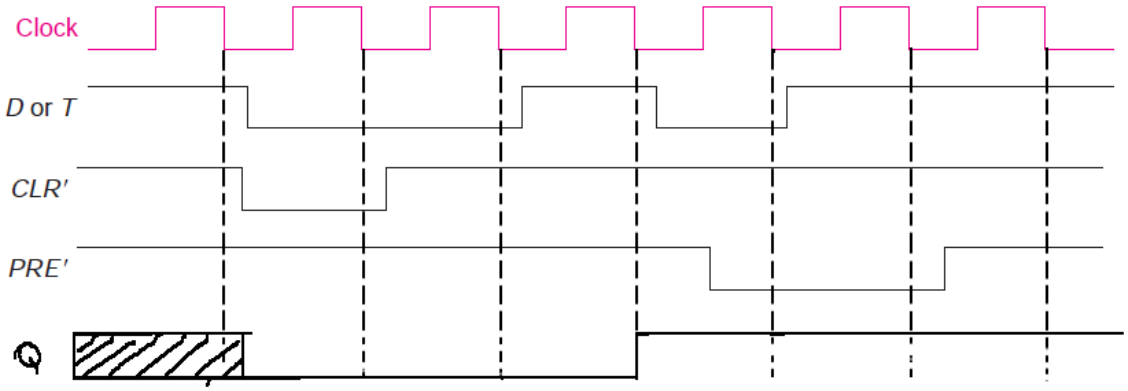
a. Assume that the flip flop is a T flip flop with only an active low clear (ignore the PRE' input).

Solution:



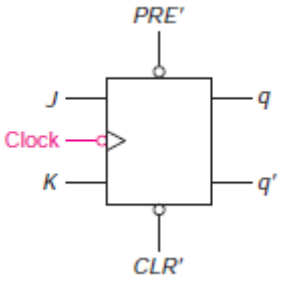
b. Assume that the flip flop is a D flip flop with both an active low clear and active low preset.

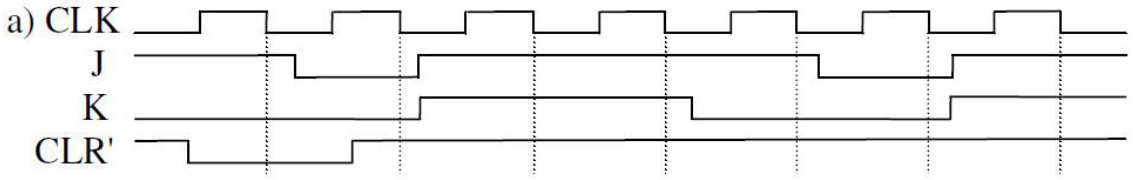
Solution:



Problem 9

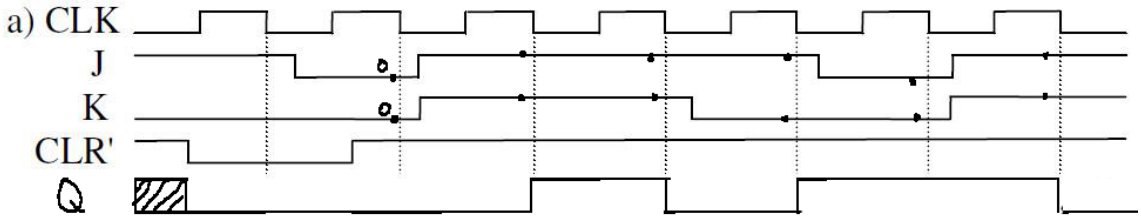
For the following JK flip flop, complete each timing diagram. First, assume the CLR' and PRE' are inactive (1). Then use the values shown.

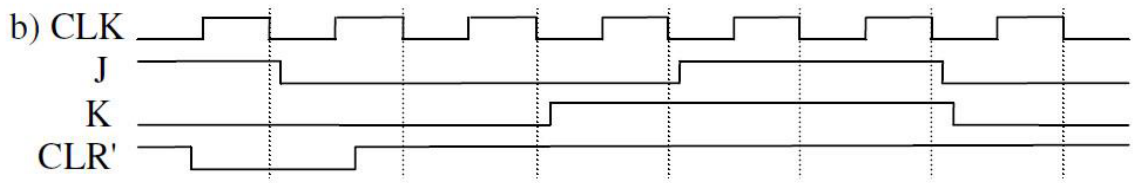




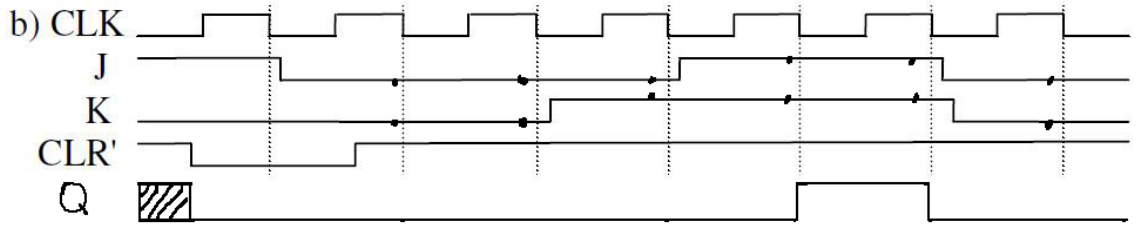
Solution:

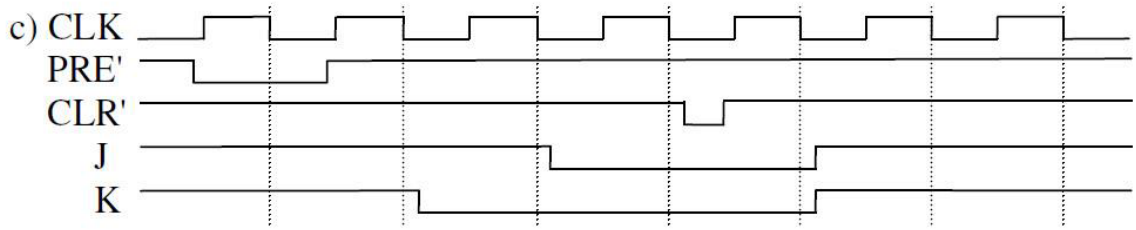
J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$



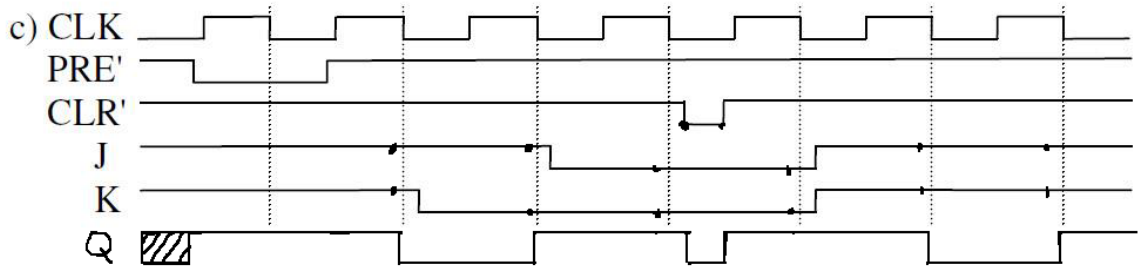


Solution:



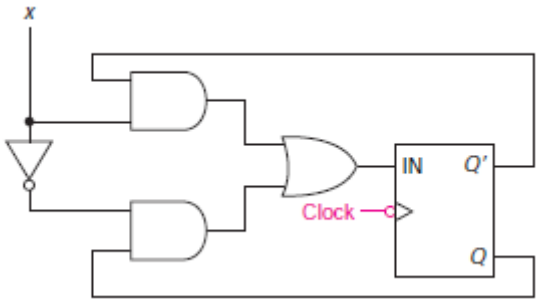


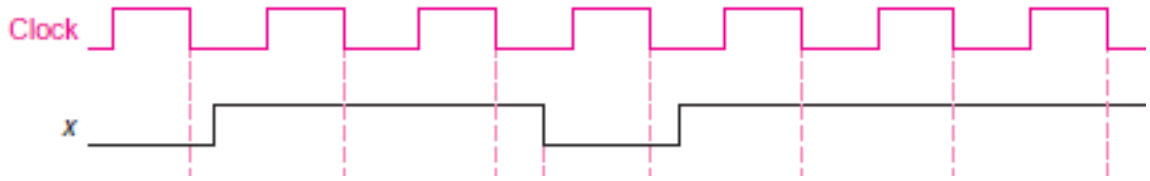
Solution:



Problem 10

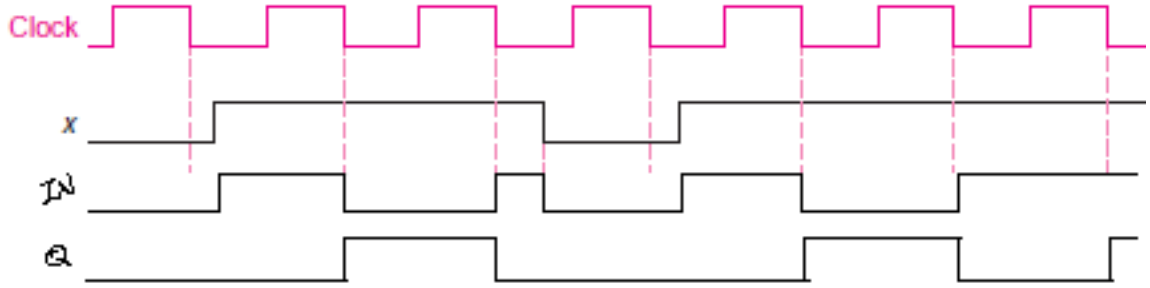
For the following circuit, complete the timing diagram assuming negative edge triggering. Include a timing graph for both IN and Q in relation to x. Assume the flip flop is a D flip flop. Assume the flip flop starts at 0.





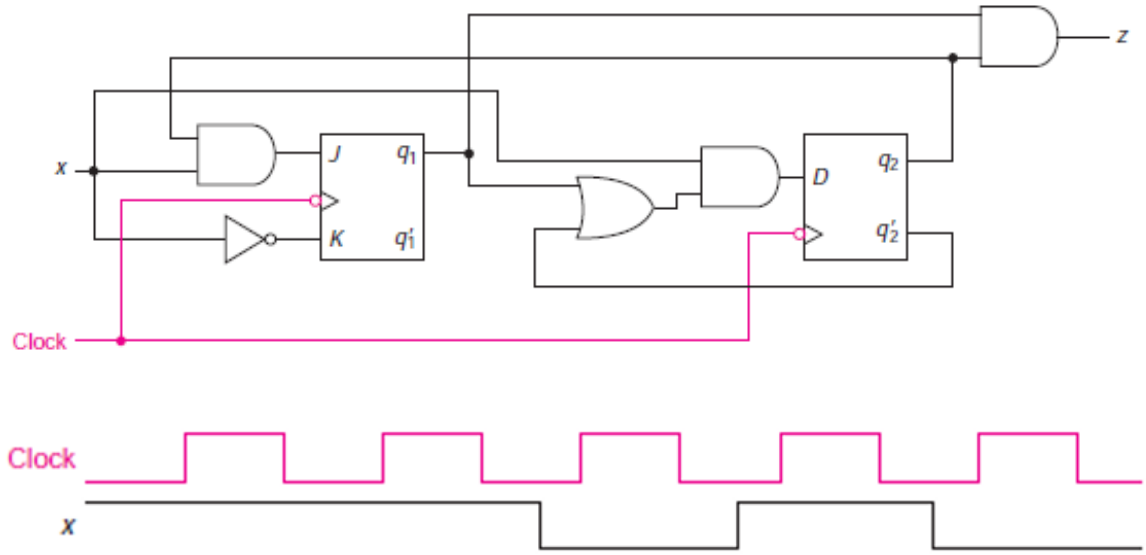
Solution:

IN equation: $\overline{Q}x+Q\overline{x}$

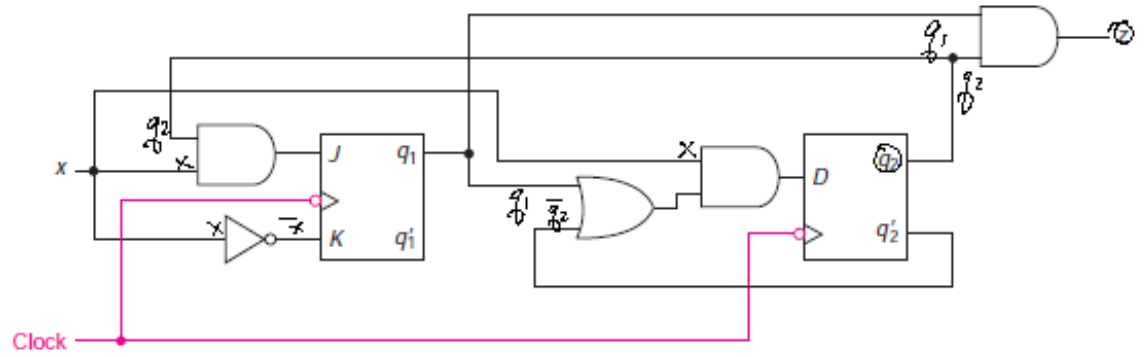


Problem 11

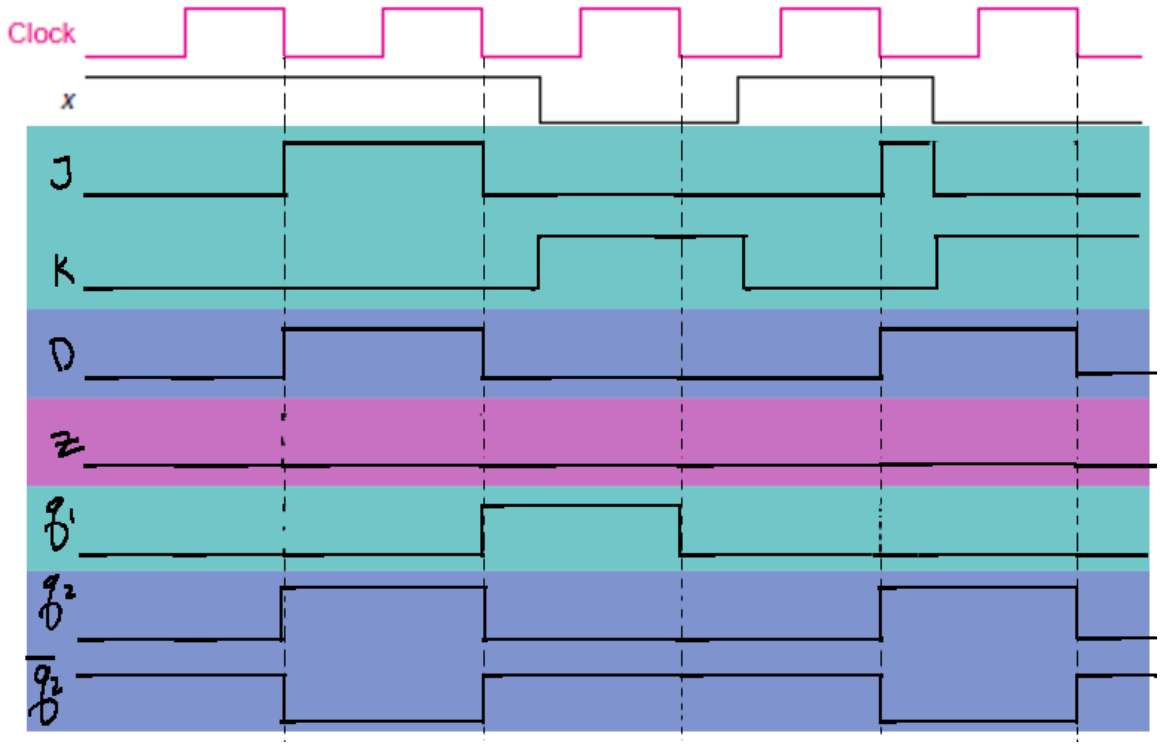
For the following circuit, complete the timing diagram for the state of each flip flop and the output, where shown. All flip flops are negative-edge triggered. Assume each flip flop starts at 0.



Solution:



$J = xq_2$ $K = \overline{x}$ $D = x(q_1 + \overline{q}_2)$ $Z = q_1 q_2$


Clock
x
J
K
D
Z
q_1
q_2
$\overline{q_2}$