SHULI HUANG

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ABOUT ME

Seeking Full-time position in process engineering

SKILLS

Software Skills
Matlab
AutoCAD
Multisim
COMSOL
Photoshop
PSpice
HSpice
Cadence Virtuoso
Eagle CAD
Visual Studio

Programming Languages
C
Matlab
Python
C#
VHDL
Verilog

Technical Skills
Thin Film
Etching
CVD
PVD
Characterization
Design of Experiments

LANGUAGE

Fluent English
Native Chinese

EDUCATION

UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

Master of Engineering in Mechanical Engineering GPA : 3.42/4.0 May 2017
Bachelor of Science in Electrical Engineering GPA : 3.19/4.0 May 2015

Area of Study:

IC Device Theory & Fabrication,Material Processing,Digital/Analog IC Design,Memory IC Structure,MEMS Device,Microelectronics and Photonics

WORK EXPERIENCE

SMIC (SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORPORATION), TIANJIN CHINA May 2016 - Aug 2016

Process Integration Engineer Intern

- Maintained inline manufacture of CMOS image sensor and EEPROM by improving wafer yield
- Designed and analyzed WAT tests to help customer companies transfer lab recipes to mass production
- Performed IC layout design rule check and fabrication recipe setup for a new EEPROM product

MICROSOFT, BEIJING CHINA June 2015 - July 2015

IT Asset Manager Intern

- Organized remote IP proxies and virtual machine usage allocation for employees
- Collaborated with a colleague in designing a user-friendly IT asset management website using C# in Microsoft Visual Studio

RESEARCH EXPERIENCE

MEMS FABRICATION AND CHARACTERIZATION Aug 2015 - Present

Personal Instructor: Sungwoo Nam

- Characterize the optical and electrical properties of monolayer graphene and MoS2 and their wrinkled structures
- Develop novel structures of crumpled monolayer CVD graphene to make highly sensitive conformal strain sensor
- Integrate crumpled graphene sensor arrays onto PCB for accuracy and sensitivity analysis

PN JUNCTION-ASSISTED MEMBRANE DESALINATION May 2014 - May 2015

Personal Instructor: Gang Logan Liu

- Discovered more efficient device design by simulating ion rejection effects of PN junction nanochannels using COMSOL
- Fabricated the nanoporous PN junction membrane using standard wafer fabrication technology in cleanroom

PROJECTS

WAFER FABRICATION TECHNOLOGY Jan 2016 - May 2016

- Studied major innovations for technology scaling, such as high-k dielectric, metal gate, drain engineering and strained Si
- Investigated the advantages and disadvantages of FinFET and FDSOI designs for 28nm and below technology nodes

THERMOELECTRIC HEATING SHOES Jan 2015 - May 2016

- Spearheaded a team of 3 in devising a heating shoe powered by thermoelectric energy harvesting circuit
- Interfaced sensors and signal amplifiers with a microcontroller to ensure temperature control accuracy
- Constructed the PCB layout of various analog parts to improve energy harvesting efficiency and reduce power consumption

[7,4] HAMMING CODE ERROR DETECTION CIRCUIT DESIGN Aug 2014 - Dec 2014

- Led a team of 5 to design a data error detection circuit at 250nm node technology using Cadence circuit layout design tools
- Optimized logic design and circuit layout by analyzing circuit delay time and power consumption in HSpice

LOGIC COMPONENTS FABRICATION AND CHARACTERIZATION Aug 2014 - Dec 2014

- Performed the whole fabrication process of basic logic gates using 180nm MOSFET technology on a 4 inch wafer
- Characterized the critical currents and capacitances on a probing station

ACTIVITIES

RACE TO ZERO (R20) 2016 NATIONAL COMPETITION, PHOTOVOLTAICS (PV) Aug 2015 - Apr 2016

Subteam Leader

- Represented UIUC R20 team of 28 people in the DOE national competition R20-2016 final presentation and earned 2nd Place
- Coordinated with HVAC subteam to implement geothermal heat pump for indoor cooling/heating and hot water production
- Achieved net zero energy rating for the target residential building by designing and optimizing PV systems