John Webster

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Summary

Experienced VLSI/ASIC designer looking for new opportunities and challenges

Core skills

Physical Design.

Antenna (NAC), LVS, DRC, netlisting. Floorplanning, Synthesis, Routing, Static timing analysis and timing closure in ASIC environment. Design rules and the underlying process technology. Layer densities, Physical Design for Debug (fiducials, fib cells, spare cells). Fill mechanisms, tech files setup. Recent tapeouts at 22,14 and 10nm process nodes. Low power design. Formal Verification. Clock tree synthesis.

Power grid design and Reliability

Power grid design and analysis, area vs IR drop, Power gating, EM, on die regulation, bump analysis

Tools and programming

Synopsys ICC, ICV (and Hercules), Synthesis, DC, PrimeTime, Apache Redhawk, verilog, VHDL
Perl, TCL, C, lisp
Unix, MS word, Excel, Powerpoint. JMP, batch compute

Management

Managed small teams (to 5 people). Mentoring of junior engineers.
Provided technical training and taught Intel core values classes
Source control, cross site working

Design

Experience in ASIC design flow from RTL to GDS/OASIS
Micro-architecture and RTL design of microprocessors
RTL verification
Debug and problem solving skills throughout ASIC design flow
Scripting for design flows and for problem solving.
Results focused ability to learn or develop new methodologies, tools and flows

Intel Corporation (Folsom, CA) September 1996 – July 2015. Senior component design engineer

2007 - 2015 Integrated graphics (VPG) – Technology team, part of physical design

- VPG supplies integrated graphics for Intel CPUs using ASIC methodologies. Physical design team responsible for hard macro generation, floor planning, synthesis, P&R, timing closure, layout closure and tapeout, SI prevention/fixing, power planning, CTS, PV, IR drop, EM analysis and formal verification
- First tapeouts on 22nm (Haswell), 14nm (Broadwell),10nm (CanonLake). Methodologies re-used on “tock” products (Skylake, Kabylake)
- Design of metal route tracks for all graphics/ASIC products as part of Intel process definition team, reliability tradeoffs, density tradeoffs, library design tradeoffs (Intel award)
- Design of graphics power grid – re-used by other ASIC teams within Intel
- Design of power gate placement and connection scheme - analysis of area impact and Electromigration
- Floorplanning and integration of on die switching regulators
- Bump analysis for IR drop, reliability and routability
- CanonLake (10nm) specific tasks in addition to above
  - Physical verification and cleanup of block
  - runset modification to support error debug and temporarily remove false errors

Intel Corporation cont.

- CanonLake (10nm) specific tasks cont.
  - Antenna rule assistance and debug for whole physical verification team
  - metal density analysis and issue debug
  - work on an internal tool to analyze effect of process parameter changes on design using PrimeTime to extract timings and Internal version of spice for simulation

2005-2006 Integrated graphics (VPG) : SandyBridge (28nm) – first Intel CPU with integrated graphics

- layout design lead, tapeout of Integrated Graphics, owned display block tapeout
- Convergence of physical design and reliabililty flows between CPU team (custom approaches) and graphics (ASIC approach) – std cell library, runset, database, fill methodologies, layout database, reliability (EM)

1997-2005 (PCI chipsets physical design)

- Integrated South Bridge/North bridge product - owned floorplan
- Broadwater chip set (integrated graphics), Key interface between RTL2Gates and APR teams, physical synthesis environment development, power grid design. Rewrite of metal fill flows in hercules to meet production density needs
- Backend lead for Plumas chipset, first server chipset within PCI chipset division. Responsible for synthesis, static timing, timing closure, floorplanning. First PCI chipset use of PrimeTime. Backend lead for Camino production steppings. Ran all gates to gates formal verification
- RTL to gates lead for several test chips and validation chips, used with FPGA and Silicon environments. RTL design on some test chips. First use of physical synthesis within PCI chipsets

1996-1997 Pre-silicon validation of 440BX chip set – single die North Bridge for Intel CPU

- Definition of tests, integration of bus models, writing tests, execution and regressions, owned DRAM testing.

ARM Ltd (Cambridge, England) 1993 - 1996

- Definition and initial support of AMBA bus standard
- Design of ARM8 integer pipeline (VHDL)
- Support and testing of VHDL wrapper for ARM software model.

Inmos Ltd (Bristol, England) 1987 - 1991

- Design of Floating Point Unit for next generation microprocessor (transputer) - performance analysis, algorithm design, definition, hdl design and simulation, custom design and layout of add/subtract unit. Integration into integer pipeline. Formal verification. Synopsys DC used for control logic synthesis.
- Board testing and design completion

Education:

B.Eng Computer Systems Engineering (First class honors) 1984-1987
University of Bristol
Internship at Ferranti Computer Systems Ltd., Bracknell 1983-1986