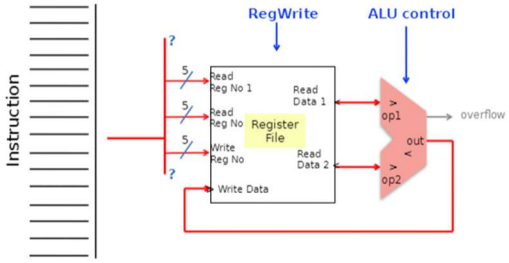
Types of Hazards:

Structural: two different instructions attempt to use the same resource at the same time; not too many in the mips pipeline

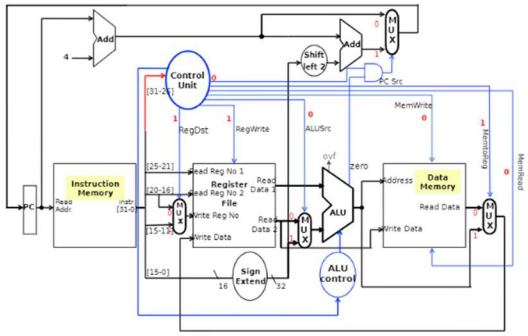
Data: Hazards a instruction attempts to use data before its ready; an instructions source operands are produced by a prior instructions, stillin the pipeline

Control Hazards: attempt to jump toa new addrerss before the brankch conditions has been evaluated.

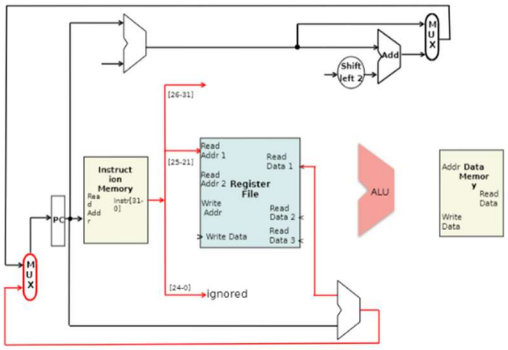
Datapath for OR Instruction



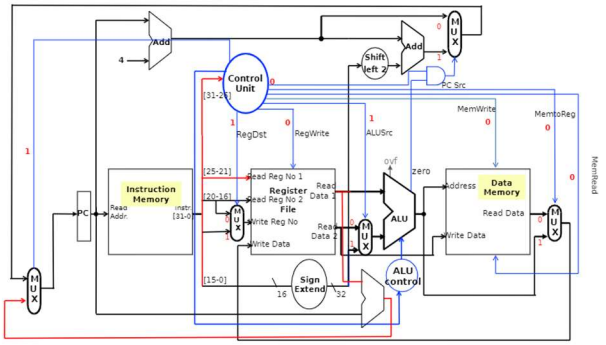
Control Signals For OR Instruction



Datapath for Long Jump



Control Signals for Long Jump



You have a 4-way set-associative cache with 8 words per block and 1024 entries. Determine the index, tag, block offset and word offset from the following 16-bit memory address. Assume addresses are word addresses and word size is 4 bytes. 0011001111111011

type of address: word address

word size: 4 bytes. words per block: 8. associativity: 4. sets: entries / associativity = 1024 / 4 = 256. * type of address is word address. So there is no word offset. * 8 words per block. Therefore, block offset log_2(8) = 3 bits. 011 * number of sets is 256. Therefore, index = log_2(256) = 8 bits. 01111111 * tag is rest of bits, 16 - 11 = 5 bits. 00110

You have a direct-mapped cache with 8 words per block and 512 entries. Determine the index, tag, block offset and word offset from the following 16-bit memory address. Assume addresses are byte addresses and word size is 4 bytes 0011001111111011

type of address: byte address. word size: 4 bytes . words per block: 8. associativity: direct-mapped. entries/sets: 512. * type of address is byte address and word size 4. Therefore, word offset is 2 bits. 11. * 8 words per block. Therefore, block offset log_2(8) = 3 bits. 110 * number of entries is 512. Therefore, index = log_2(512) = 9 bits. 110011111 * tag is rest of bits, 16 - 14 = 2 bits. 00

Size of Cache: -> [data type size][1][j]

Compulsory miss: Initially, all data and instructions for a program are in main memory. First access to any memory location is always a miss

Conflict: Conflict misses occur when Two memory locations M and M' map to the same cache block.M' evicts M before the second reference to M. No conflict miss if M is not reused

--- [pagetable] page corresponding to VPN: 5 fetched from Disk

--- [TLB] replacing LRU VPN: 5 with VPN: 5

MEM[5]: TLB Miss; Page Fault

Store – register – memory

Intel – Store register – memory

Machine instructions that have constants encoded in them are called - immediate instructions

If we have 4 bits in the address field of an instruction, how many different memory addresses can we express with those bits? 16 During the execution of this instruction, the following events are taking place in what order?

send signals to register file, compute memory address, read from memory, write to register file