

5

4

3

2

1

Revision	Date	Brief Description of Changes
Rev0.1	Oct 29, 2018	This is original issue of FPGA Computing Board

D

C

B

A

QDSGV

Drawing Title:

FPGA Computing Board

Page Title:

Revision History

Size

A3

Document Number

<Doc>

Rev

01

Date:

Wednesday, November 14, 2018

Sheet

1

of

77

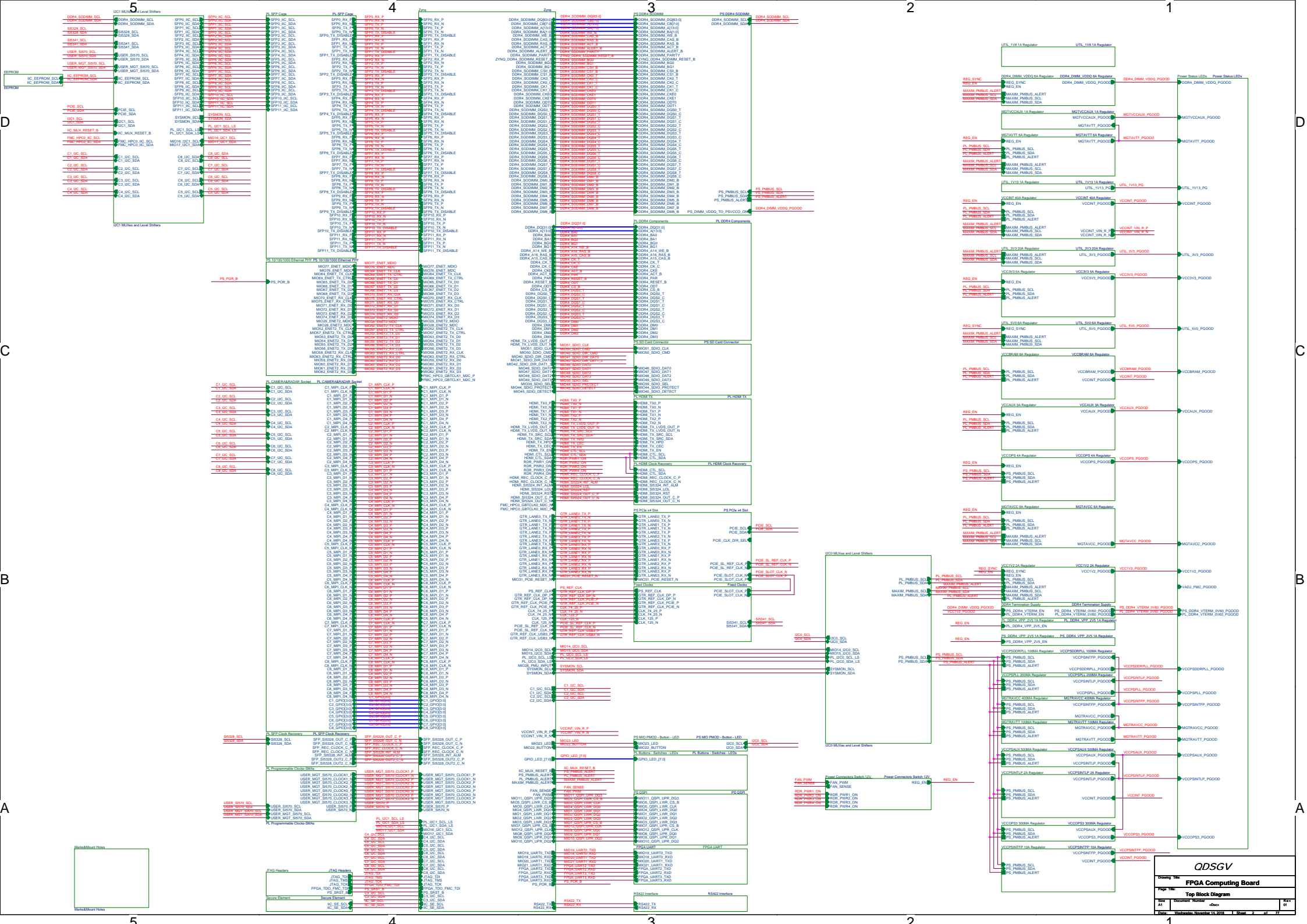
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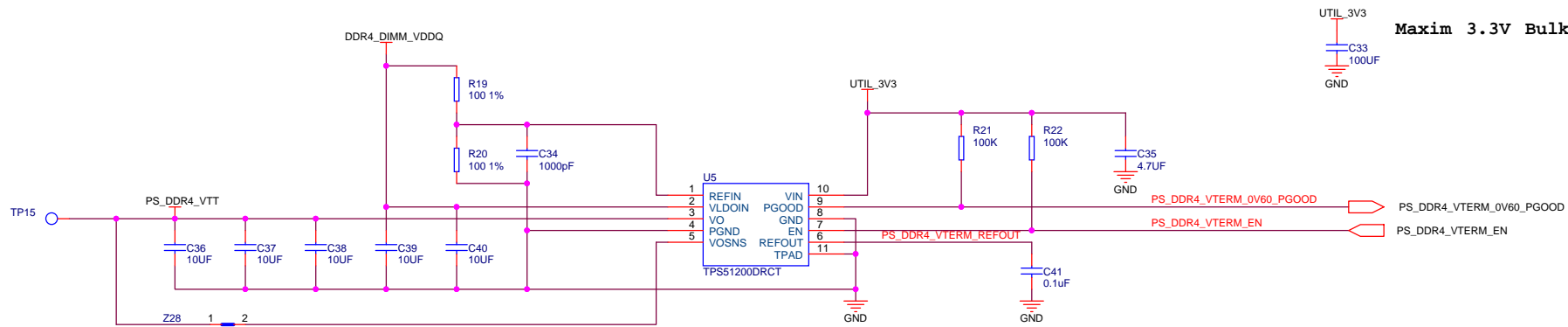
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3

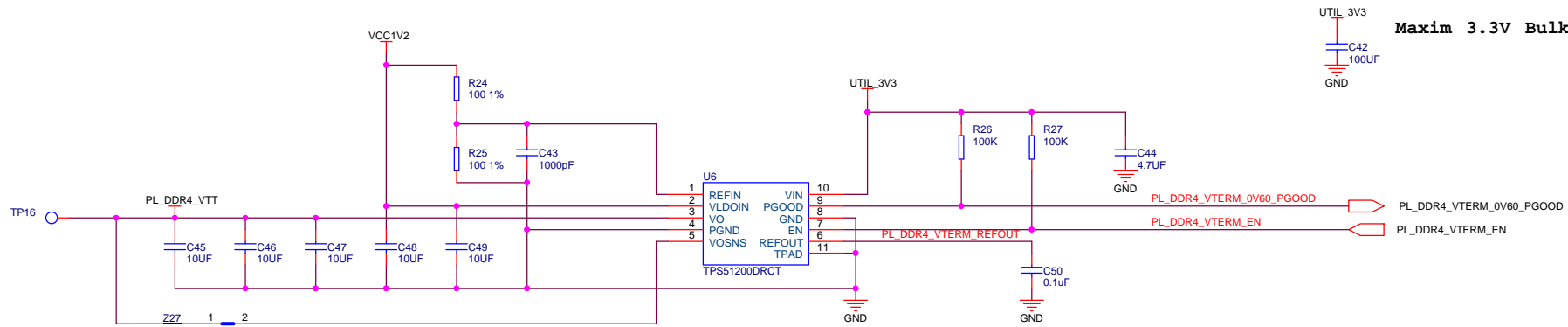
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1





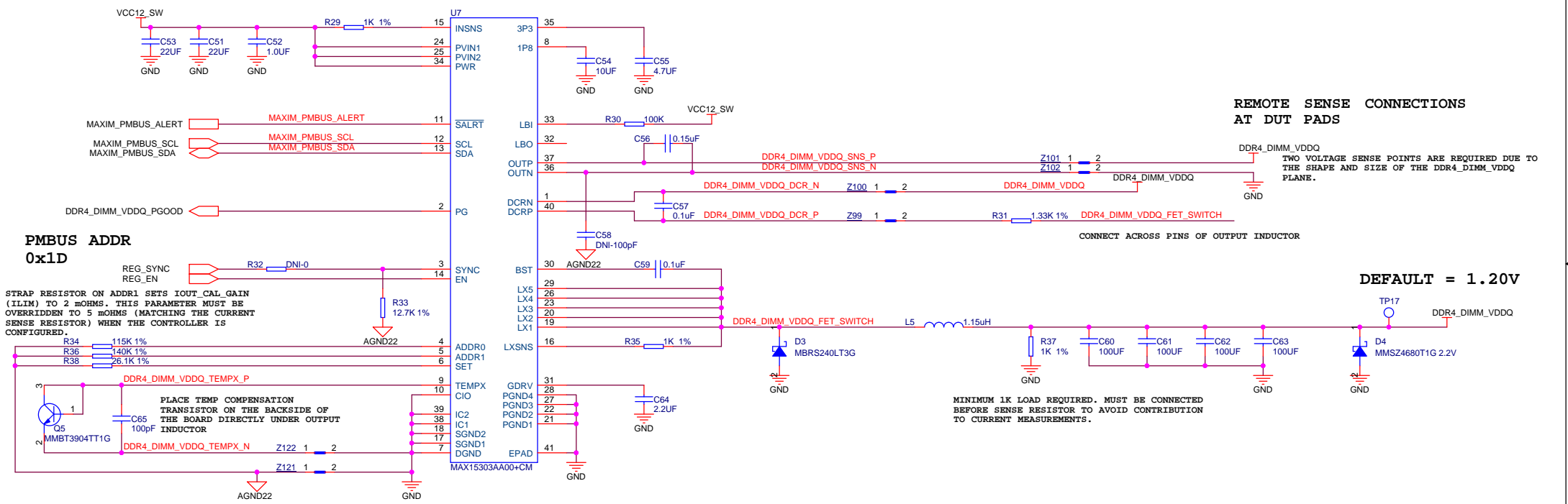
Maxim 3.3V Bulk (near PS VTT)



Maxim 3.3V Bulk (near PL VTT)

QDSGV

Drawing Title:			FPGA Computing Board		
Page Title:			DDR4 Termination Supply		
Size A3	Document Number <Doc>				Rev 01
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**PMBUS ADDR 0x1D**

STRAP RESISTOR ON ADDR1 SETS IOUT\_CAL\_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

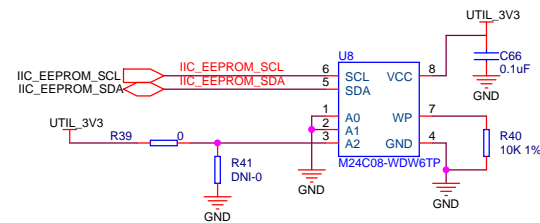
**REMOTE SENSE CONNECTIONS AT DUT PADS**

TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE DDR4\_DIMM\_VDDQ FLANE.

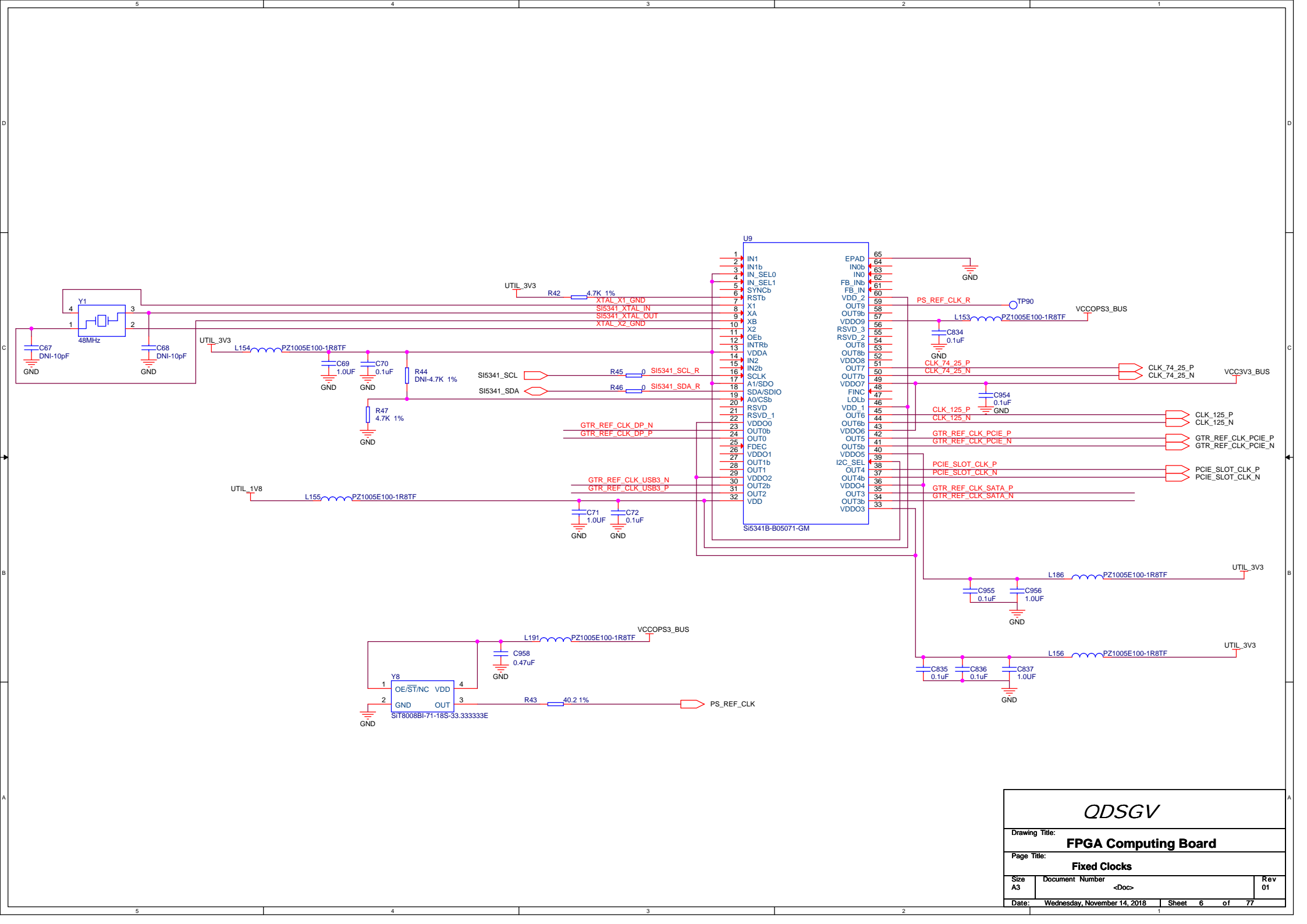
**DEFAULT = 1.20V**

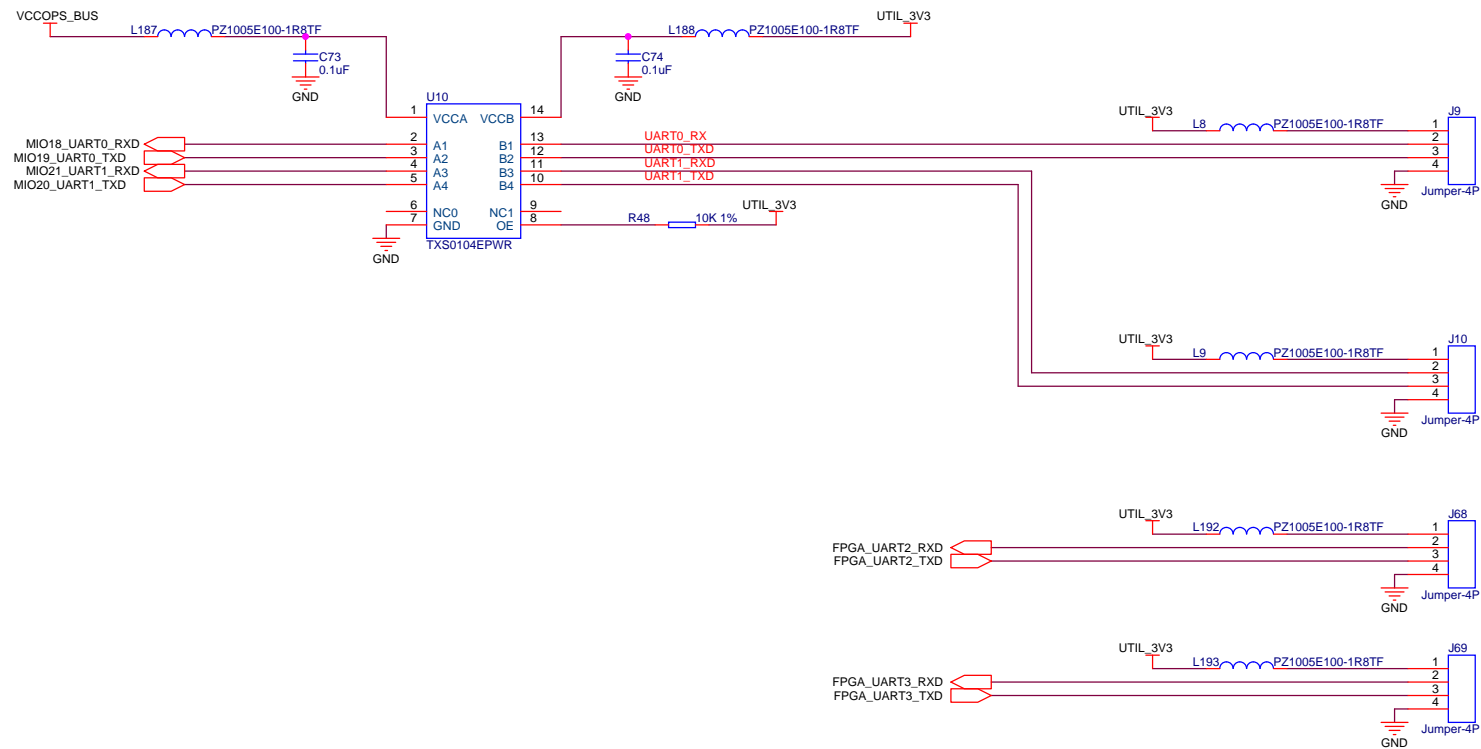
MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

QDSGV			
Drawing Title: <b>FPGA Computing Board</b>			
Page Title: <b>DDR4_DIMM_VDDQ 6A Regulator</b>			
Size A3	Document Number <Doc>		Rev 01
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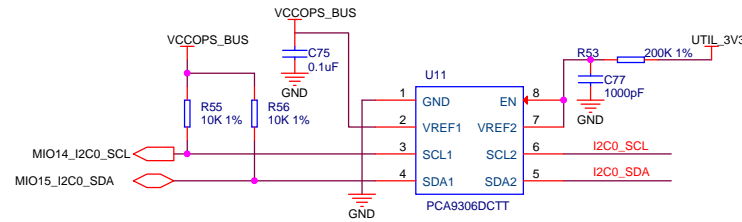
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Page Title: EEPROM			
Size A3	Document Number <Doc>		Rev 01
Date:	Wednesday, November 14, 2018	Sheet 5 of 77	



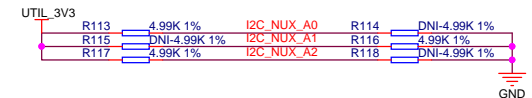
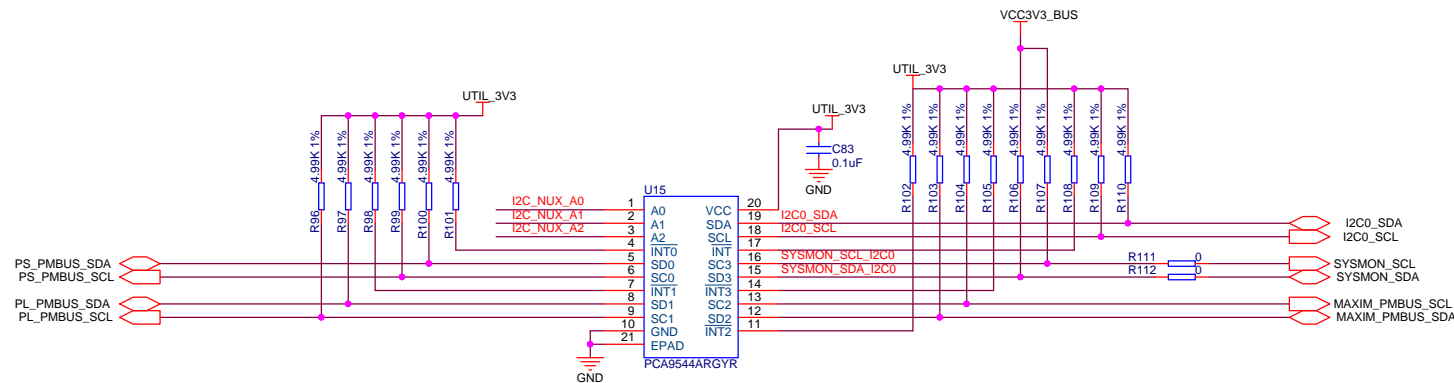
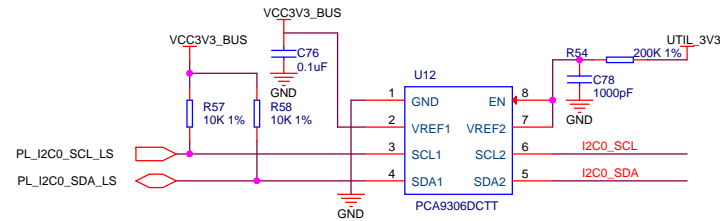


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Drawing Title:			
FPGA Computing Board			
Page Title:			
FPGA UART			
Size	Document Number	Rev	
A3	<Doc>	01	
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### PS I2C Level Shifter (I2C0)



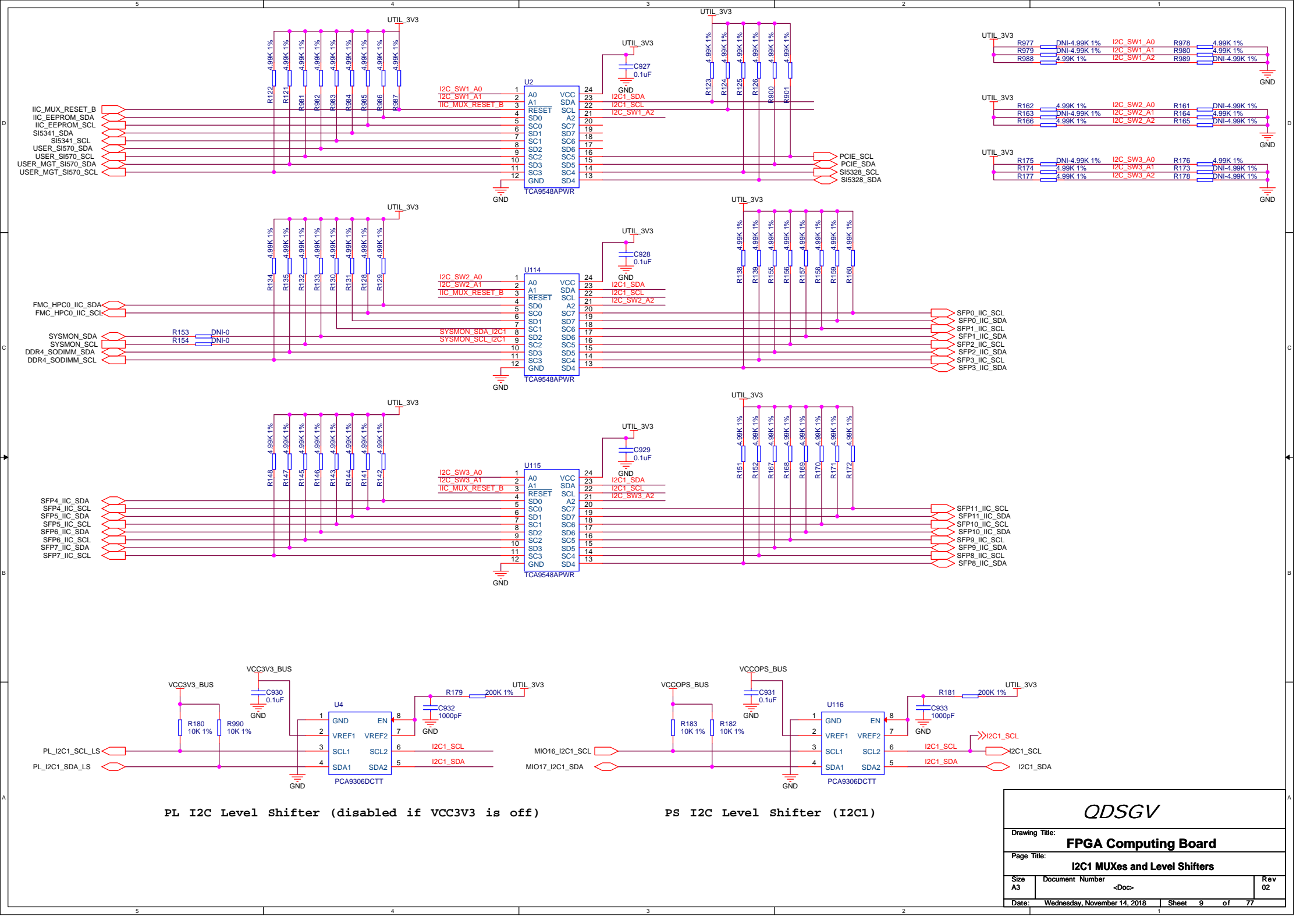
### PL I2C Level Shifter (disabled if VCC3V3 is off)



*QDSGV*

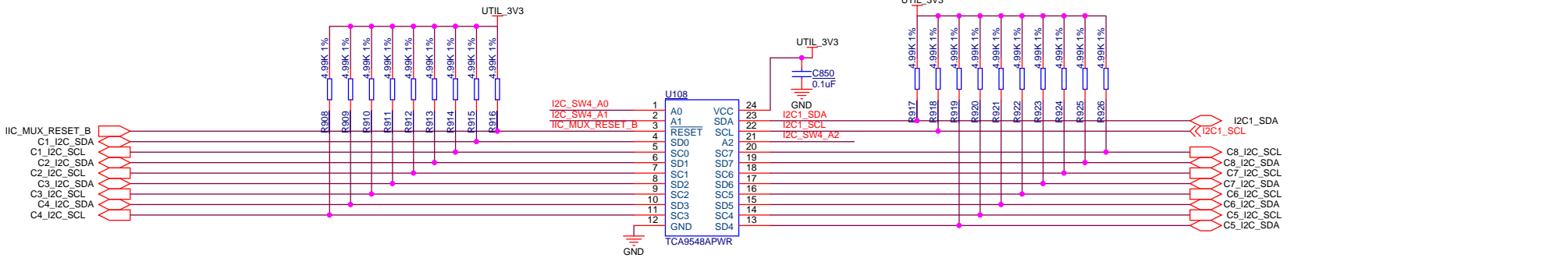
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FPGA Computing Board			
Page Title:			
I2C0 MUXes Expanders Level Shifters			
Size A3	Document Number	<Doc>	Rev 01
Date:	Wednesday, November 14, 2018	Sheet 8 of 77	

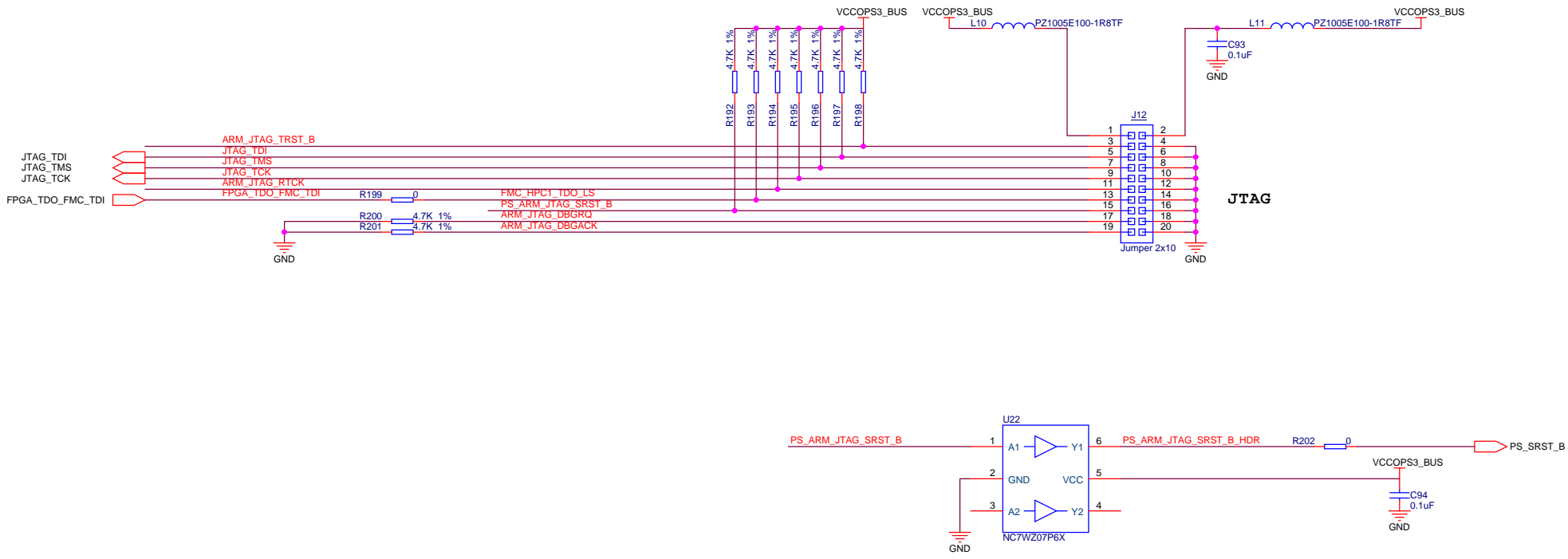


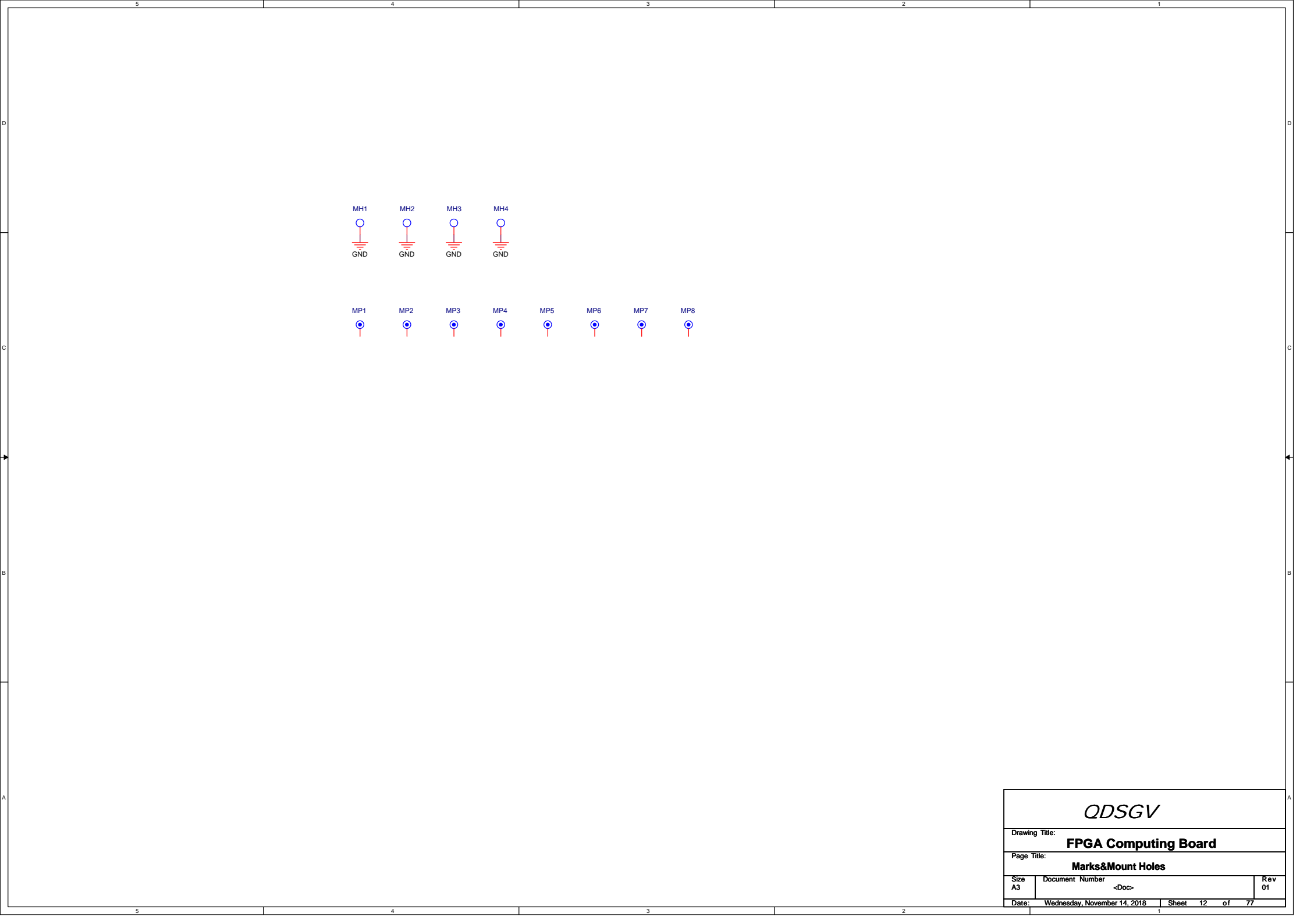


PL I2C Level Shifter (disabled if VCC3V3 is off)

PS I2C Level Shifter (I2C1)

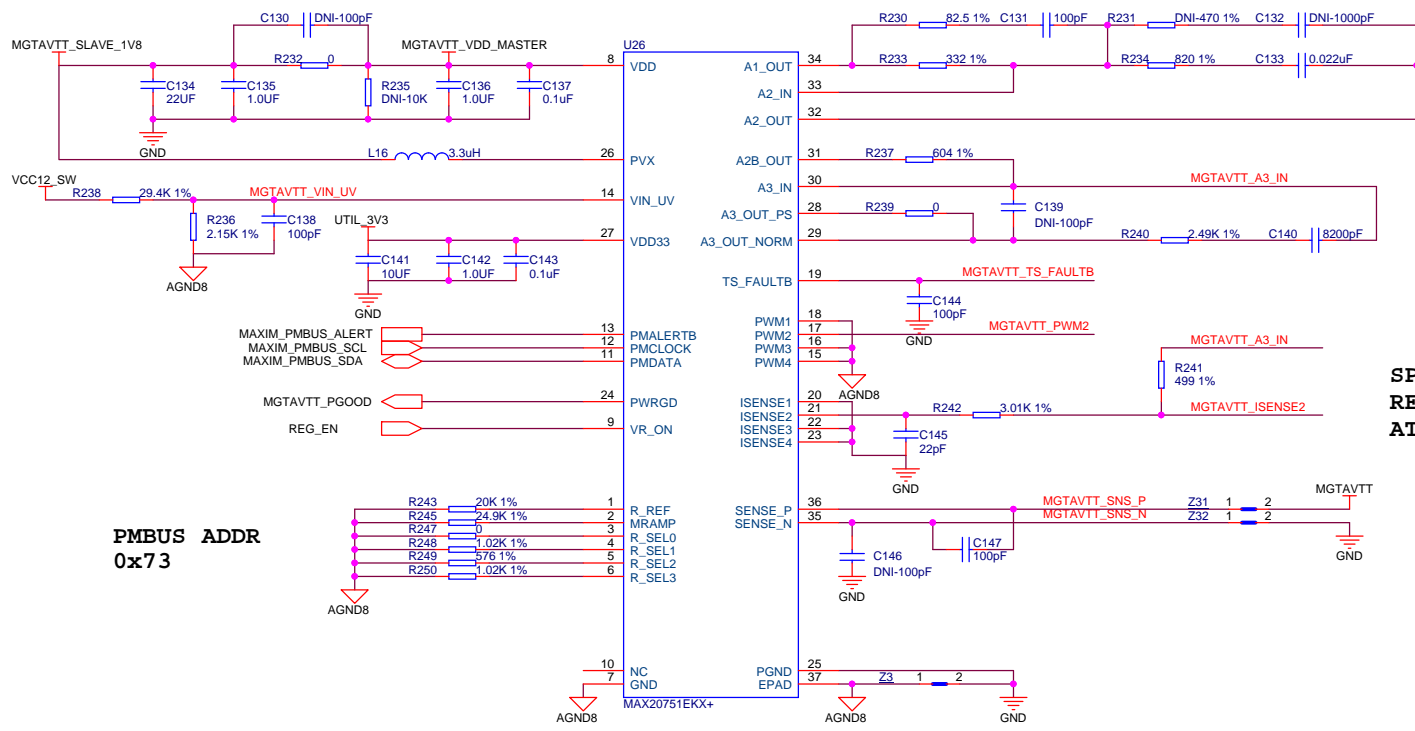




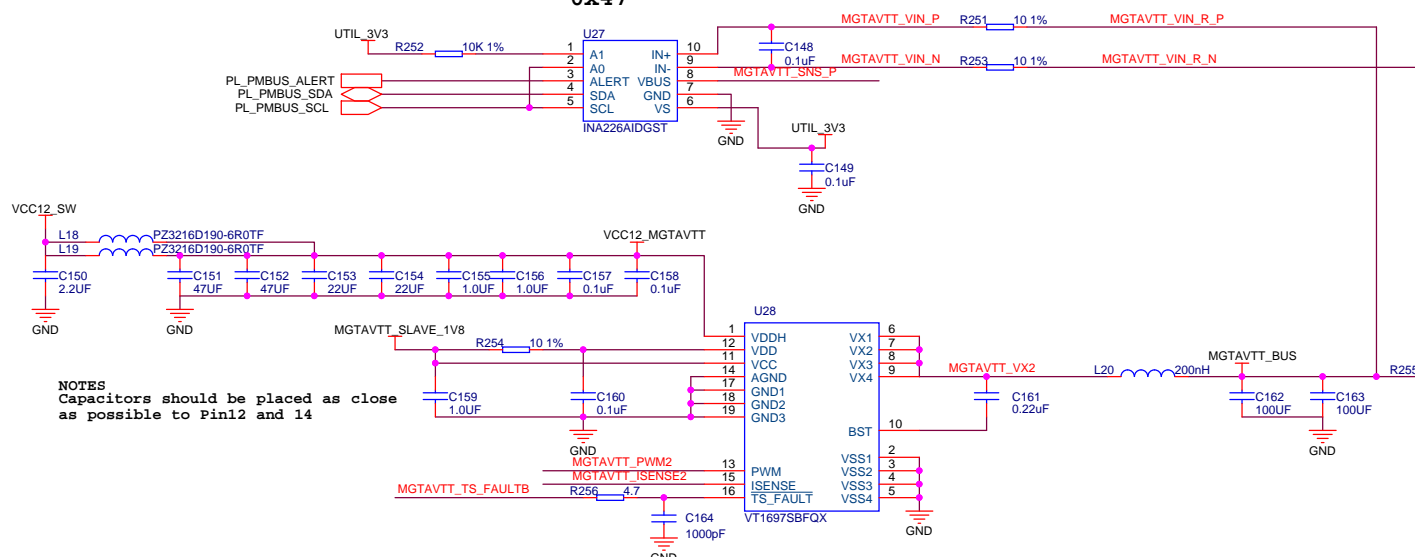


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Drawing Title: FPGA Computing Board			
Page Title: Marks&Mount Holes			
Size A3	Document Number <Doc>		Rev 01
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SPLIT POWER PLANE  
REMOTE SENSE CONNECTIONS  
AT DUT PADS

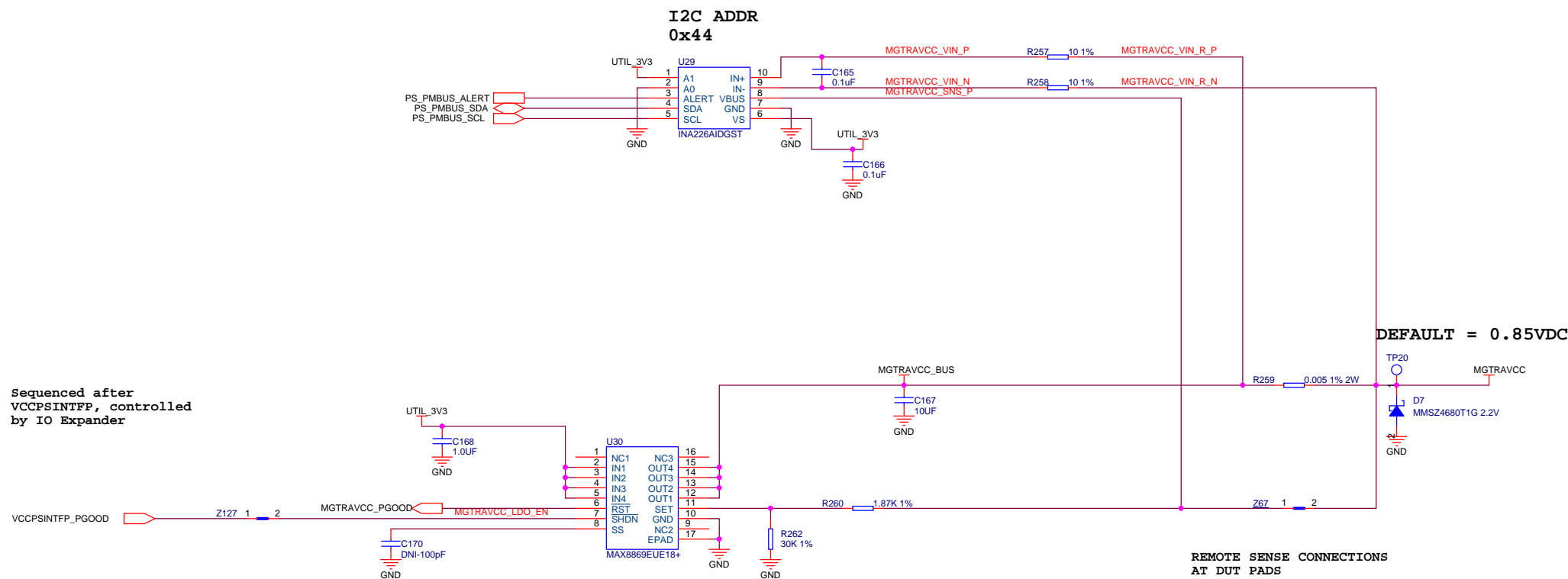


DEFAULT=1.20VDC

NOTES  
Capacitors should be placed as close  
as possible to Pin12 and 14

QDSGV			
Drawing Title: FPGA Computing Board			
Page Title: MGTAVTT 6A Regulator			
Size A3	Document Number	<Doc>	Rev 02
Date:	Wednesday, November 14, 2018	Sheet 14	of 77

Sequenced after  
VCCPSINTFP, controlled  
by IO Expander

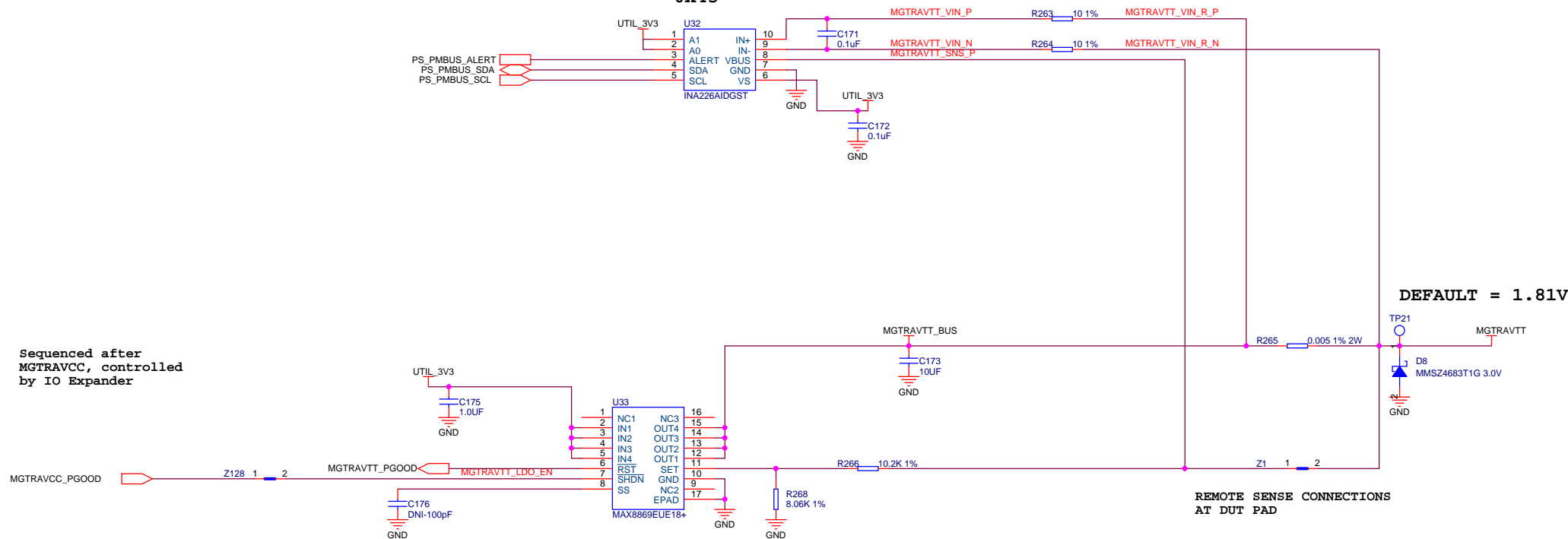


*QDSGV*

Drawing Title:			FPGA Computing Board		
Page Title:			MGTRAVCC 400mA Regulator		
Size A3	Document Number <Doc>				Rev 01
Date:	Wednesday, November 14, 2018	Sheet	15	of	77

Sequenced after  
MGTRAVCC, controlled  
by IO Expander

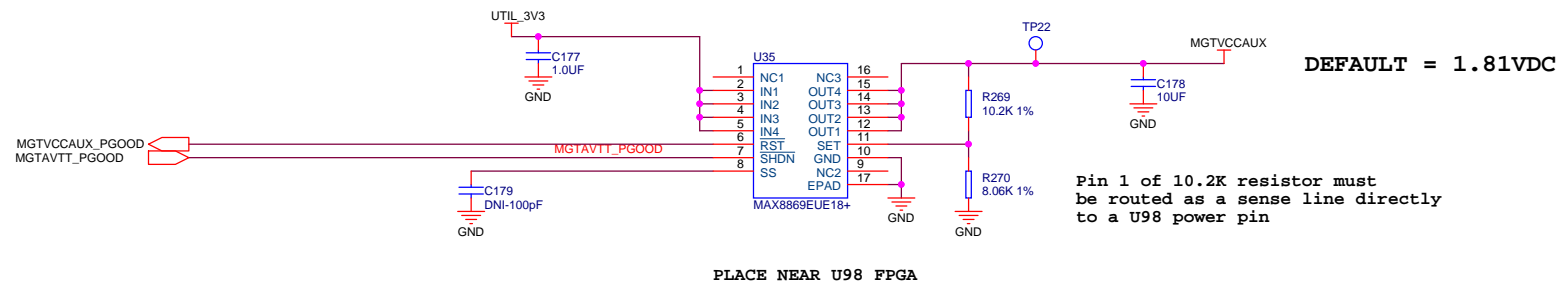
I2C ADDR  
0x45



QDSGV

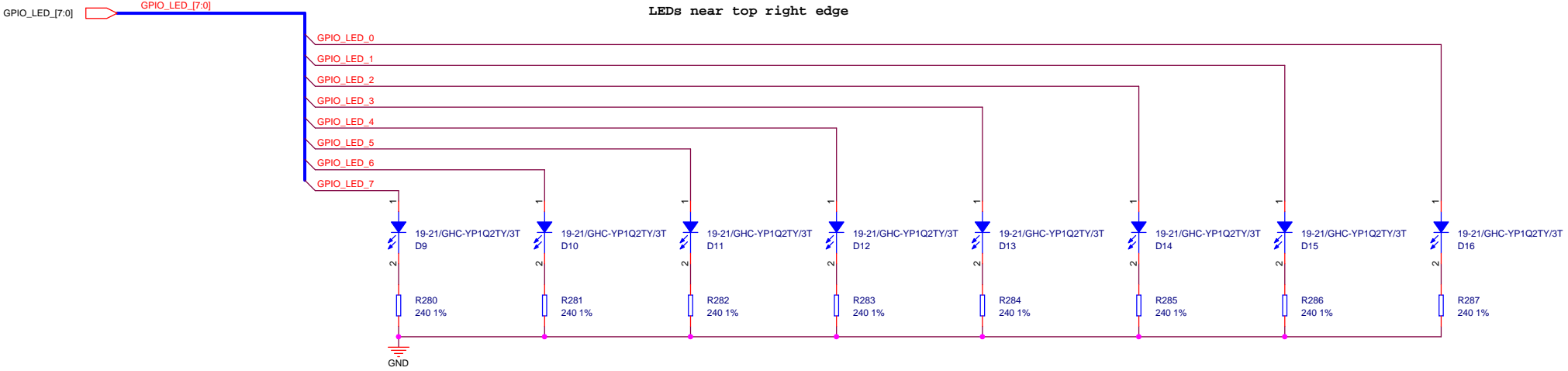
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Page Title:			MGTRAVTT 100mA Regulator		
Size A3	Document Number <Doc>				Rev 01
Date:	Wednesday, November 14, 2018	Sheet	16	of	77

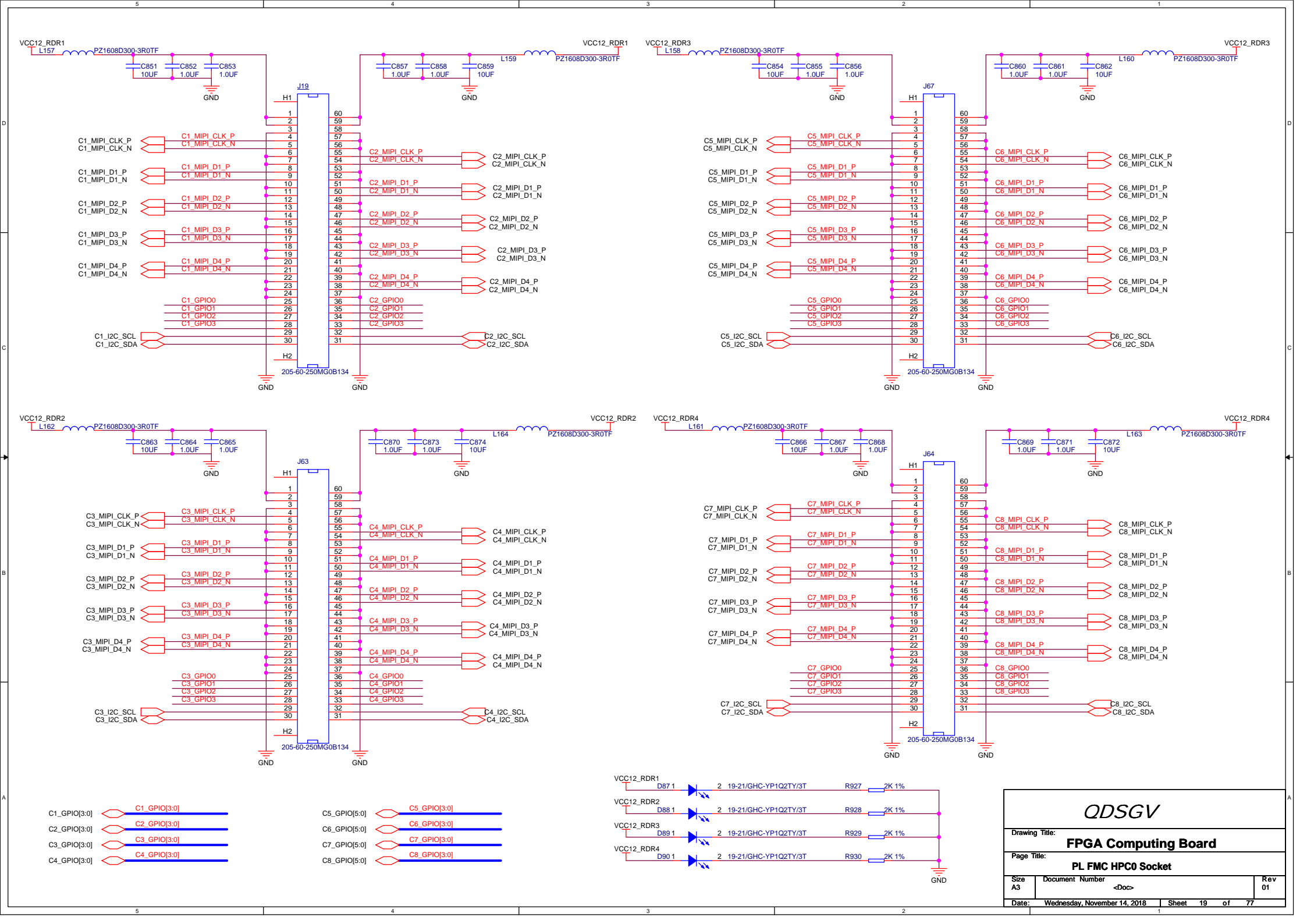


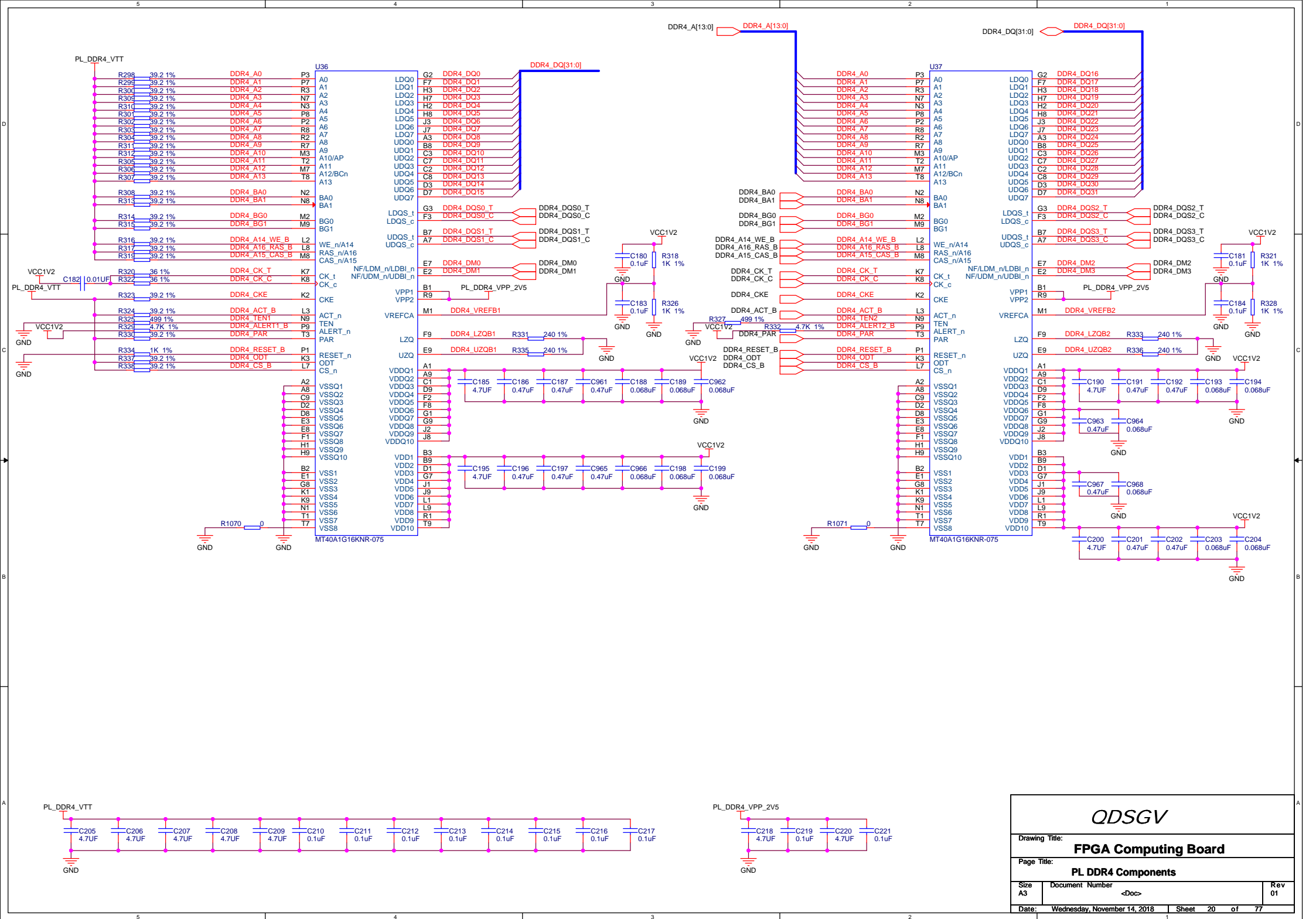


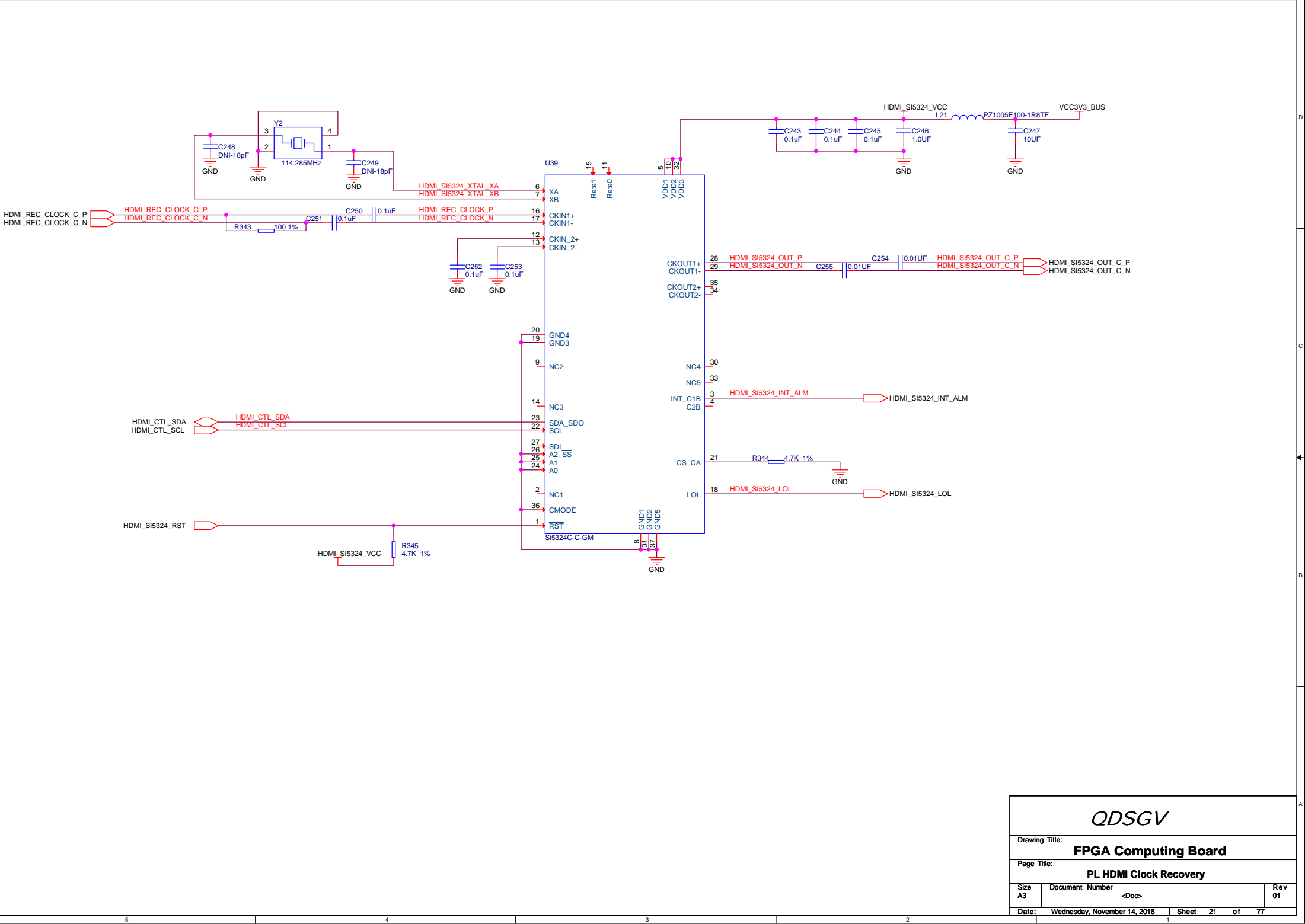
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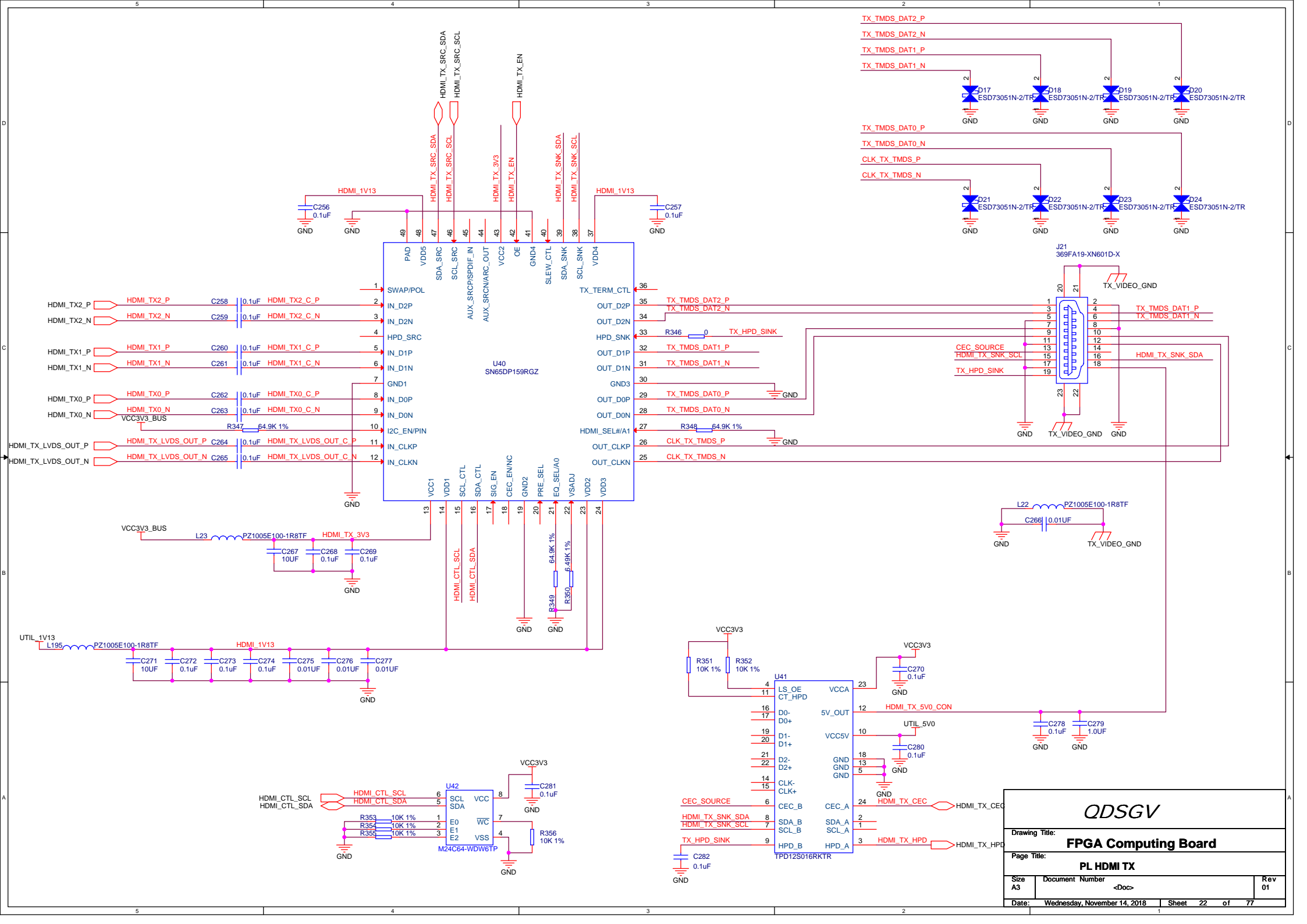
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Page Title:			MGTVCCAUX 1A Regulator		
Size A3	Document Number <Doc>				Rev 01
Date:	Wednesday, November 14, 2018	Sheet 17	of 77		

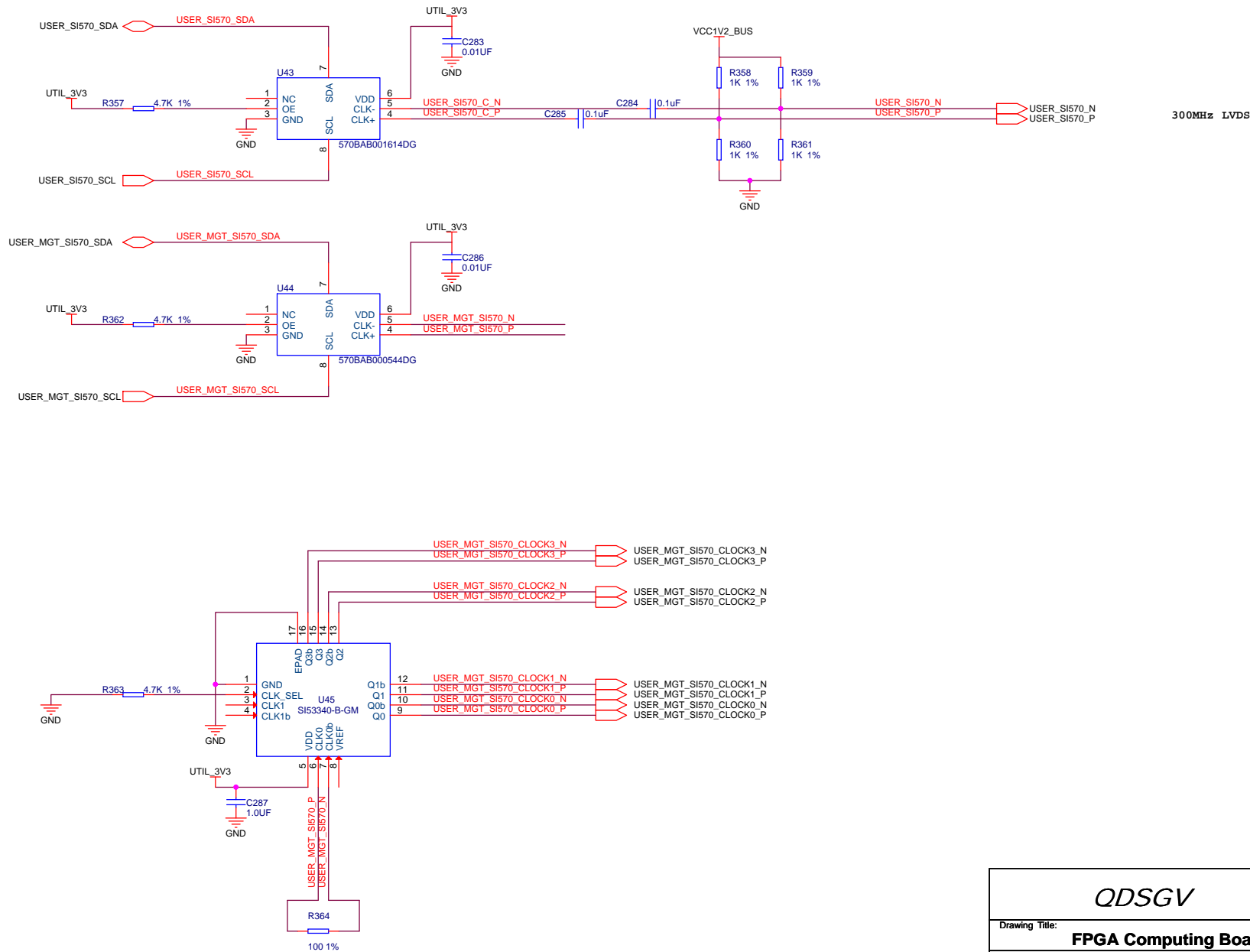




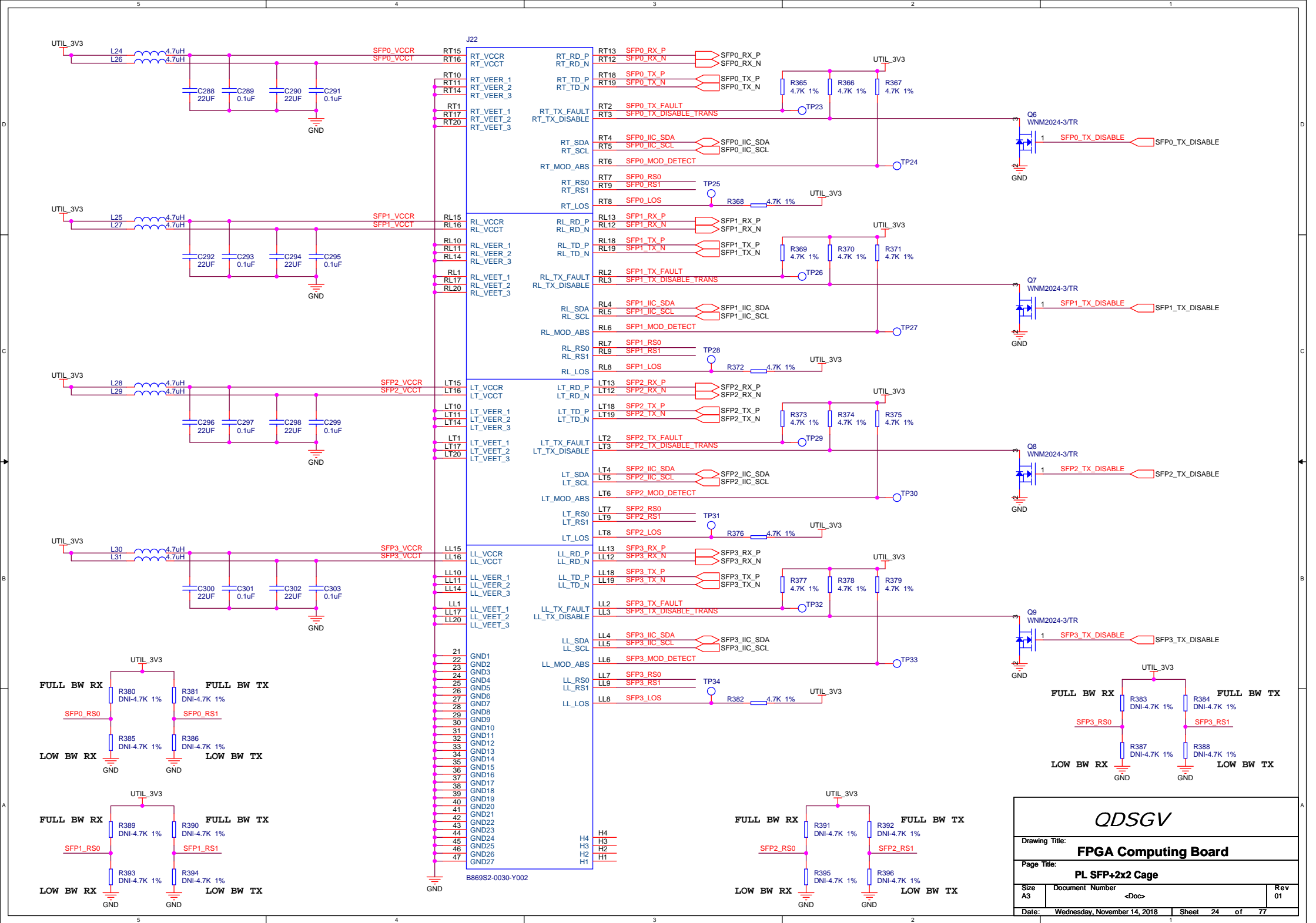




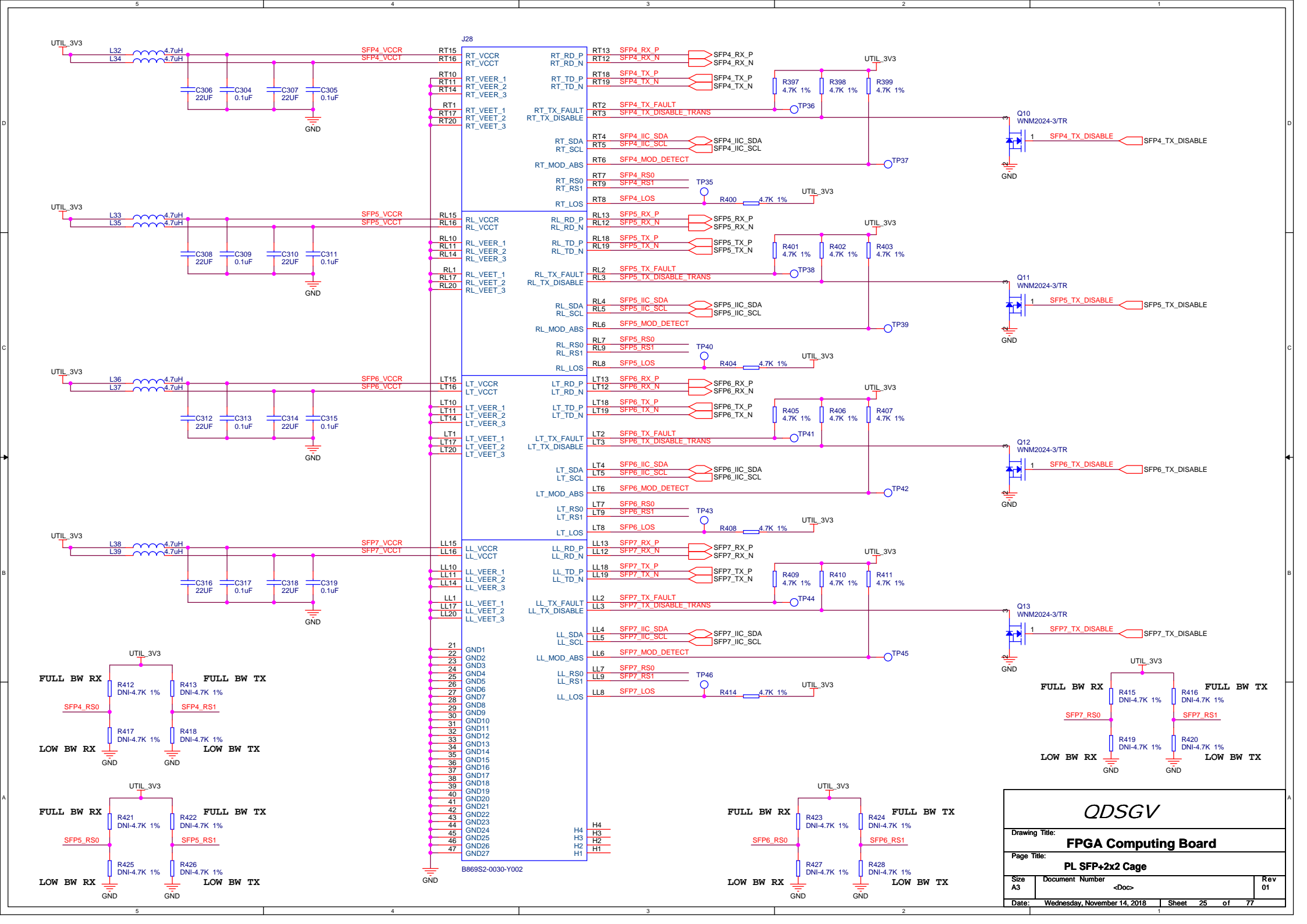


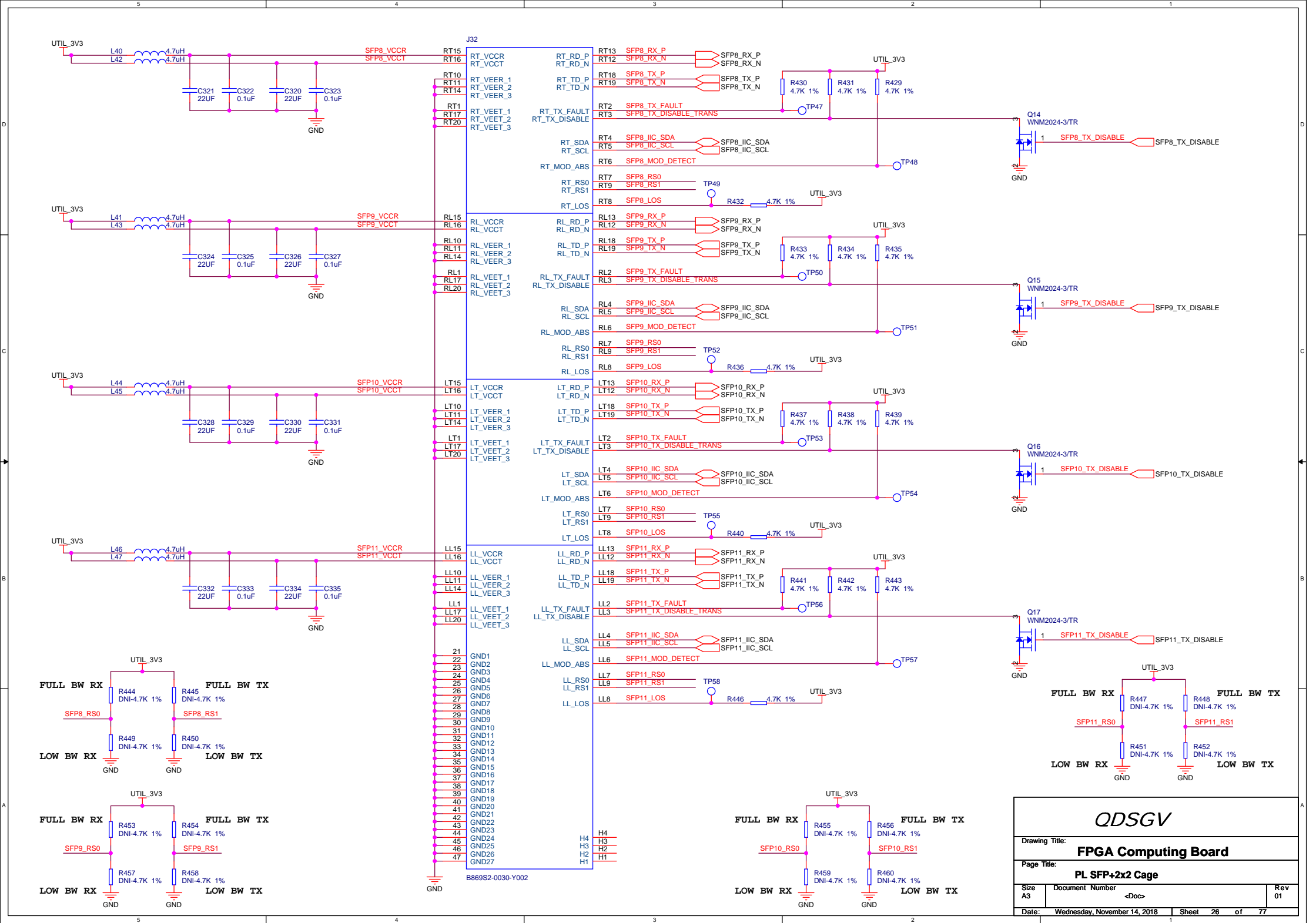


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Page Title: <b>PL Programmable Clocks-SMAs</b>			
Size A3	Document Number <Doc>		Rev 01
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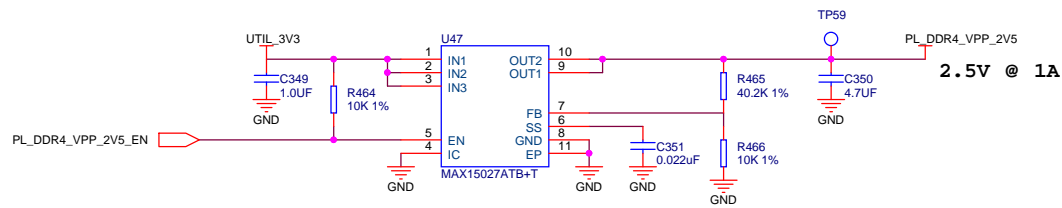






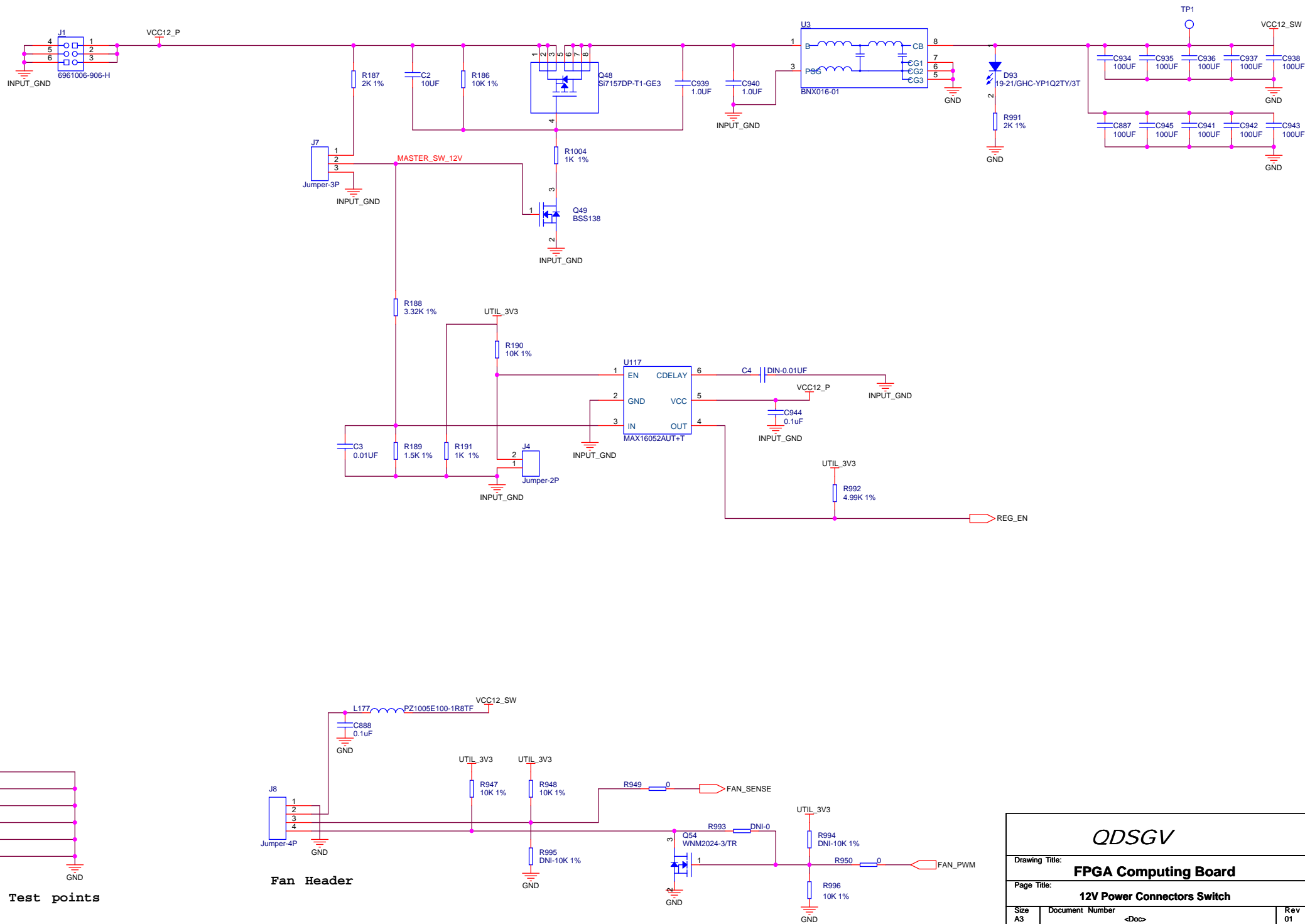






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Drawing Title:			<b>FPGA Computing Board</b>		
Page Title:			<b>PL_DDR4_VPP_2V5 1A Regulator</b>		
Size A3	Document Number <Doc>				Rev 01
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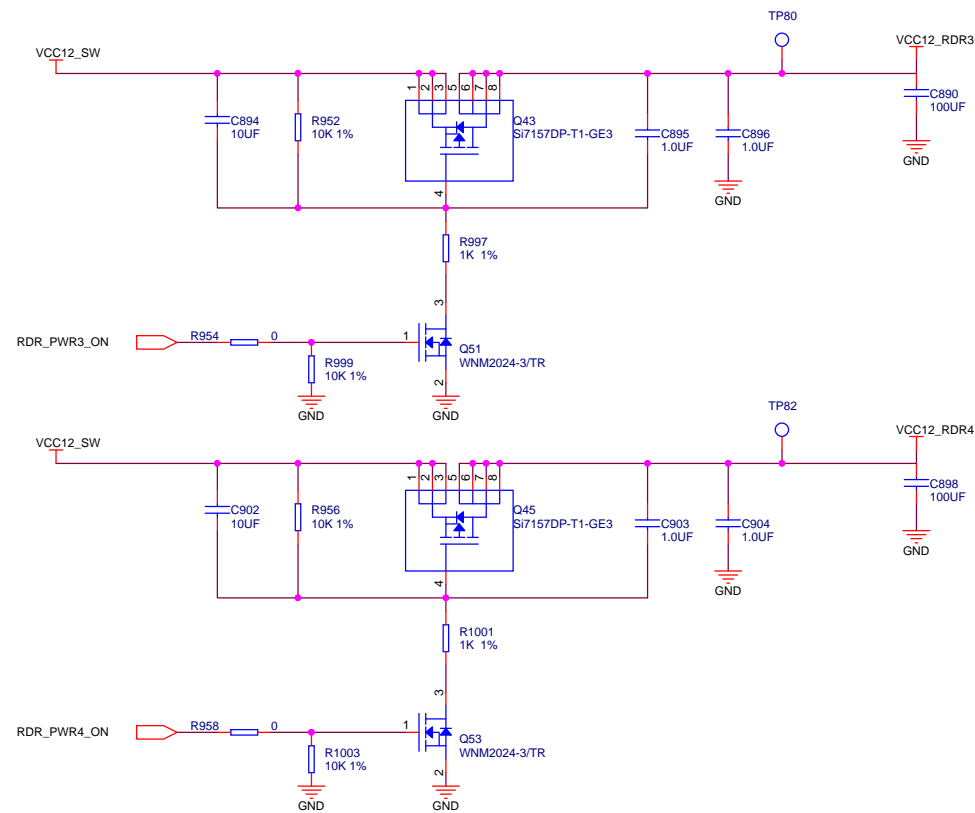
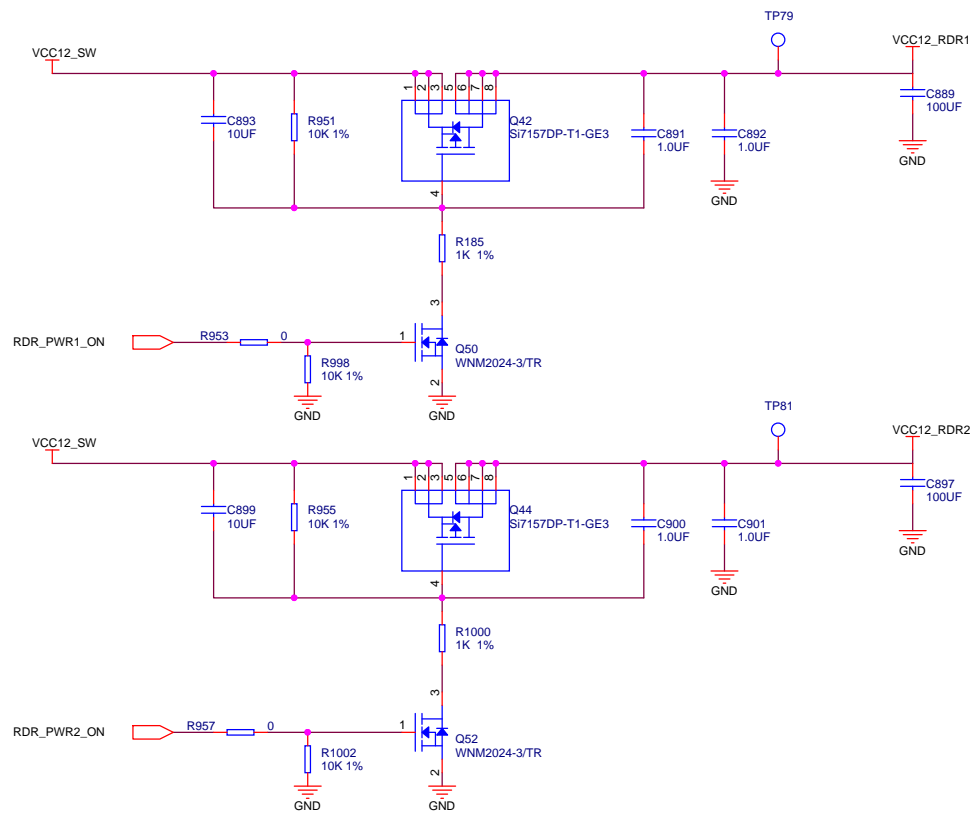


TP2  
TP3  
TP4  
TP5  
TP6  
TP7

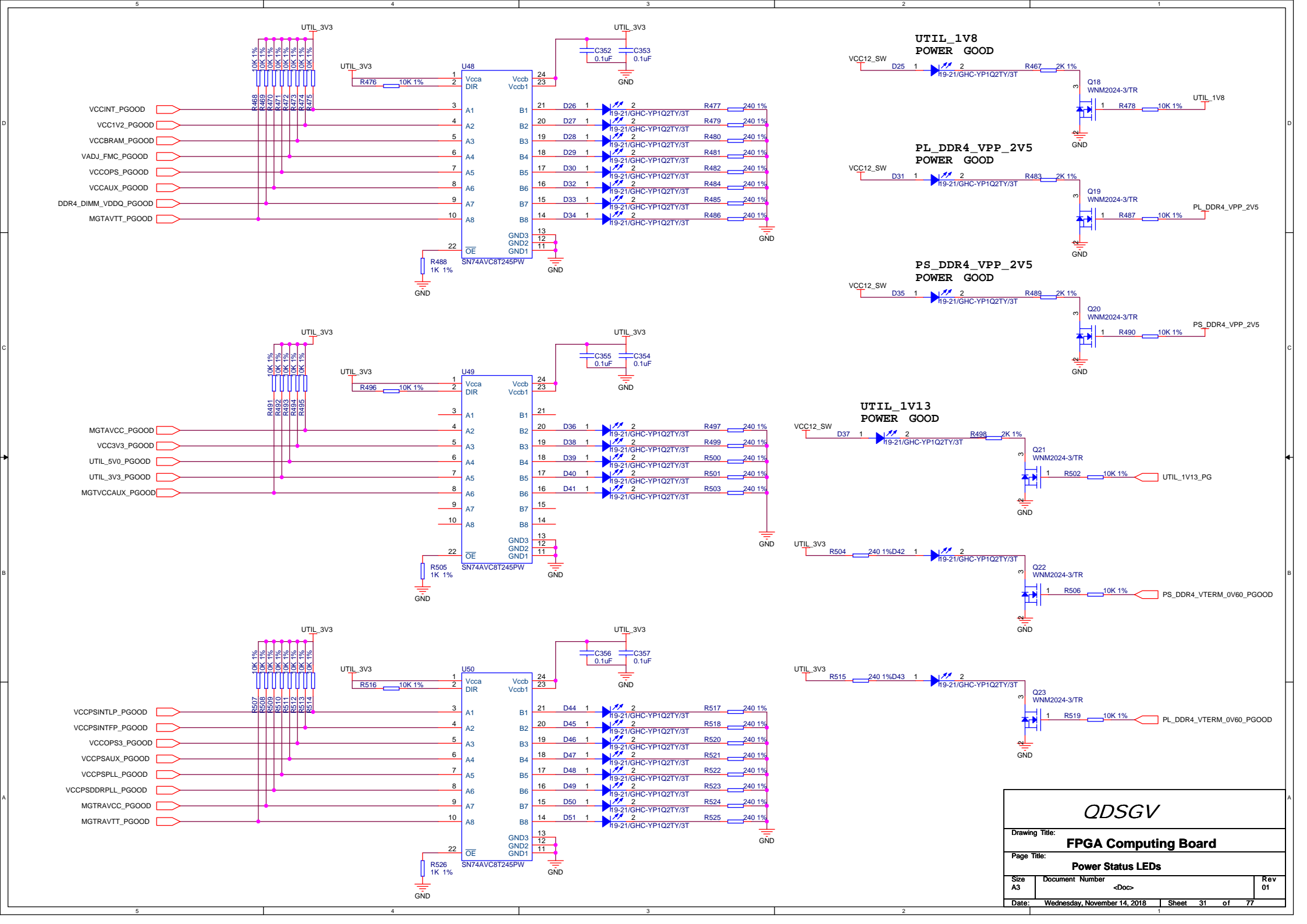
GND Test points

Fan Header

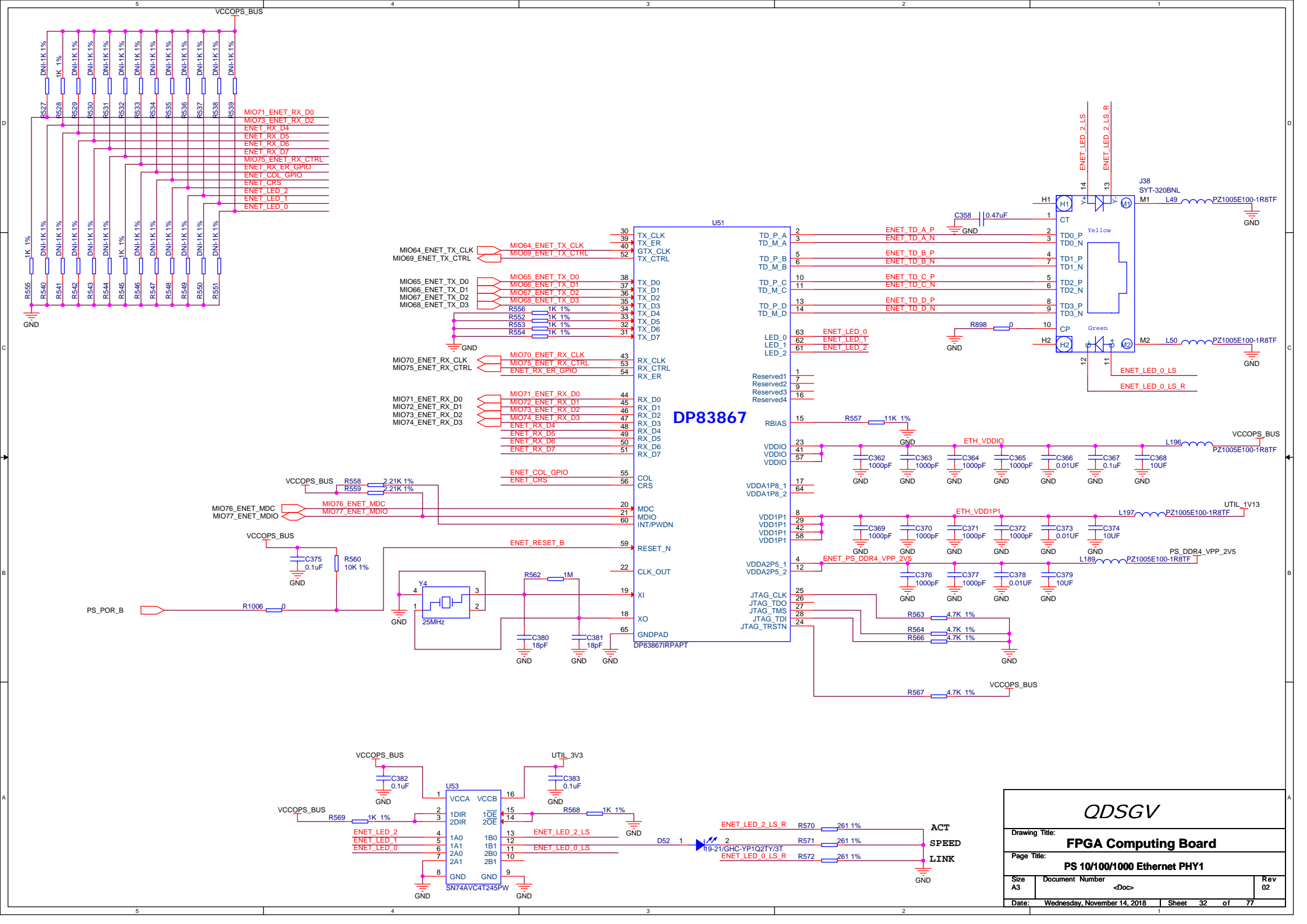
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Page Title: 12V Power Connectors Switch			
Size A3	Document Number	<Doc>	
Date:	Wednesday, November 14, 2018	Sheet 29	of 77



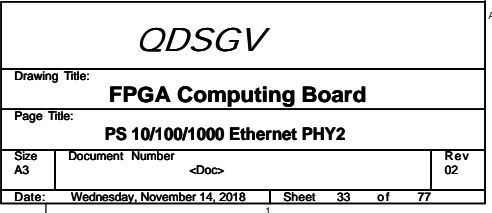
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Page Title: <b>Camera&amp;Radar 12V Power Connectors Switch</b>			
Size A3	Document Number <Doc>		Rev 01
Date:	Wednesday, November 14, 2018	Sheet 30 of 77	

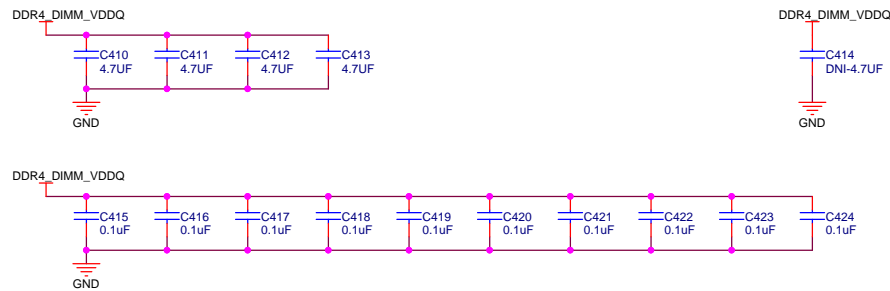


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Page Title: Power Status LEDs			
Size A3	Document Number	<Doc>	Rev 01
Date:	Wednesday, November 14, 2018	Sheet 31	of 77

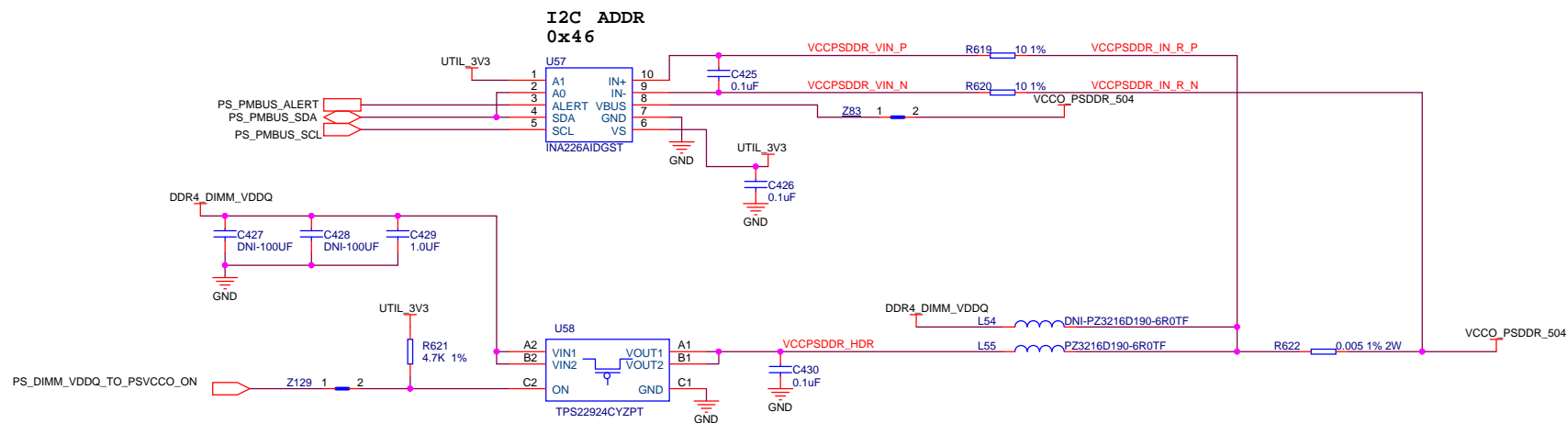








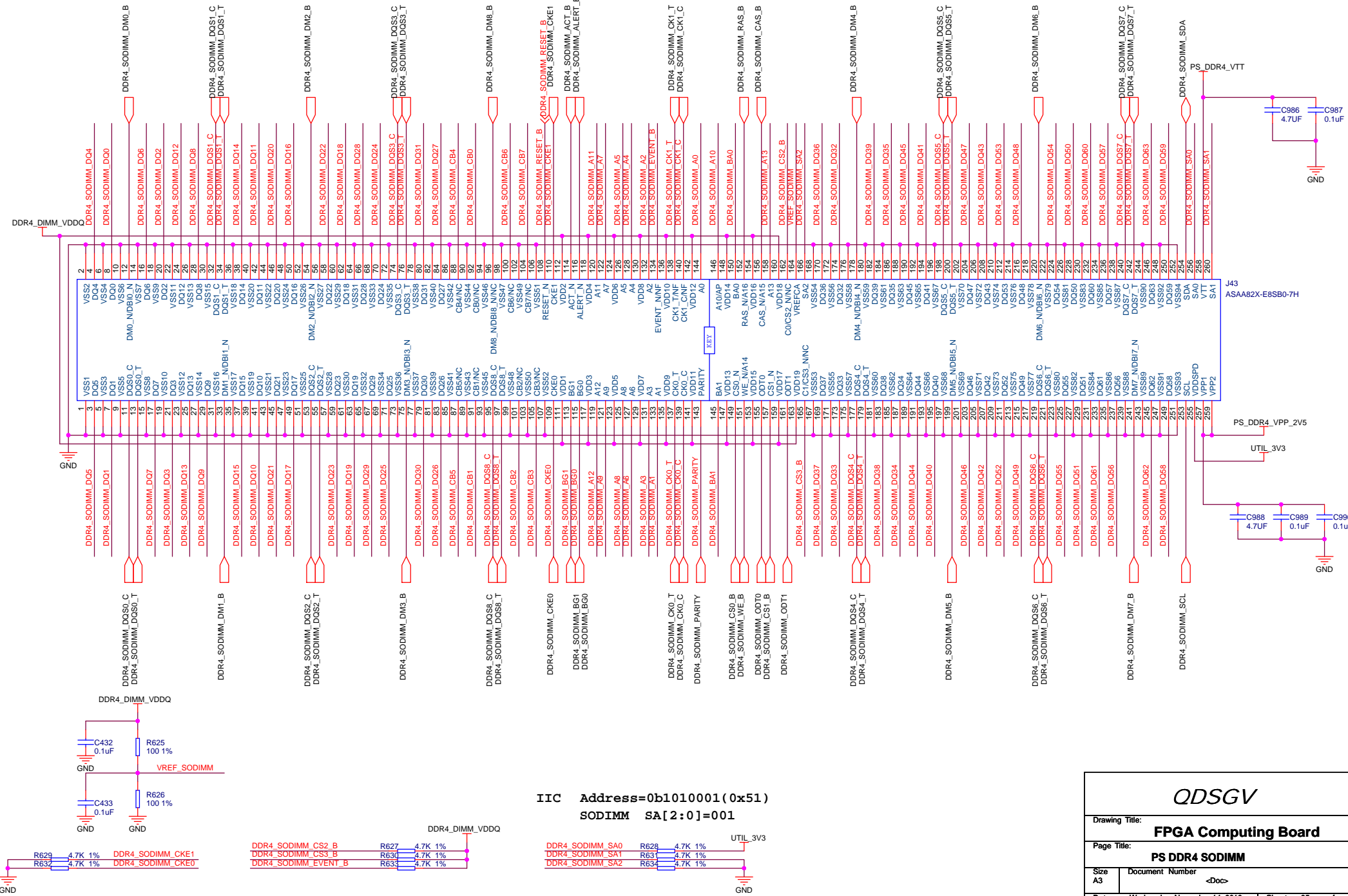
PLACE ABOVE CAPS BENEATH/CLOSE TO DIMM SOCKET



DDR DIMM VCCO DISABLE

DDR DIMM RESET\_B CONTROL

QDSGV			
Drawing Title: <b>FPGA Computing Board</b>			
Page Title: <b>PS DDR4 SODIMM Decoupling</b>			
Size A3	Document Number <Doc>		Rev 02
Date: Wednesday, November 14, 2018	Sheet 34	of 77	



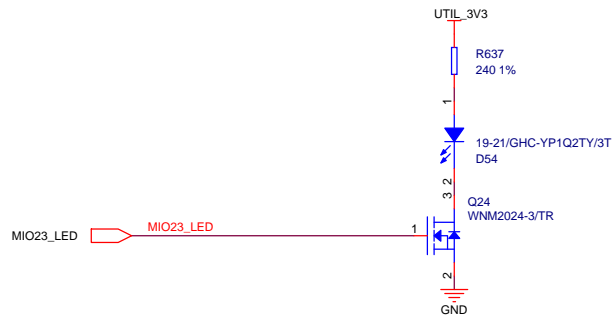
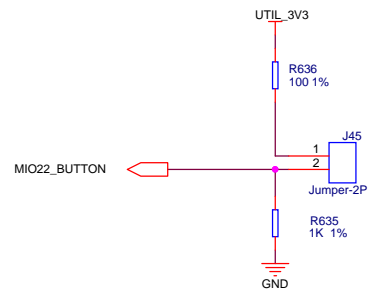
```
IIC  Address=0b1010001(0x51)
SODIMM SA[2:0]=001
```

*QDSGV*

Drawing Title: **FPGA Computing Board**

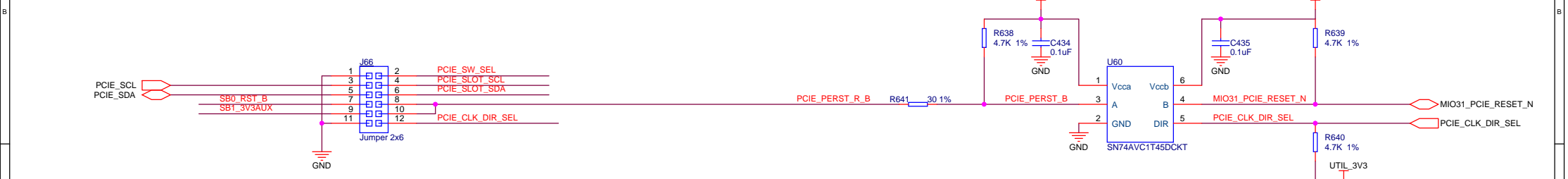
Page Title: **PS DDR4 SODIMM**

Size A3	Document Number <Doc>	Rev 02
Date:	Wednesday, November 14, 2018	Sheet 35 of 77

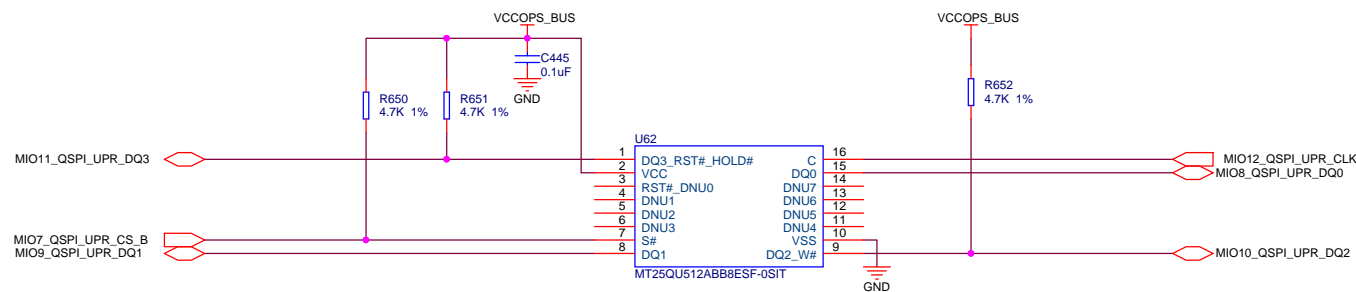
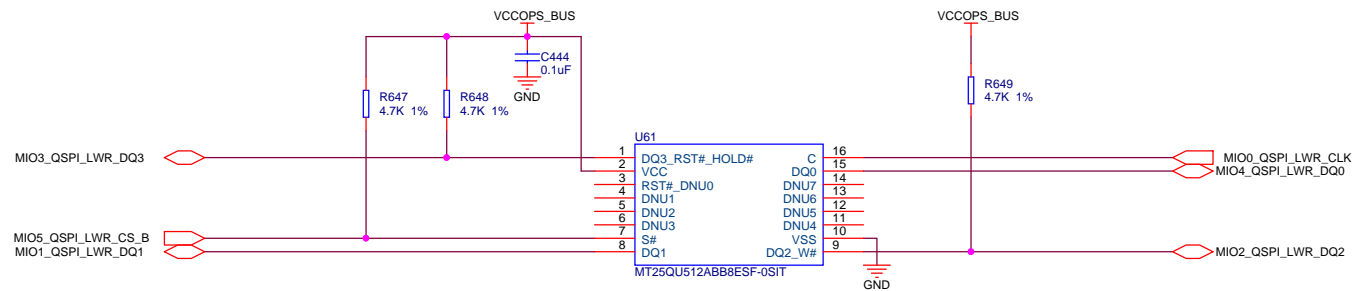


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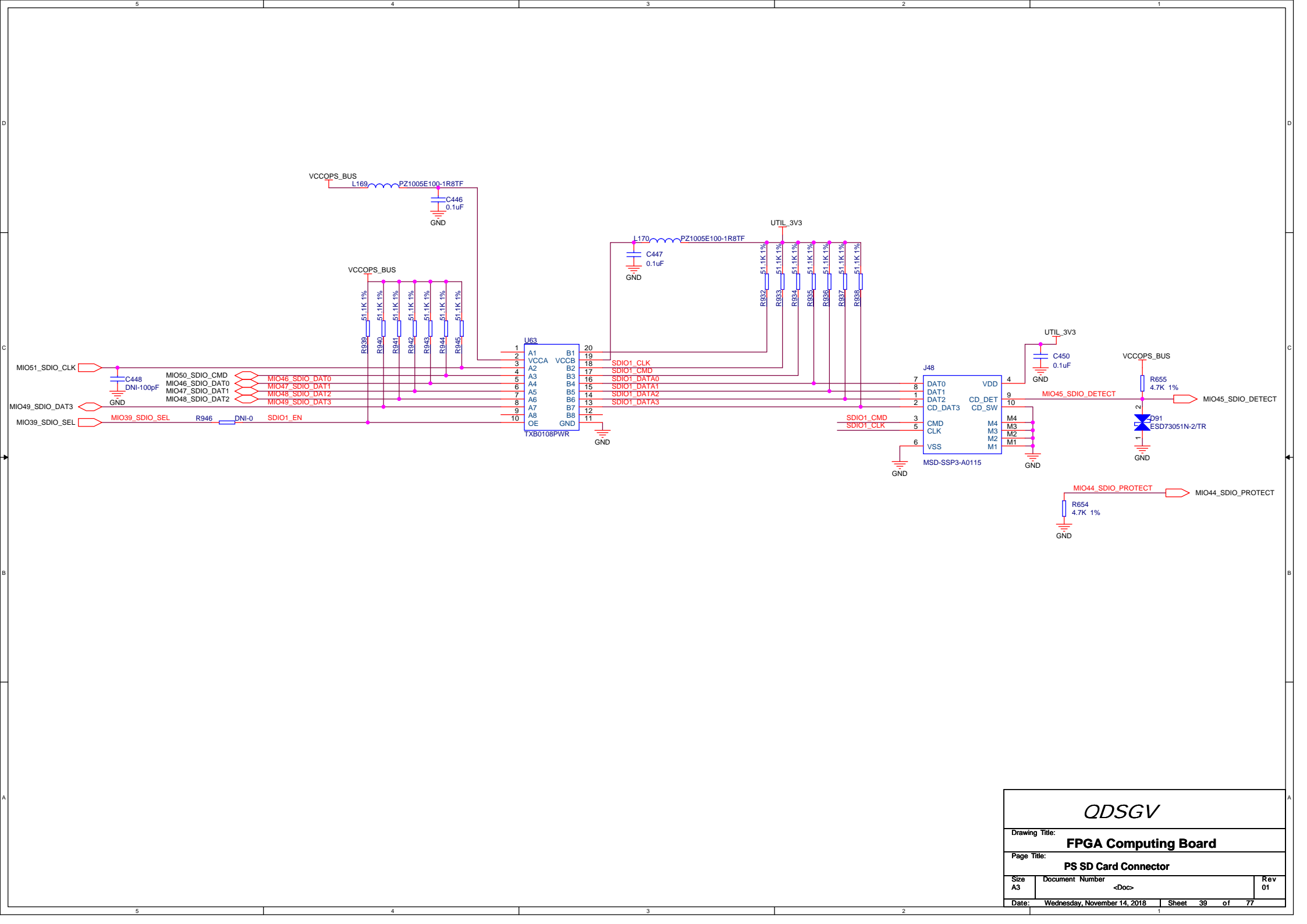
Drawing Title:			
FPGA Computing Board			
Page Title:			
PS MIO PMOD - Button - LED			
Size A3	Document Number <Doc>		Rev 01
Date:	Wednesday, November 14, 2018	Sheet 36 of 77	1

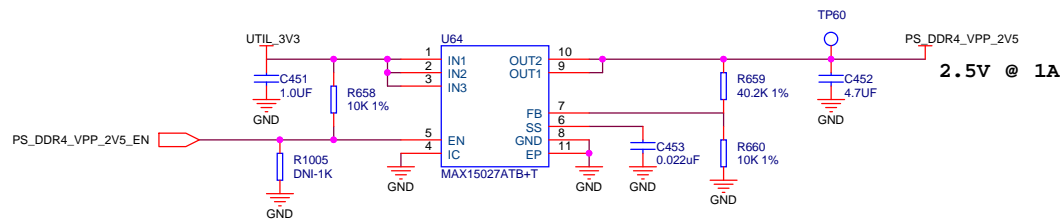


Pin Configuration	PCIe Mode
9-10	Slave(Default)
1-2 3-4 5-6 7-8 11-12	Master



QDSGV		
Drawing Title: FPGA Computing Board		
Page Title: PS QSPI		
Size A3	Document Number <Doc>	Rev 01
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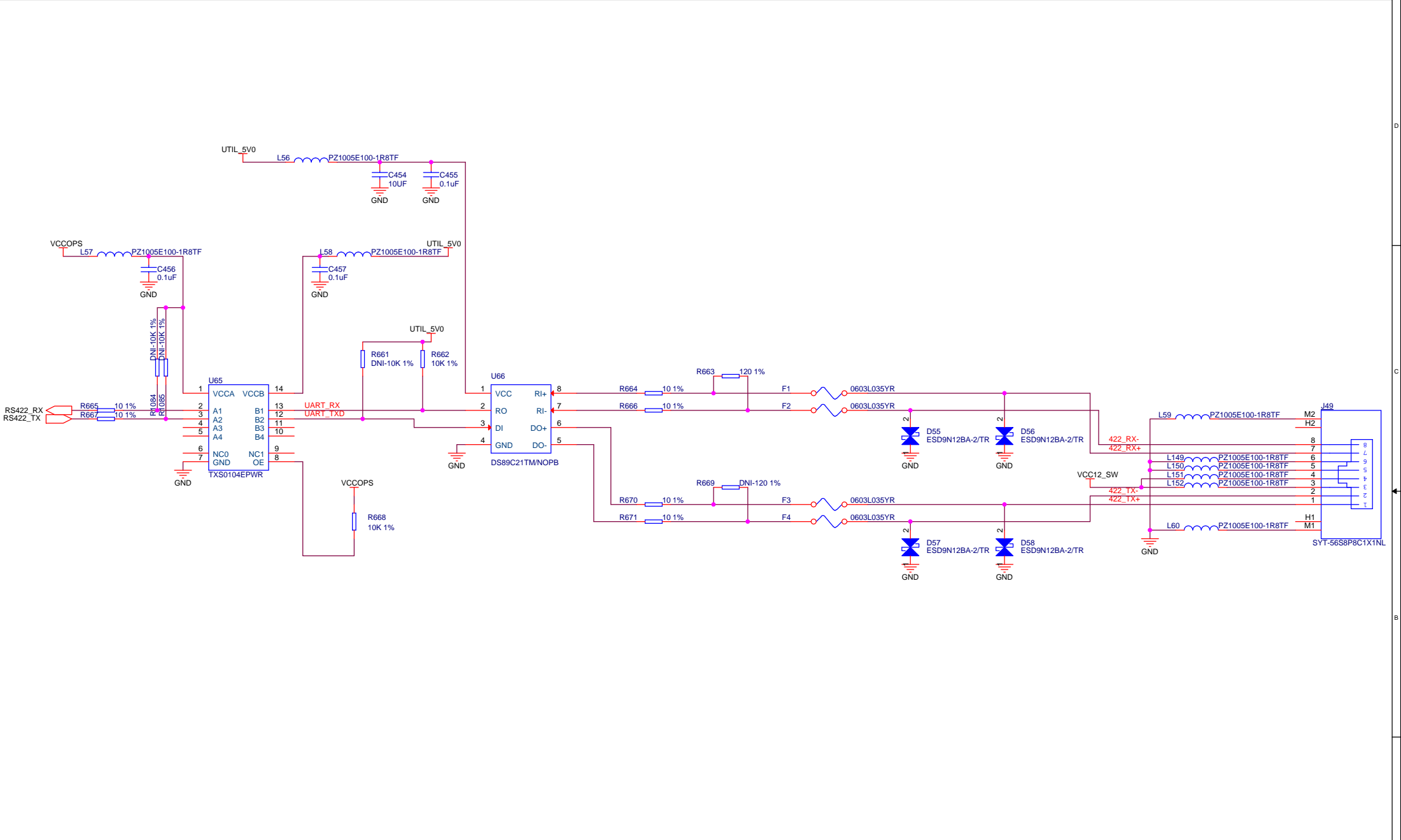


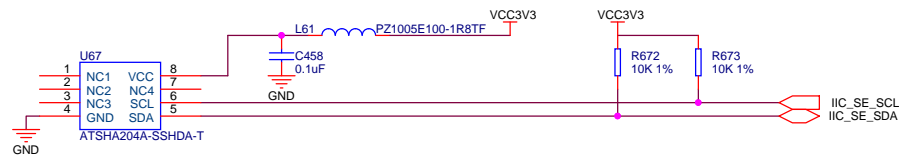


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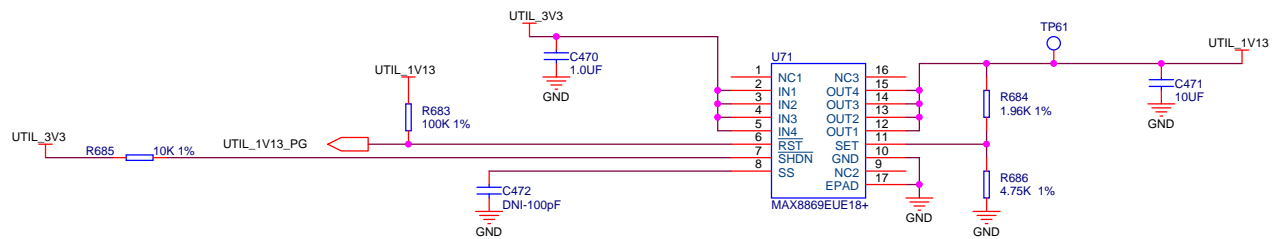
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Size A3	Document Number <Doc>				Rev 01
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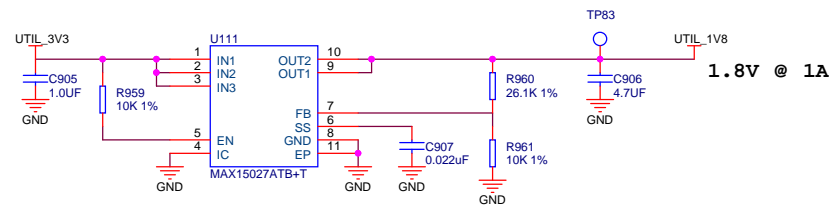


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Page Title: Secure Element			
Size A3	Document Number <Doc>		Rev 01
Date:	Wednesday, November 14, 2018	Sheet 42 of 77	1

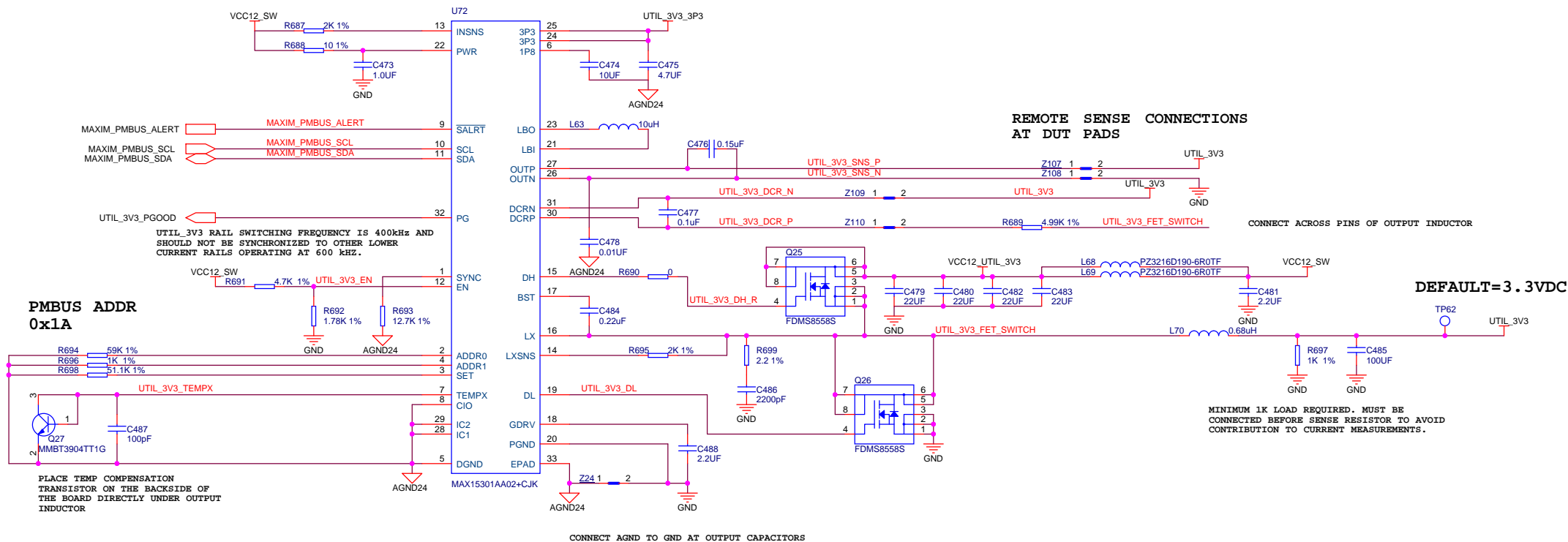


1.13V @ 1A satisfies voltage and total current requirements for TI ENET PHY, as well as HDMI TX and RX transcievers

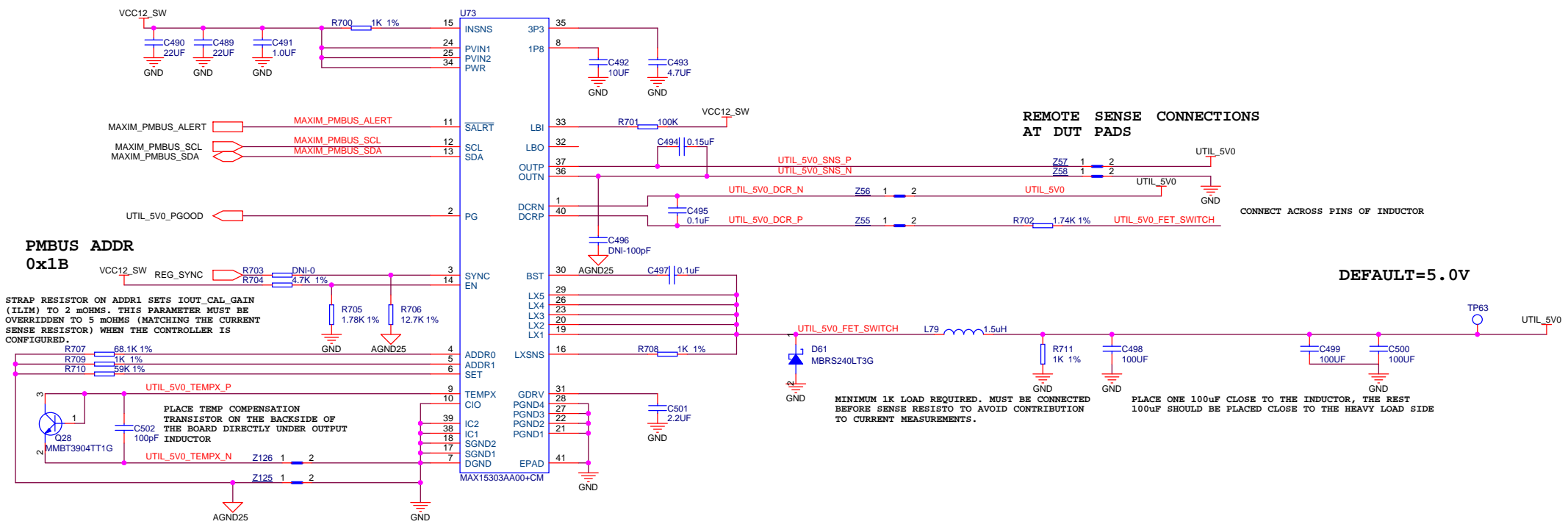
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Page Title: UTIL_1V13 1A Regulator			
Size A3	Document Number <Doc>		Rev 01
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QDSGV			
Drawing Title: FPGA Computing Board			
Page Title: UTIL_1V8 1A Regulator			
Size A3	Document Number <Doc>		Rev 01
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QDSGV			
Drawing Title: <b>FPGA Computing Board</b>			
Page Title: <b>UTIL_3V3 20A Regulator</b>			
Size A3	Document Number <Doc>		Rev 01
Date: Wednesday, November 14, 2018	Sheet 45	of 77	



**PMBUS ADDR**  
**0x1B**

STRAP RESISTOR ON ADDR1 SETS IOUT\_CAL\_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT

**REMOTE SENSE CONNECTIONS AT DUT PADS**

CONNECT ACROSS PINS OF INDUCTOR

**DEFAULT=5.0V**

MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTO TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

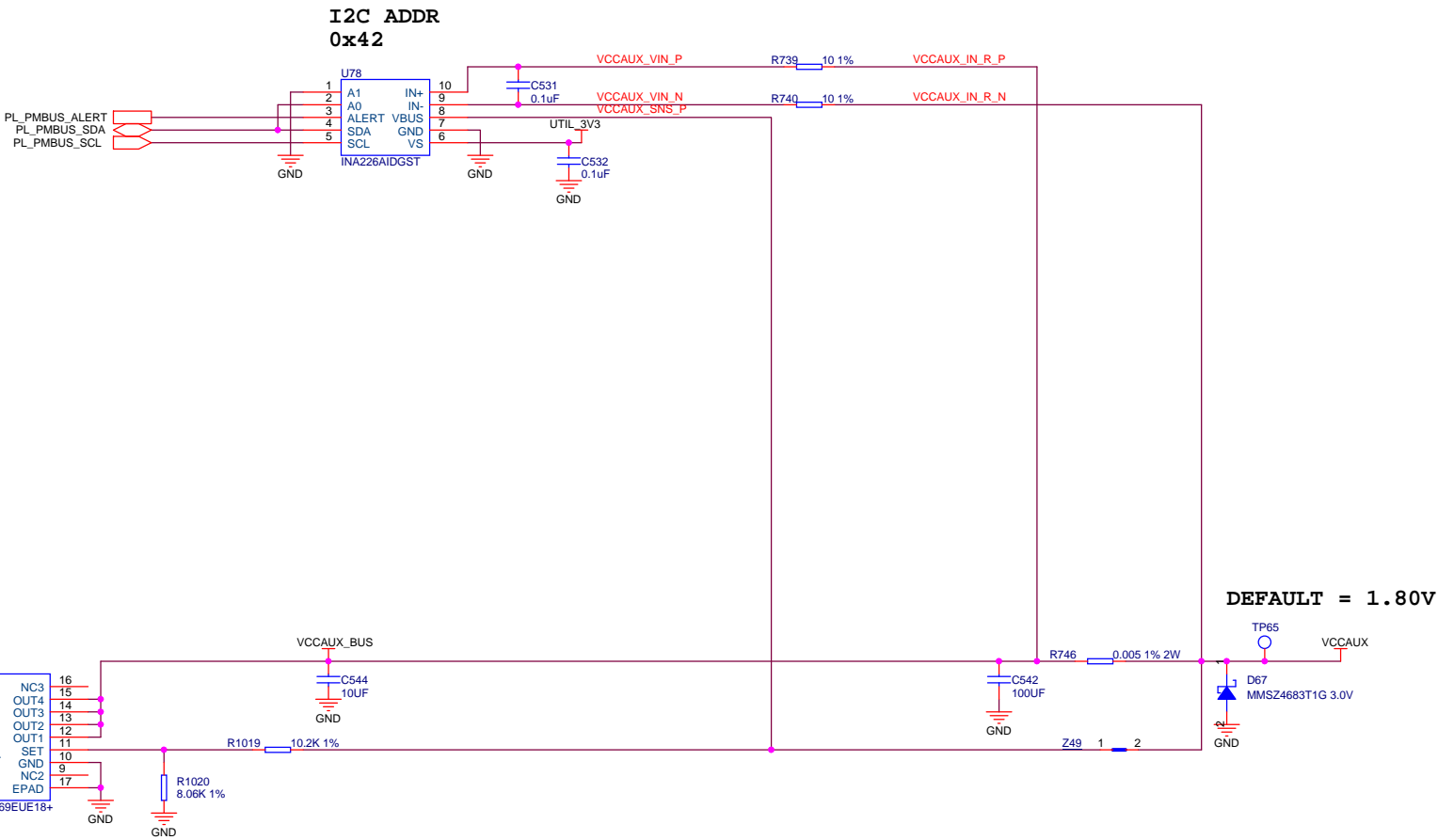
PLACE ONE 100uF CLOSE TO THE INDUCTOR, THE REST 100uF SHOULD BE PLACED CLOSE TO THE HEAVY LOAD SIDE

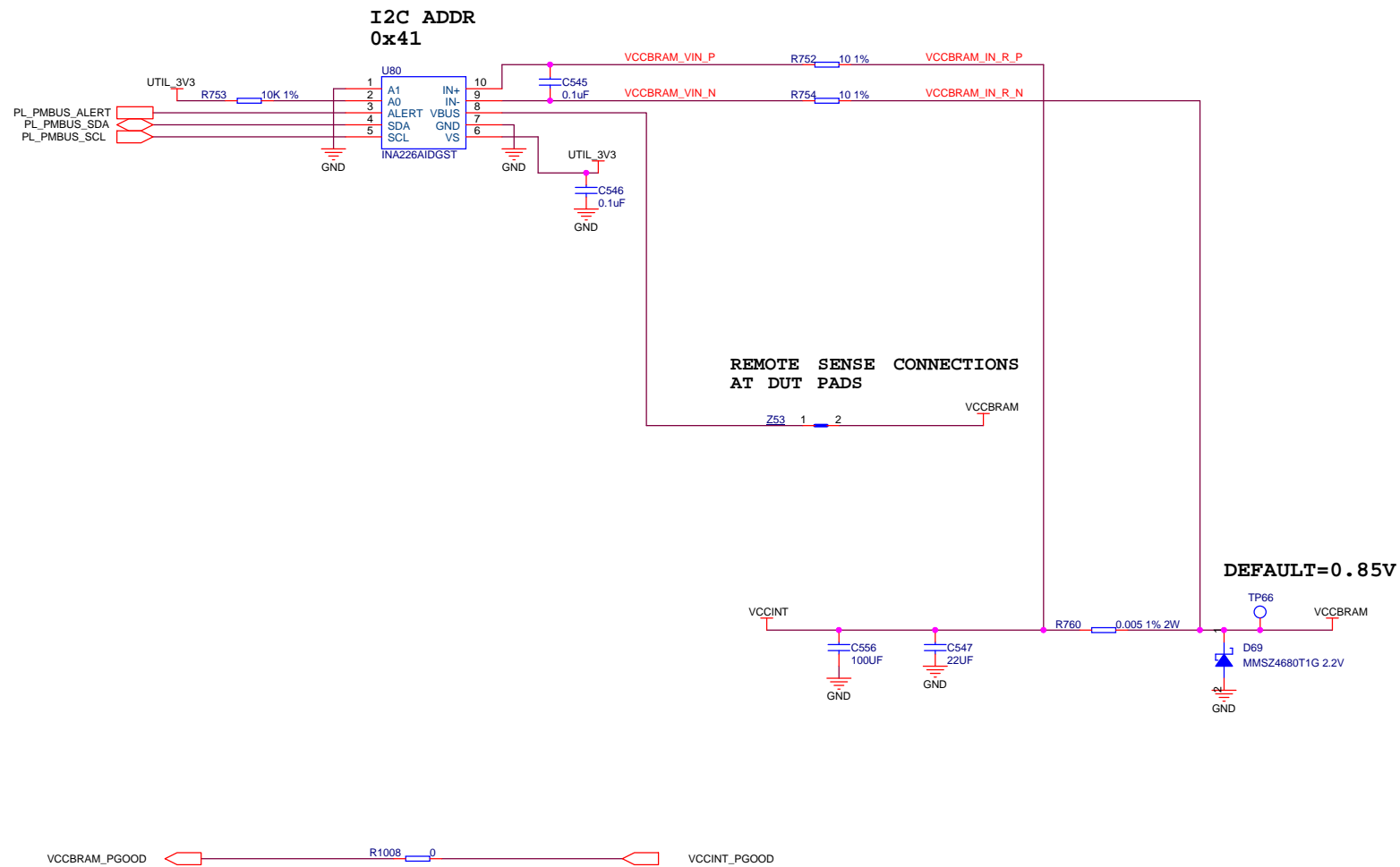
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Page Title: <b>UTIL_5V0 6A Regulator</b>			
Size A3	Document Number <Doc>		Rev 01
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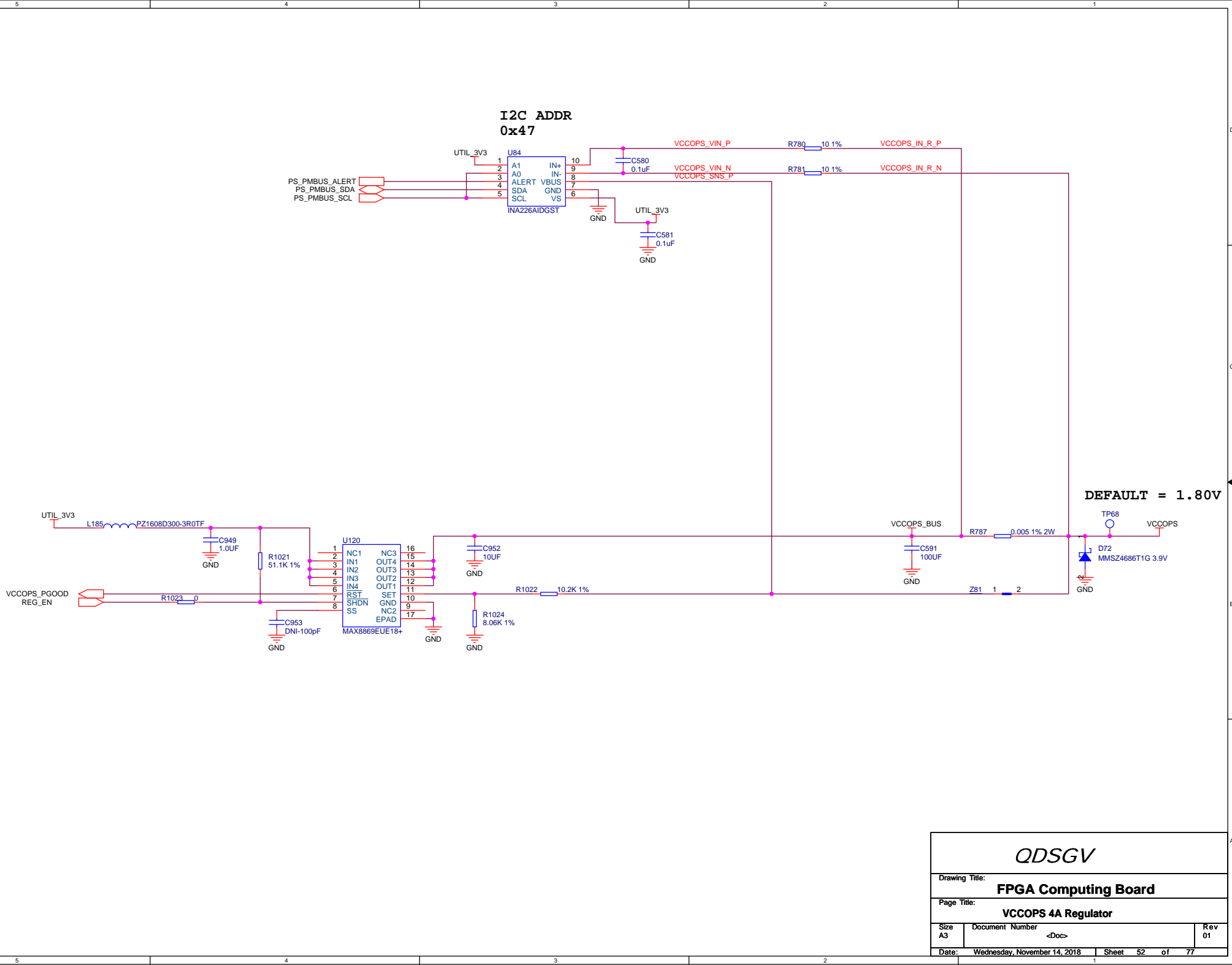






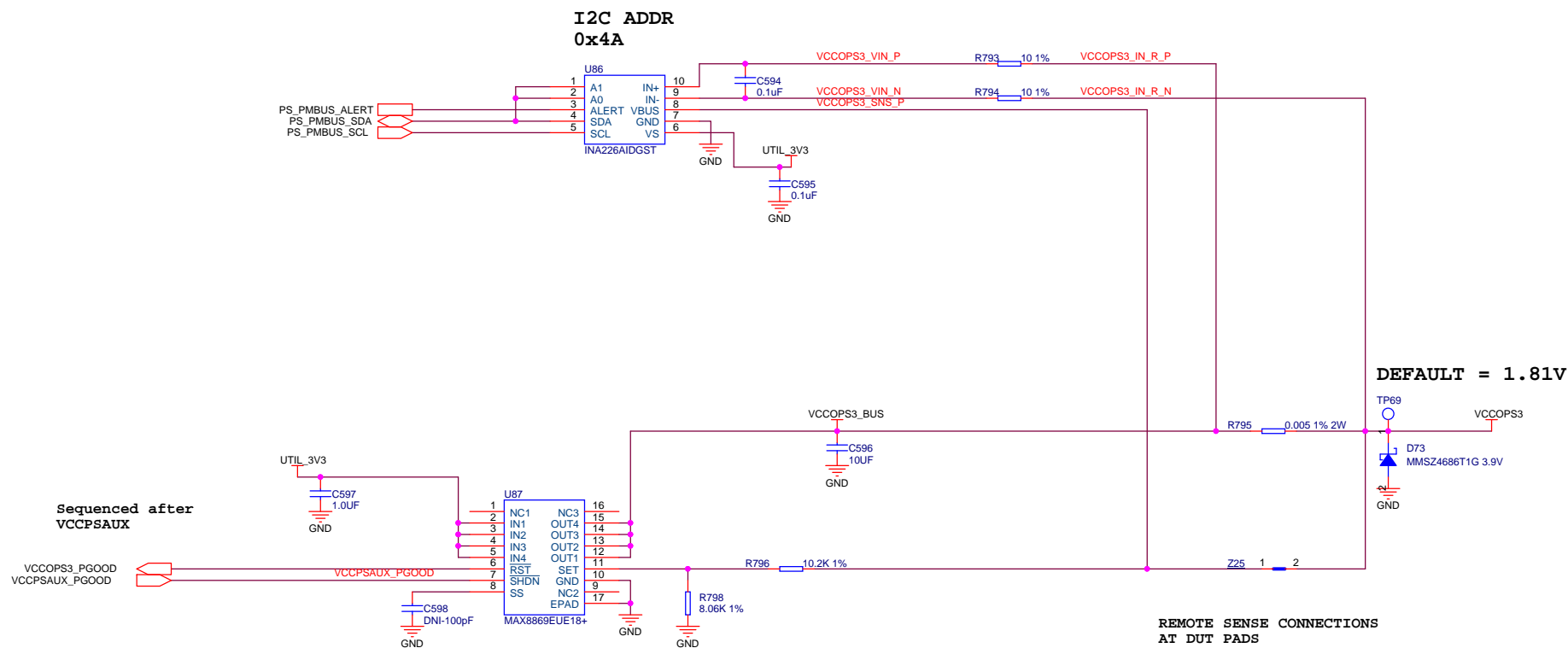




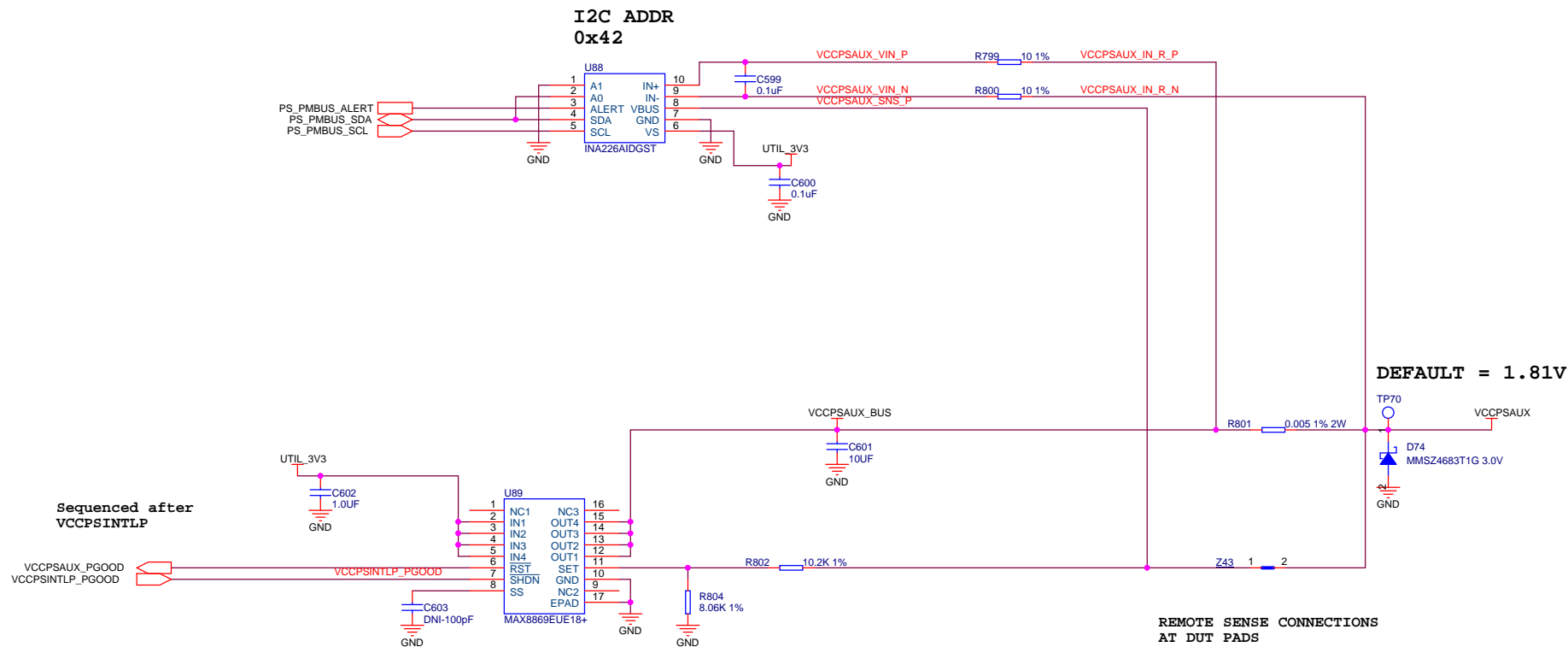


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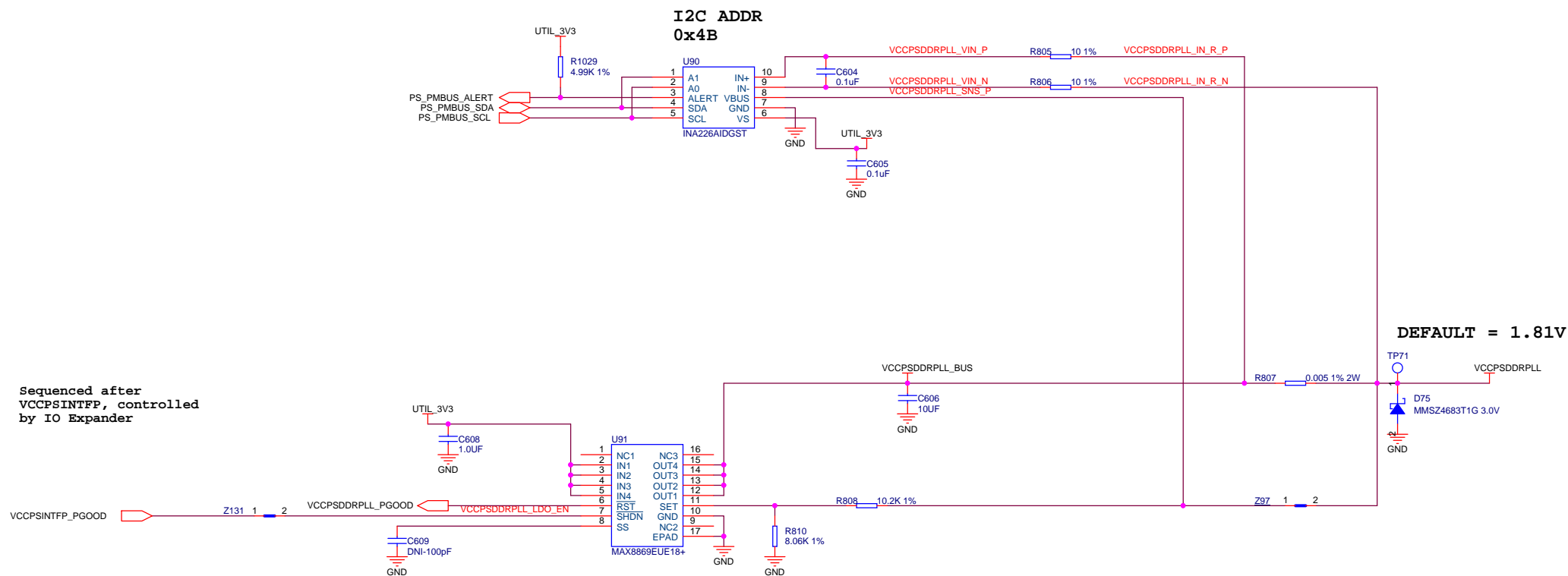
Drawing Title:			FPGA Computing Board		
Page Title:			VCCOPS 4A Regulator		
Size A3	Document Number <Doc>				Rev 01
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QDSGV			
Drawing Title: <b>FPGA Computing Board</b>			
Page Title: <b>VCCOPS3 300MA Regulator</b>			
Size A3	Document Number <Doc>		Rev 01
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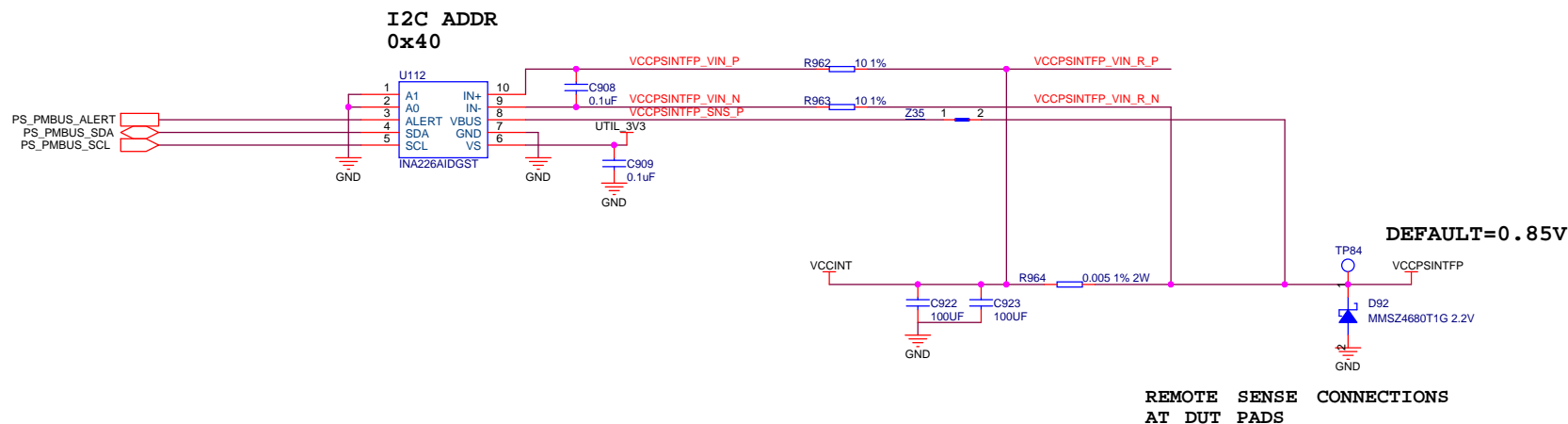


Sequenced after  
VCCPSINTFP, controlled  
by IO Expander



*QDSGV*

Drawing Title:			FPGA Computing Board		
Page Title:			VCCPSDDRPLL 100MA Regulator		
Size A3	Document Number <Doc>				Rev 01
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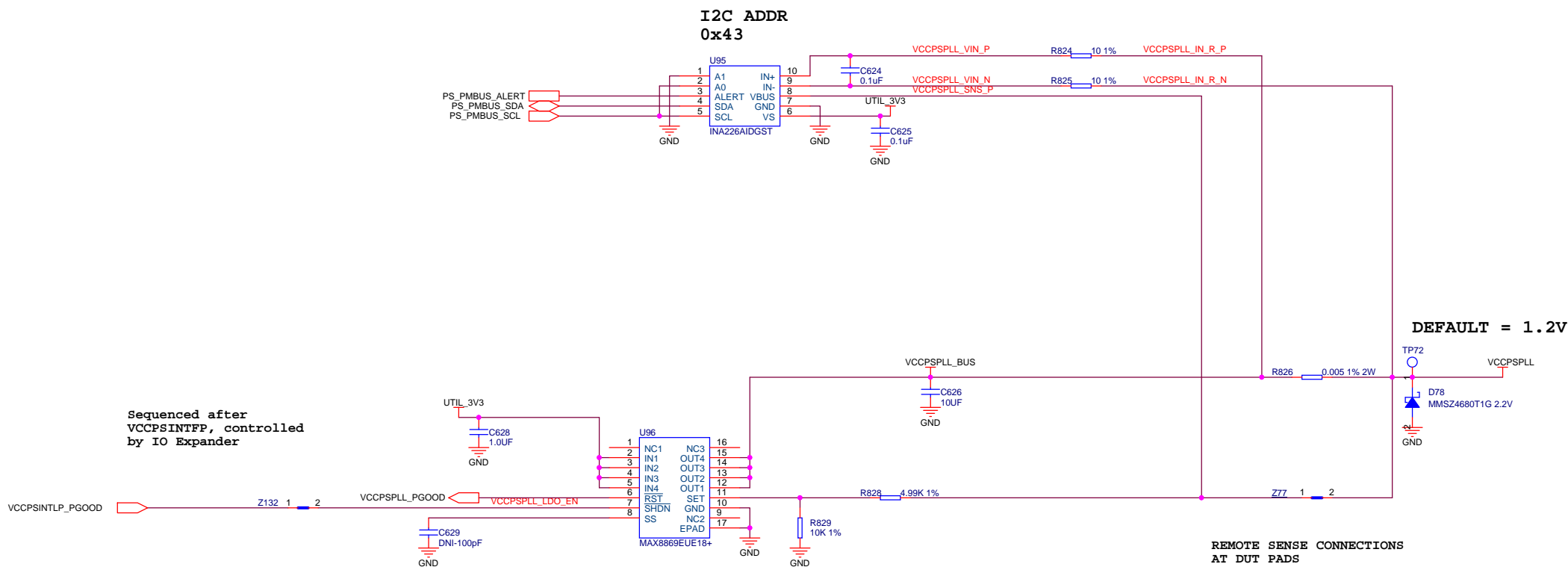


QDSGV

Drawing Title:			FPGA Computing Board		
Page Title:			VCCPSINTFP 10A Regulator		
Size A3	Document Number <Doc>				Rev 01
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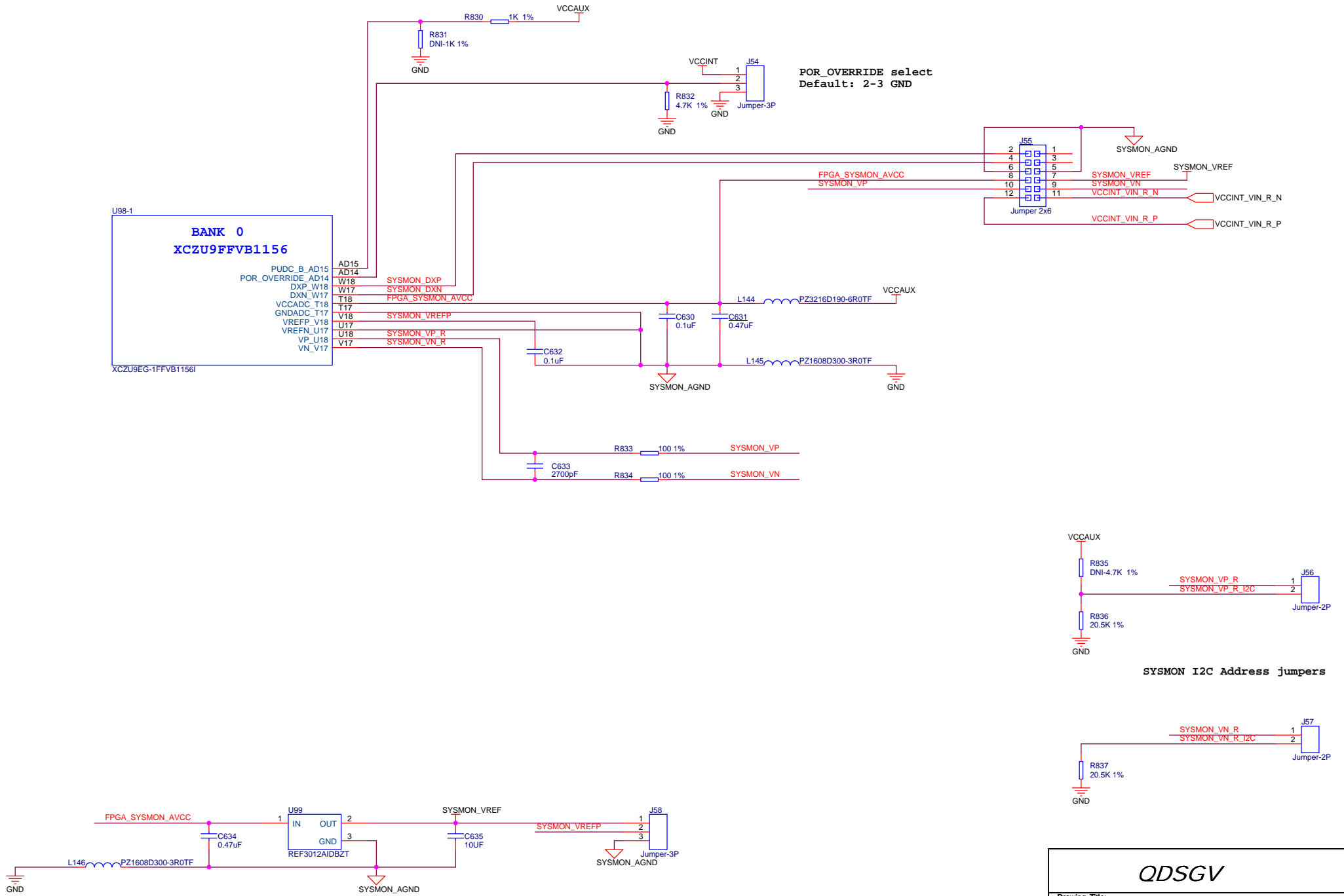




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Drawing Title: <b>FPGA Computing Board</b>			
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Size A3	Document Number <Doc>		Rev 01
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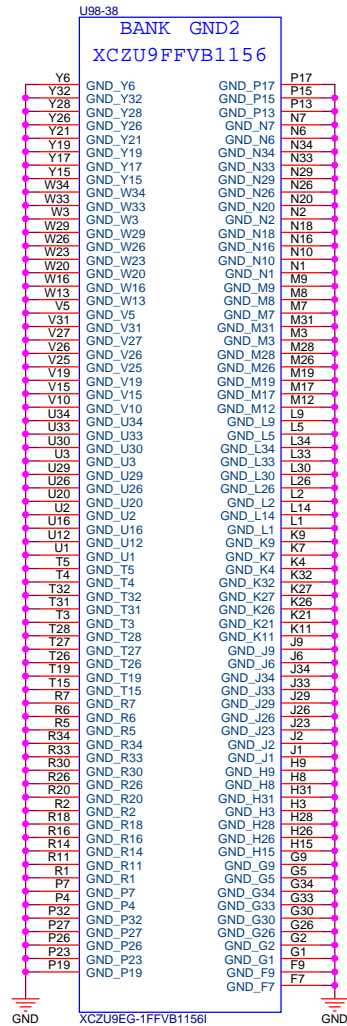
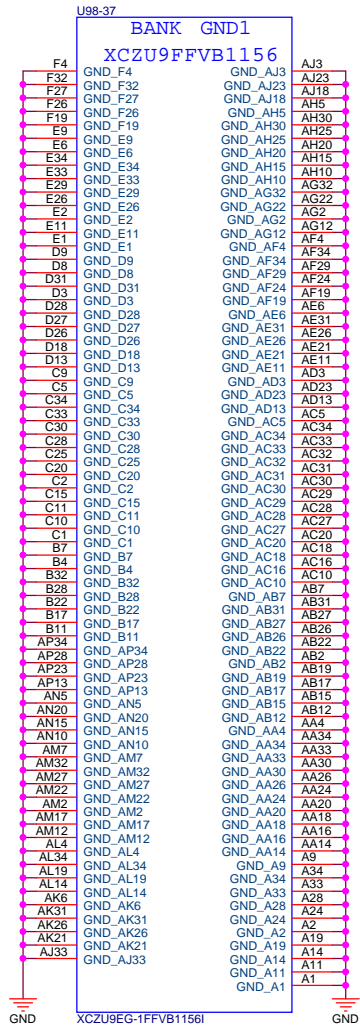


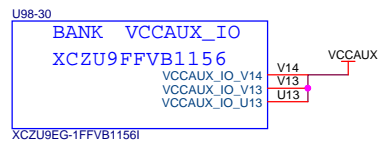
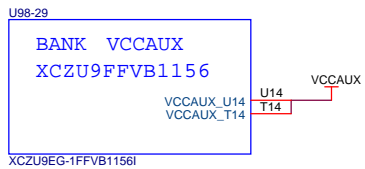
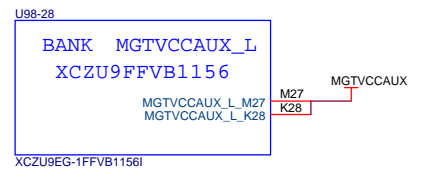
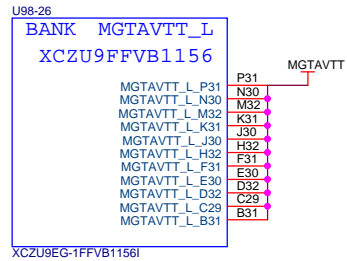
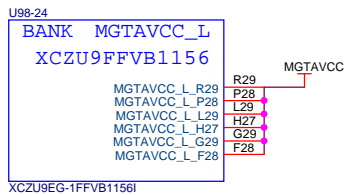
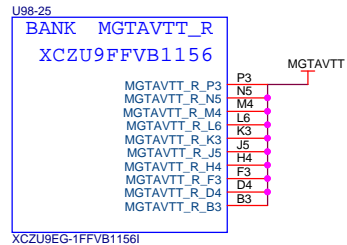
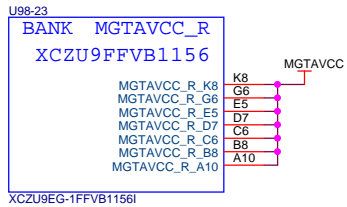
POR\_OVERRIDE select  
Default: 2-3 GND

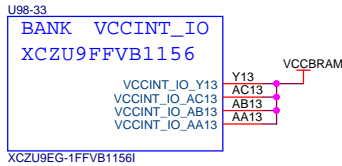
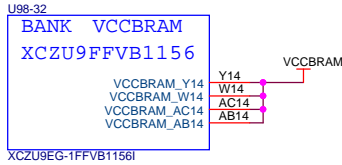
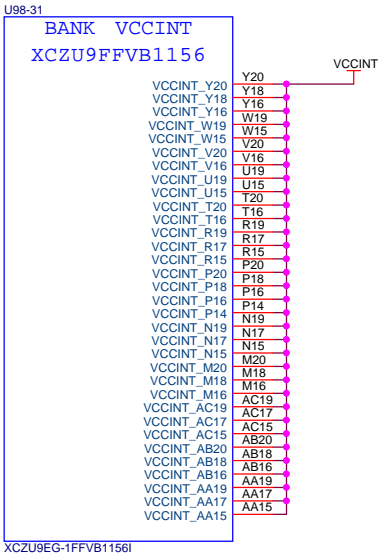


QDSGV

Drawing Title:			FPGA Computing Board		
Page Title:			Zynq Bank 0		
Size A3	Document Number <Doc>				Rev 02
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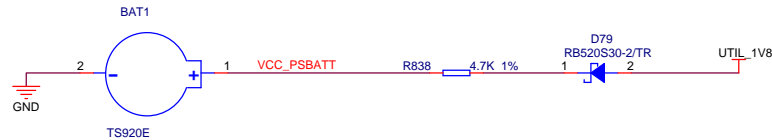
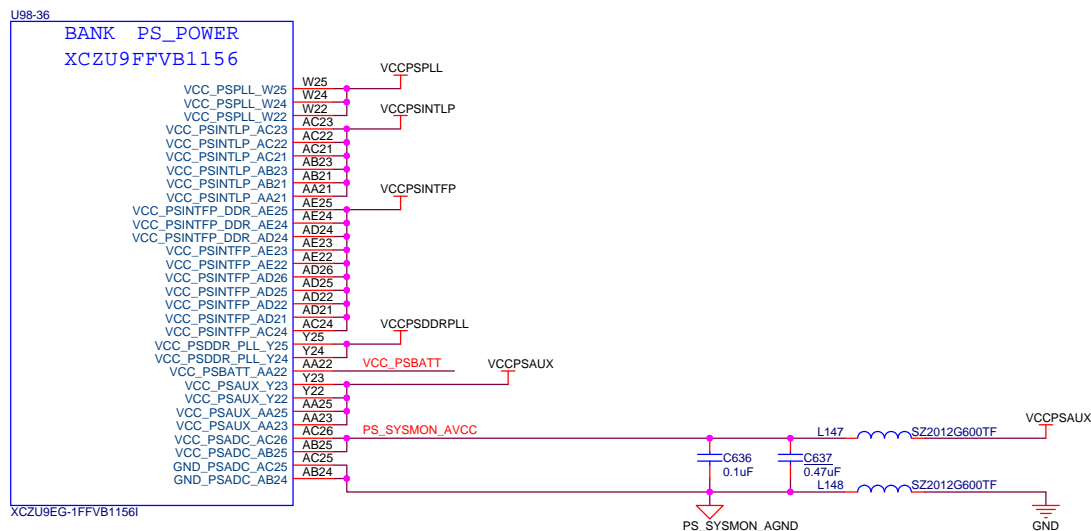
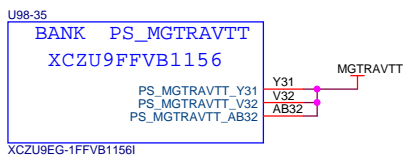
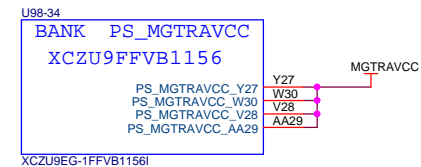




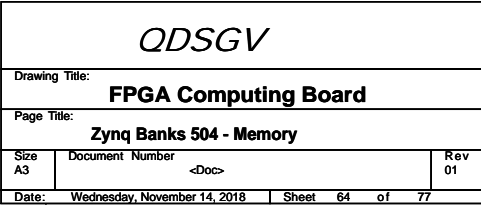


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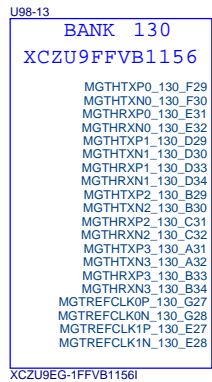
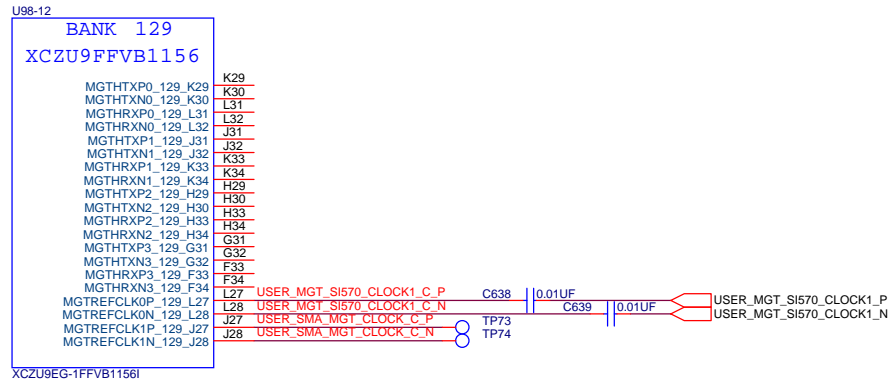
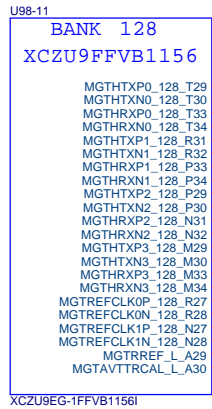
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FPGA Computing Board			
Page Title:			
Zynq Power 2			
Size A3	Document Number <Doc>		Rev 01
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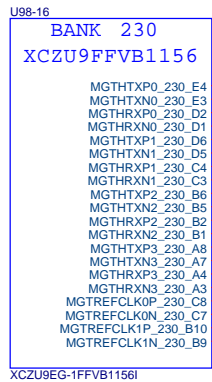
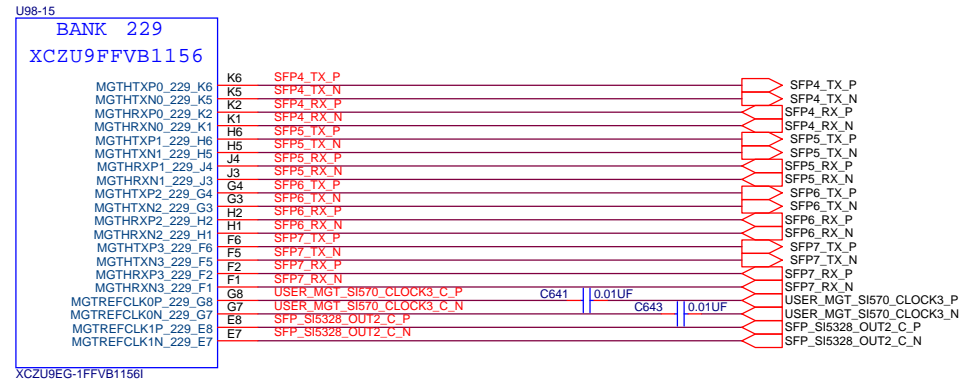
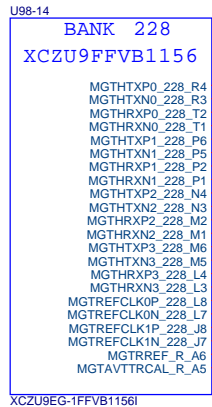


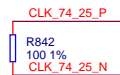
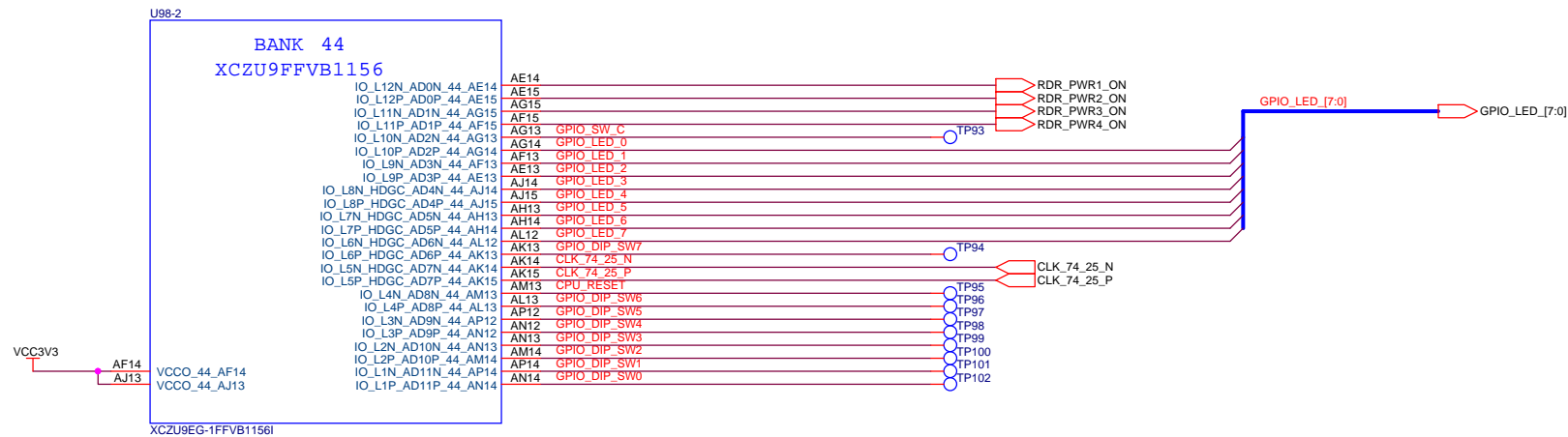
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Size A3	Document Number <Doc>		Rev 01
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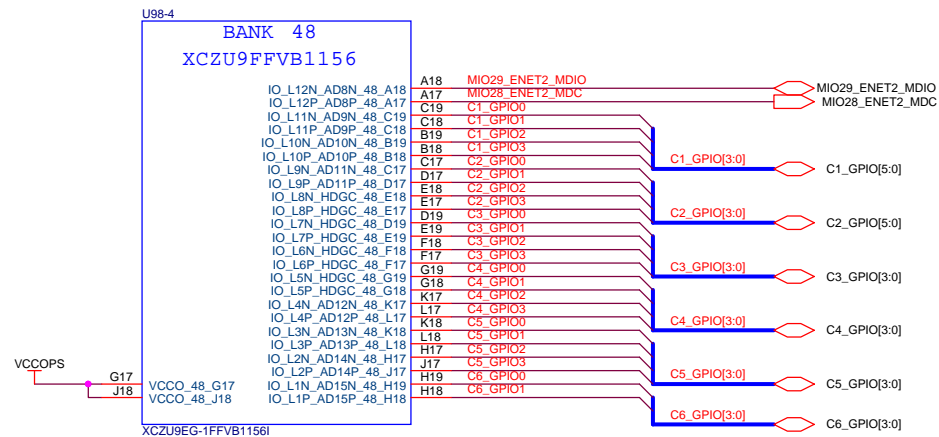




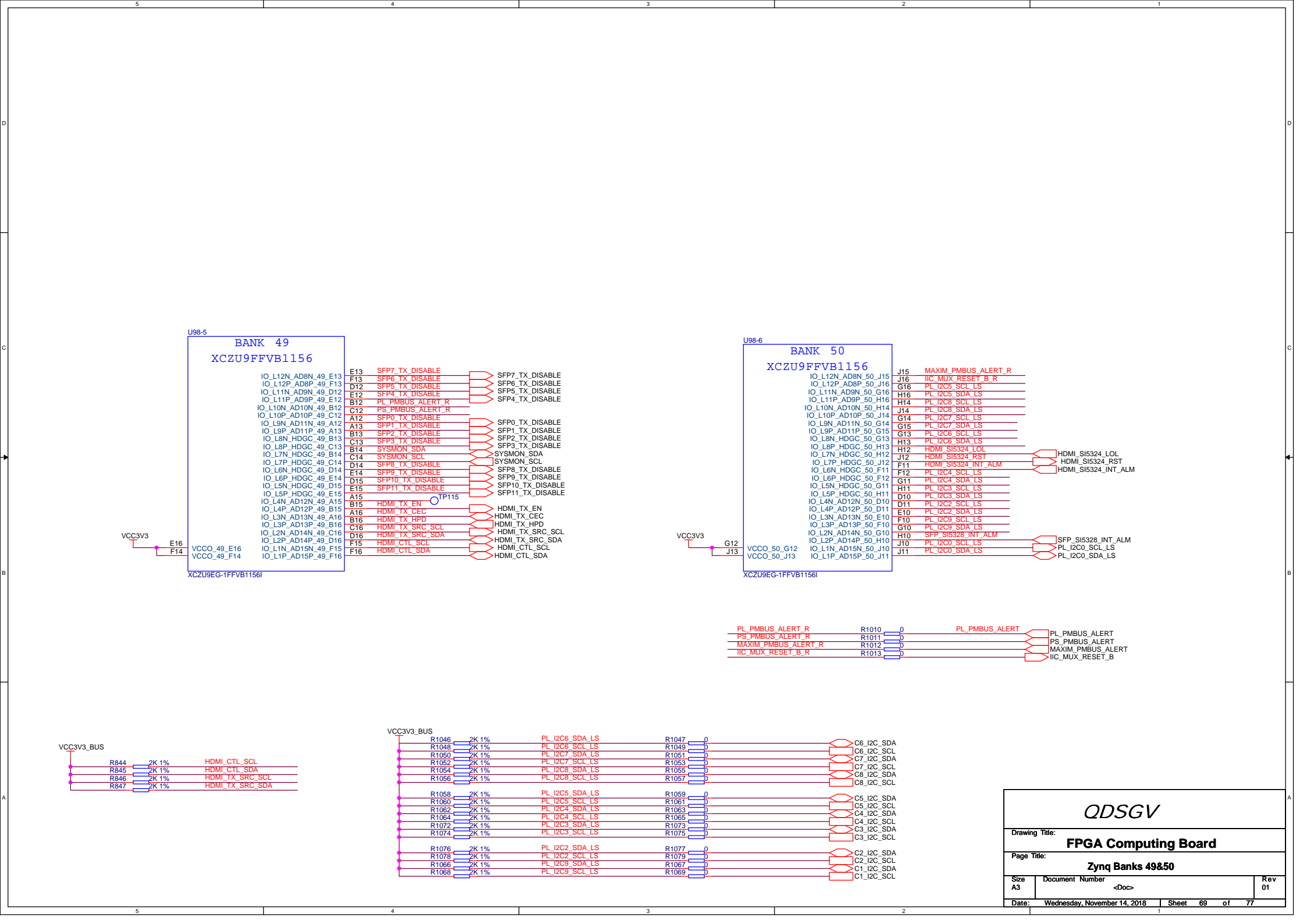


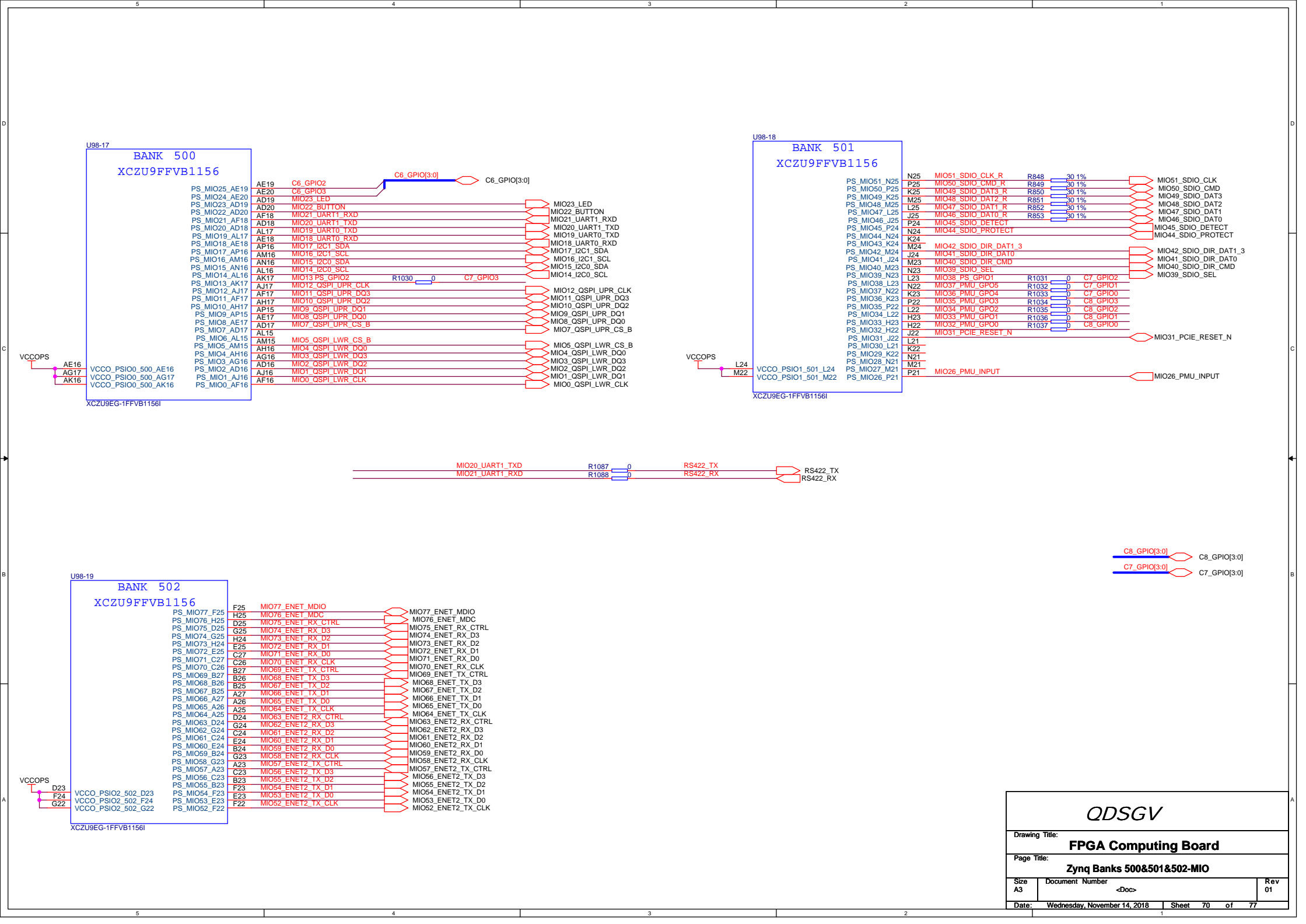


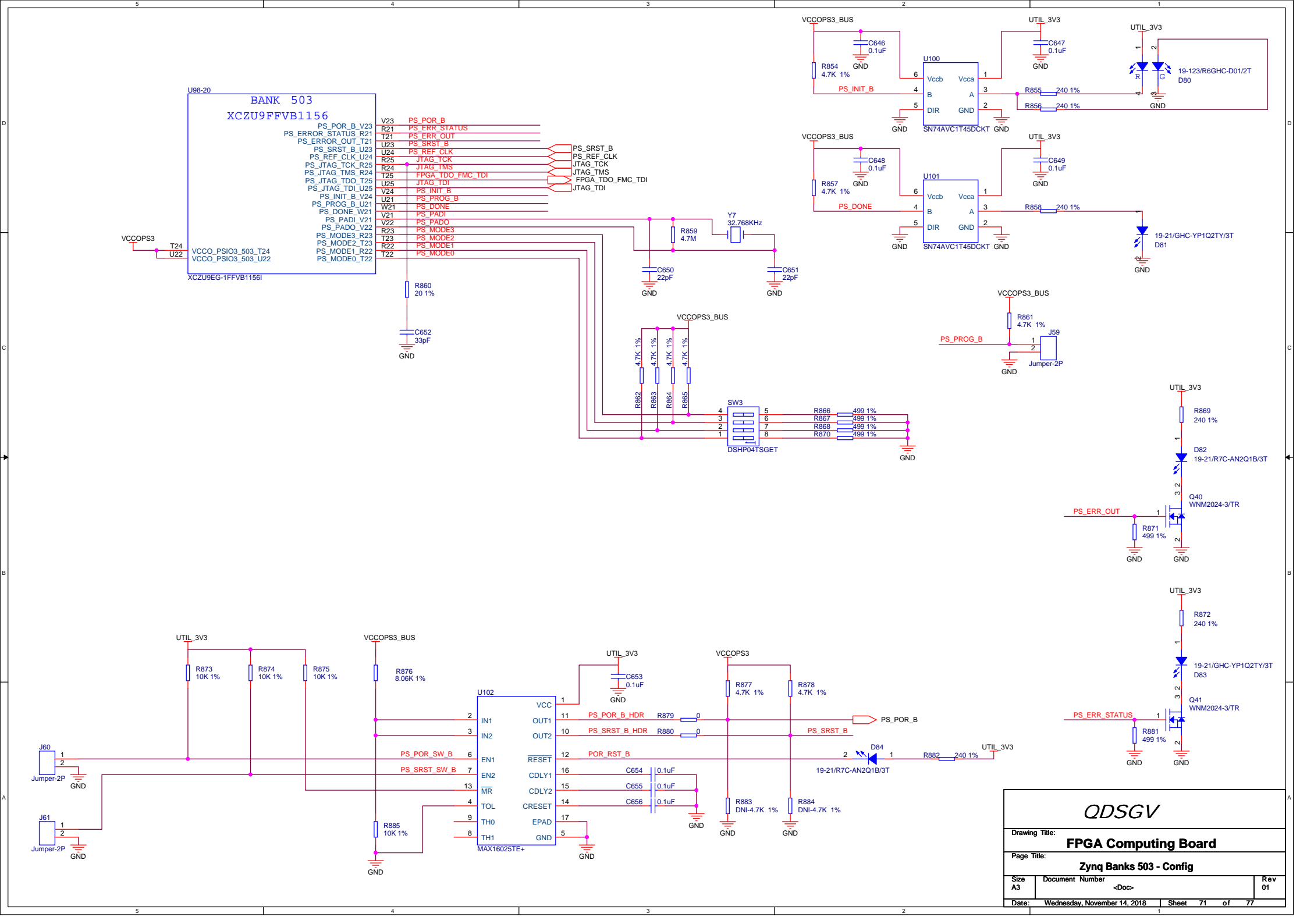
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Drawing Title:			
FPGA Computing Board			
Page Title:			
Zynq Banks 47&48			
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U98-22

**BANK 505**  
**XCZU9FFVB1156**

PS\_MGTRTXP0\_505\_AB29  
PS\_MGTRTXN0\_505\_AB30  
PS\_MGTRRXN0\_505\_AB33  
PS\_MGTRRXN0\_505\_AB34  
PS\_MGTRTXP1\_505\_Y29  
PS\_MGTRTXN1\_505\_Y30  
PS\_MGTRRXN1\_505\_AA31  
PS\_MGTRRXN1\_505\_AA32  
PS\_MGTRTXP2\_505\_W31  
PS\_MGTRTXN2\_505\_W32  
PS\_MGTRRXN2\_505\_Y33  
PS\_MGTRRXN2\_505\_Y34  
PS\_MGTRTXN3\_505\_V29  
PS\_MGTRTXN3\_505\_V30  
PS\_MGTRRXN3\_505\_V33  
PS\_MGTRRXN3\_505\_V34  
PS\_MGTREFCLK0P\_505\_AA27  
PS\_MGTREFCLK0N\_505\_AA28  
PS\_MGTREFCLK1P\_505\_W27  
PS\_MGTREFCLK1N\_505\_W28  
PS\_MGTREFCLK2P\_505\_U27  
PS\_MGTREFCLK2N\_505\_U28  
PS\_MGTREFCLK3P\_505\_U31  
PS\_MGTREFCLK3N\_505\_U32  
PS\_MGTREF\_505\_AB28

XCZU9EG-1FFVB1156I

AB29	GTR_LANE0_TX_P					GTR_LANE0_TX_P
AB30	GTR_LANE0_TX_N					GTR_LANE0_TX_N
AB33	GTR_LANE0_RX_P					GTR_LANE0_RX_P
AB34	GTR_LANE0_RX_N					GTR_LANE0_RX_N
Y29	GTR_LANE1_TX_P					GTR_LANE1_TX_P
Y30	GTR_LANE1_TX_N					GTR_LANE1_TX_N
AA31	GTR_LANE1_RX_P					GTR_LANE1_RX_P
AA32	GTR_LANE1_RX_N					GTR_LANE1_RX_N
W31	GTR_LANE2_TX_P					GTR_LANE2_TX_P
W32	GTR_LANE2_TX_N					GTR_LANE2_TX_N
Y33	GTR_LANE2_RX_P					GTR_LANE2_RX_P
Y34	GTR_LANE2_RX_N					GTR_LANE2_RX_N
V29	GTR_LANE3_TX_P					GTR_LANE3_TX_P
V30	GTR_LANE3_TX_N					GTR_LANE3_TX_N
V33	GTR_LANE3_RX_P					GTR_LANE3_RX_P
V34	GTR_LANE3_RX_N					GTR_LANE3_RX_N
AA27	GTR_REF_CLK_PCIE_C_P	C657	0.01UF			GTR_REF_CLK_PCIE_P
AA28	GTR_REF_CLK_PCIE_C_N	C658	0.01UF			GTR_REF_CLK_PCIE_N
W27	PCIE_SL_REF_CLK_C_P			C659	0.01UF	PCIE_SL_REF_CLK_P
W28	PCIE_SL_REF_CLK_C_N	C660	0.01UF			PCIE_SL_REF_CLK_N
U27	GTR_REF_CLK_USB3_C_P					
U28	GTR_REF_CLK_USB3_C_N					
U31	GTR_REF_CLK_DP_C_P					
U32	GTR_REF_CLK_DP_C_N					
AB28						

R886  
500 0.1%  
GND

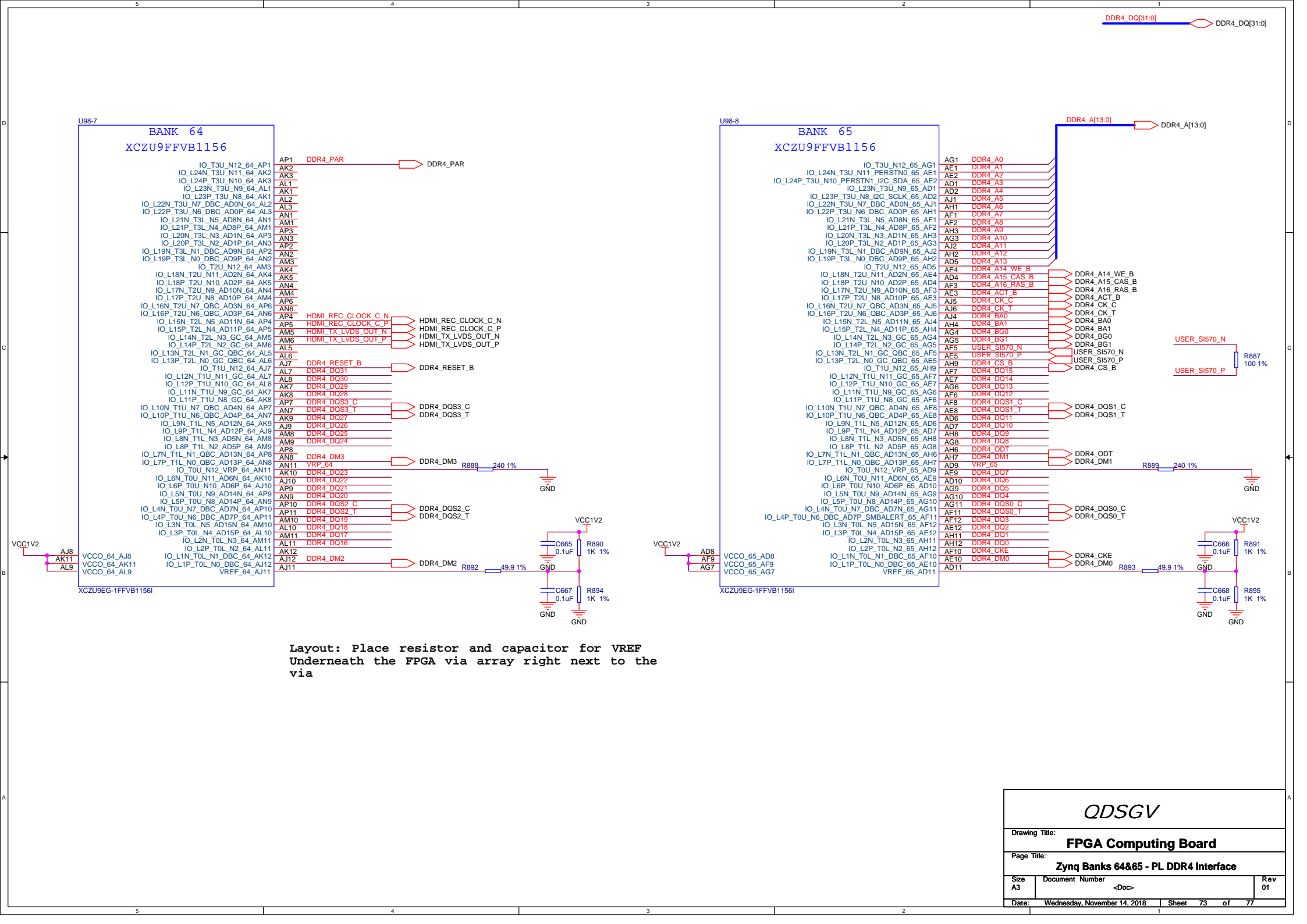
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Page Title:  
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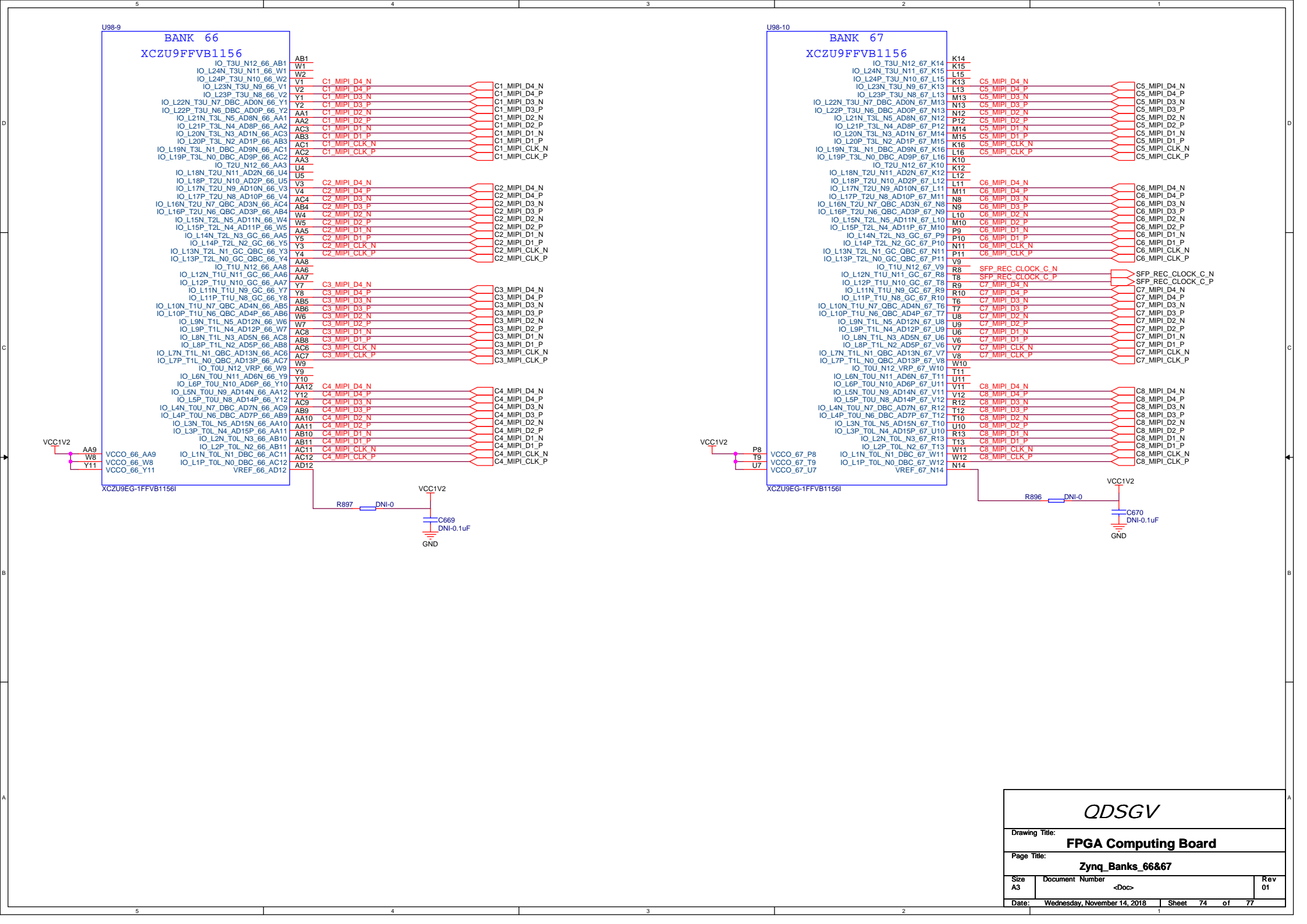
Size A3	Document Number <Doc>	Rev 01
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Layout: Place resistor and capacitor for VREF  
Underneath the FPGA via array right next to the  
via

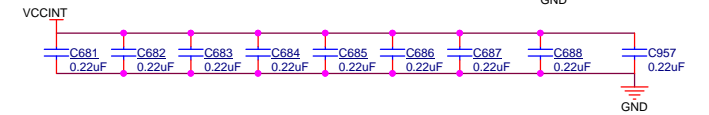
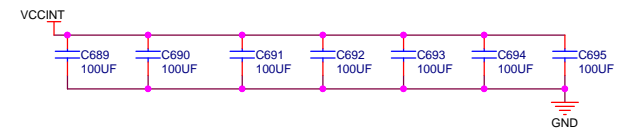
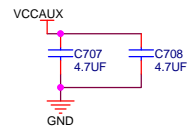
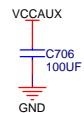
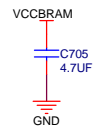
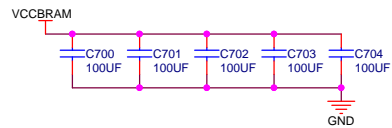
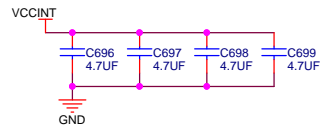
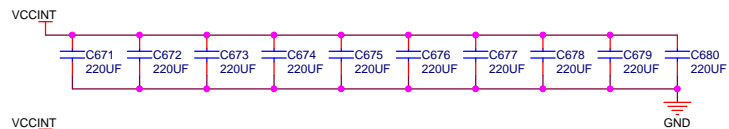
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Size A3	Document Number  -<Doc>-	Rev 01	
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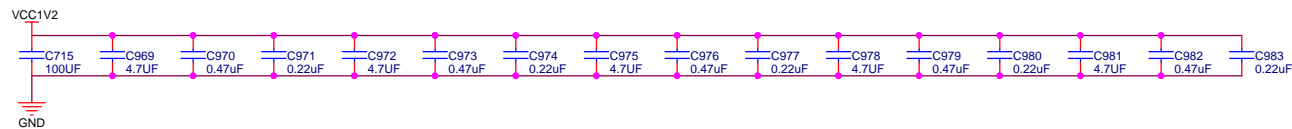
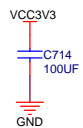
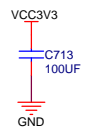
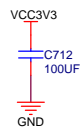
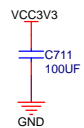
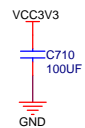
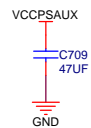
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Page Title: **Zynq\_Banks\_66&67**

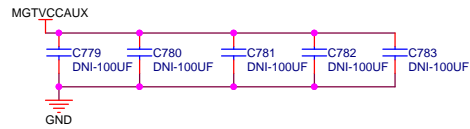
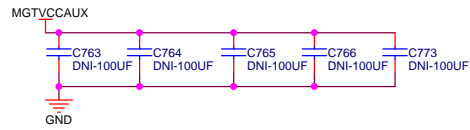
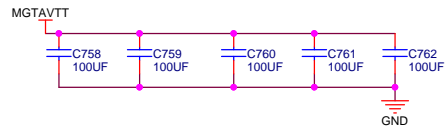
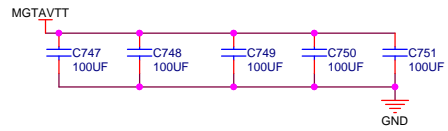
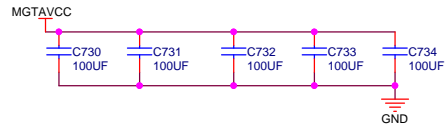
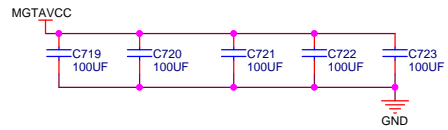
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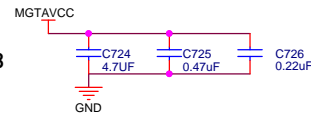
VCCO BANKS 0 44 47 48 49 50 64 65 66 67



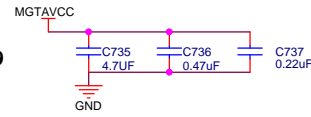
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Size A3	Document Number <Doc>		Rev 01
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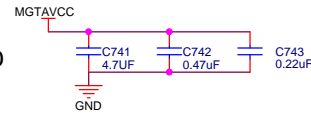
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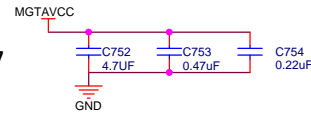
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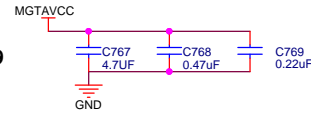
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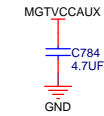
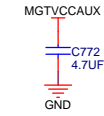
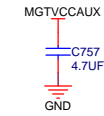
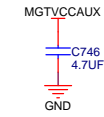
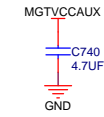
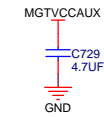
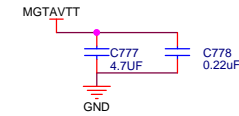
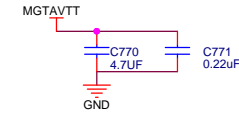
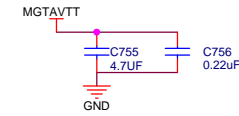
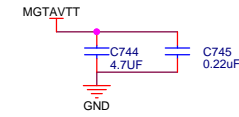
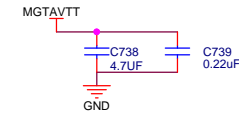
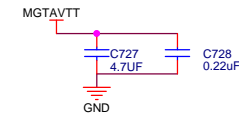
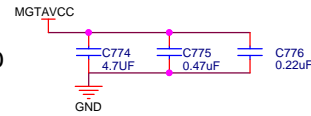
**BANK 227**



**BANK 229**

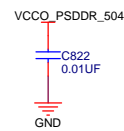
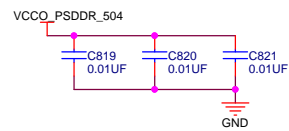
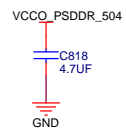
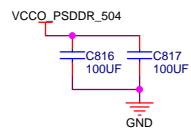
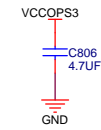
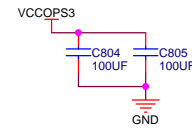
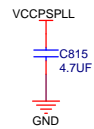
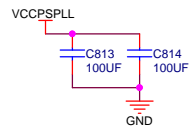
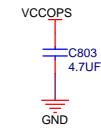
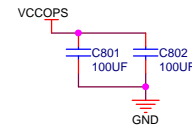
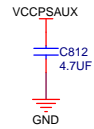
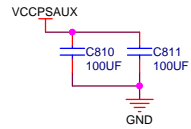
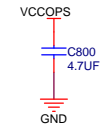
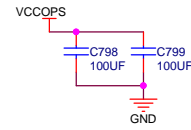
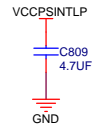
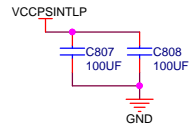
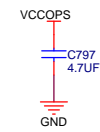
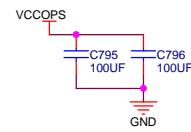
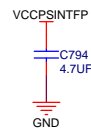
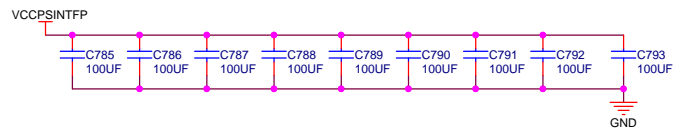


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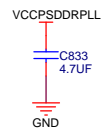
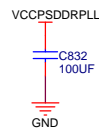
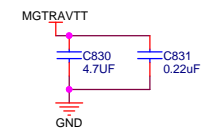
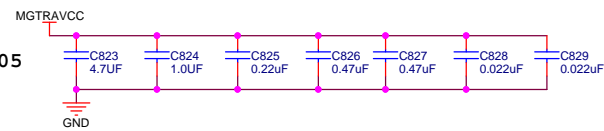


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