PIC16(L)F18325/18345

PIC16(L)F18325/18345 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F18325/18345 family devices that you have received conform functionally to the current Device Data Sheet (DS40001795**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F18325/18345 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F18325/18345 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A4
PIC16F18325	303Eh	2004h
PIC16LF18325	3040h	2004h
PIC16F18345	303Fh	2004h
PIC16LF18345	3041h	2004h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F183XX Memory Programming Specification"* (DS40001738) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A4
Oscillators	Fail-Safe Clock Monitor (FSCM)	1.1	The FSCM may fail to trigger.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Oscillators

1.1 Fail-Safe Clock Monitor (FSCM)

The Fail-Safe Clock Monitor may fail to trigger with the loss of the external clock signal when the 4x PLL is enabled. This includes all external clock modes, LP, XT, HS, ECL, ECM and ECH.

Work around

None.

Affected Silicon Revisions

A4							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001795**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: CCP

In **Section 28.3**, a note box will be added as follows:

Note:	When the CCP is configured in Compare mode using the 'toggle output on match' setting (CCPxMODE<3:0> bits = 0010) and the reference timer is set for an input clock prescale other than 1:1, the output of the CCP will toggle multiple times until finally settling a '0' logic level. To avoid this, the timer input clock prescale select bits must be set to a 1:1 ratio (TxCKPS = 00).

2. Module: Oscillators

In **Section 6.5**, the HFINTOSC Frequency Selection Register (OSCFRQ) will be modified as follows:

REGISTER 6-6: OSCFRQ: HFINTOSC FREQUENCY SELECTION REGISTER

U-0	U-0	U-0	U-0	**R/W-0/0**	R/W-q/q	R/W-q/q	R/W-q/q
—	—	—	—	**Reserved**	HFFRQ<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-**4** Unimplemented: Read as '0'.

bit 3 **Reserved. Bit must be maintained as '0'.**

bit 2-0 HFFRQ<2:0>: HFINTOSC Frequency Selection bits**(1)**

HFFRQ<2:0>	Nominal Freq. (MHz) (NOSC = 110)	2xPLL Freq. (MHz) (NOSC = 000)
000	1	N/A
001	2	
010	Reserved	
011	4	
100	8	16
101	12	24
110	16	32
111	Reserved	Reserved

Note 1: When RSTOSC = 110 (HFINTOSC 1 MHz), the HFFRQ bits will default to '011' upon Reset; when RSTOSC = 000 (HFINTOSC 32 MHz), the HFFRQ bits will default to '110' upon Reset.

3. Module: Resets

In **Section 5.12**, bit 6 of the Brown-out Reset Control Register (BORCON) will be modified as follows:

REGISTER 5-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	R/W-0/0	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN(1)	Reserved	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 SBOREN: Software Brown-out Reset Enable bit(1)
If BOREN <1:0> in Configuration Words ≠ 01:
SBOREN is read/write, but has no effect on the BOR.
If BOREN <1:0> in Configuration Words = 01:
1 = BOR Enabled
0 = BOR Disabled

bit 6 Reserved. Bit must be maintained as '0'.

bit 5-1 Unimplemented: Read as '0'.

bit 0 BORRDY: Brown-out Reset Circuit Ready Status bit
1 = The Brown-out Reset circuit is active
0 = The Brown-out Reset circuit is inactive

Note 1: BOREN<1:0> bits are located in Configuration Words.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (09/2015)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

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