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## OSI 502 Replica Build Notes

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*Author:* John Newcombe

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# 1

## Introduction

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This document describes the build, configuration and calibration of the OSI 502 board, in particular for standalone use with a serial terminal or terminal emulation software.

The 502 board was designed specifically for cassette-based systems and supports OSI ROM Basic. It has five ROM sockets, four for BASIC and one for a 2K monitor ROM that maps 256-byte segments into the memory space via a priority encoder. It uses 2114 RAM chips and can support 8K on board. A 300-baud cassette interface is included using an ACIA and associated analog circuitry. The same ACIA can be used for the on board serial interface. The C2-4P used this board.

### Acknowledgements

This document was created as a series of notes made during the build of a board and is not meant to be definitive. Most of the information was gathered from the OSIWeb forum and from dealing with issues during the build.

Thanks go to members of the OSIWeb Forum, <https://osiweb.org/osiforum/index.php> and Jeff Ferguson for his build guide [https://github.com/osiweb/Hardware/raw/master/repro/OSI\\_502/502\\_Assembly\\_Instructions\\_and\\_Log.pdf](https://github.com/osiweb/Hardware/raw/master/repro/OSI_502/502_Assembly_Instructions_and_Log.pdf).



# 2

## Construction

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### 2.1 Component List

C1	68pf
C2,C3,C6	0.01uf
C4,C8	82pf
C5	150pf
C7	22nf
C9,C20-26,C28-38, C40-45	0.1uf
C10	0.001uf
C27	??
C39	47uf 16V
D1-D5	1N914
Q1-Q3	2N3906 pnp
Q4-Q6	2N3904 npn
R1,R14,R16,R74,R76	1K
R2,R4,R10,R12,R26, R52,R54,R55,R57, R58,R60,R61,R63, R65	10K
R3	100K
R5-R9,R15,R18-R25,R62, R64,R66	4K7
R11,R13,R75	10K POT
R17	5K POT
R27	100
R28-R45,R53, R56,R59,R67	470R
R46,R48,R50,R69, R71,R73	220R
R47,R49,R51,R68,R70, R72	390R (see note below)

R77-R84	???
U1	7476
U2	CA3130
U3	6850
U4	6502
U5-U9	2716/28C16
U10 , U19	8T26
U11	74LS123
U12 , U17 , U20 , U28 , U31	74LS04 (see 2716 mods below)
U13	NE555
U14	74LS148
U15 (Empty Socket)	
U16	74LS139
U18	74LS30
U21 (Empty Socket)	
U22	74123
U23	7474
U24 , U25 , U32 , U41	74LS17
U26	74LS138
U27	74LS10
U29	74LS20
U30	74LS14
U33-U40	2114

The following Components are not needed if the RS232 is not required, see (*Adding the RS232 Interface*).

D3-D5
Q1-Q6
R46-R66
U20
U30

The 502 CPU has an internal clock oscillator but often derives its clock externally such as from the 540 video card via the bus. This is selected by link W1. The following components are not needed if an external, clock is to be used.

C4
C8

R10-13  
U11

## 2.2 Modifications

### 2.2.1 Board Modifications

The modifications described here required are required to get the board to function correctly.

- Cut trace from U22-6 to R75 center pin and install a jumper from R75 center pin to C9.
- Install Jumper between the two square holes near R26.
- Fix missing trace on U16 pin 14. It connects to neighbouring trace on top of PCB.

### 2.2.2 Using 2716 EPROMS

The modifications described here are to allow the board to support 2716 EPROMS or 28C16 EEPROMS.

- Cut trace between U6-18 and U6-21 (component side).
- Connect U6-18 to U5-18 on (solder side).
- Above U7, cut bridge at W4 topside and connect center of W4 to other position (ground).
- Above U9: cut bridge at W8a (there should be no link on W8a, see below).
- Above U9, connect U9-18 to U8-18 (solder side).
- Below U8, W5 would normally be moved from its default position to the alternative position. However, if U17 is removed as described below, this is not strictly necessary.
- U17 (74LS04) is no longer required and can be removed and replaced by linking pin 3-4, pin 5-6, pin 8-9, pin 10-11 and pin 12-13.

W8 is in fact two links, W8a and W8b. Whilst viewing the board with the 48 way bus connector on the right, W8a is the link on the left with W8b being the one on the right.

It is worth noting that some EPROMS have been found not to work in the 502 board. For example, whilst many ***SGS M2716 F1*** devices seem to work fine, that is not always the case for the ***SGS M271 F1 Fast*** devices.

### 2.2.3 Adding the RS232 Interface

The 502 card supports either a cassette interface or a serial interface. In addition, the serial interface can be configured to be TTL levels or RS232 levels.

Fitting resistors R46-R51 and R68-R73 provide a TTL serial I/O at J3 in addition to the cassette interface at J2.

The cassette and the serial interfaces share the same ACIA and in theory can be used simultaneously. However, in practice this can be problematic. When configuring the system for serial use it may be prudent to isolate the cassette interface. This can most easily be done by removing U23 and U1.

To make the serial interface compatible with an RS232 serial device, the following components need to be fitted.

D3-D5  
Q1-Q6  
R46-R66  
U20  
U30

Note the orientation of the transistors as the through holes on the circuit board are positioned the opposite way round for transistors typically supplied in the TO92 package.

In addition R46-R51 and R68-R73 should not be present and the links adjacent to U30 and U41 should be cut. See **Fig. 2.1** and **Fig. 2.2** for details.

When configuring the system for RS232 compatibility it would be prudent to isolate the cassette interface. This can most easily be done by removing U23 and U1.

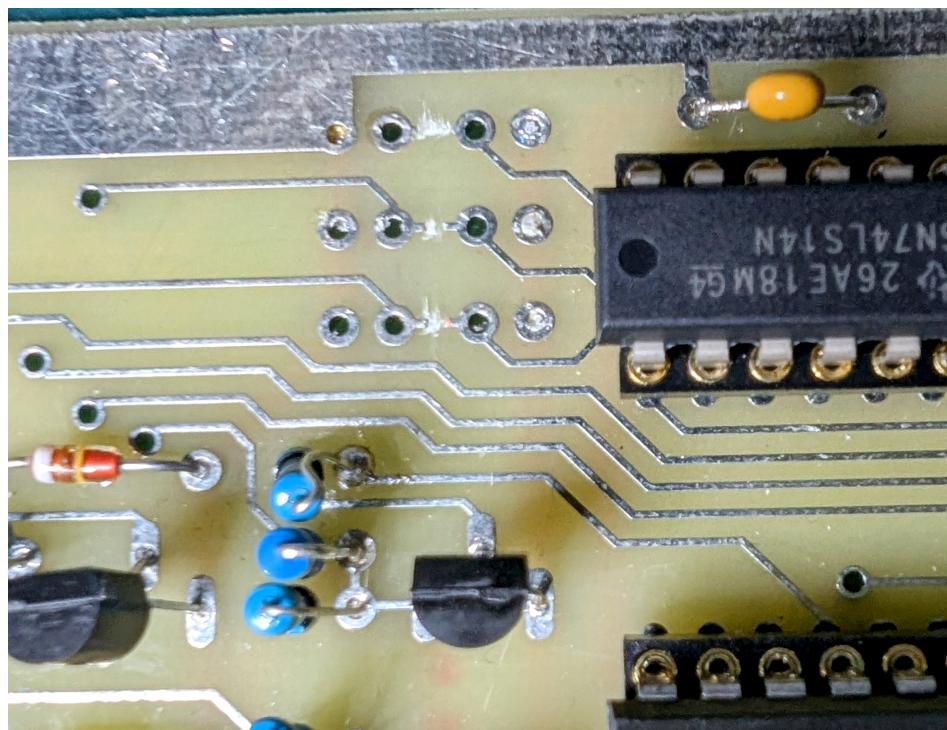


Figure 2.1: Links to be cut just next to U30 on component side.

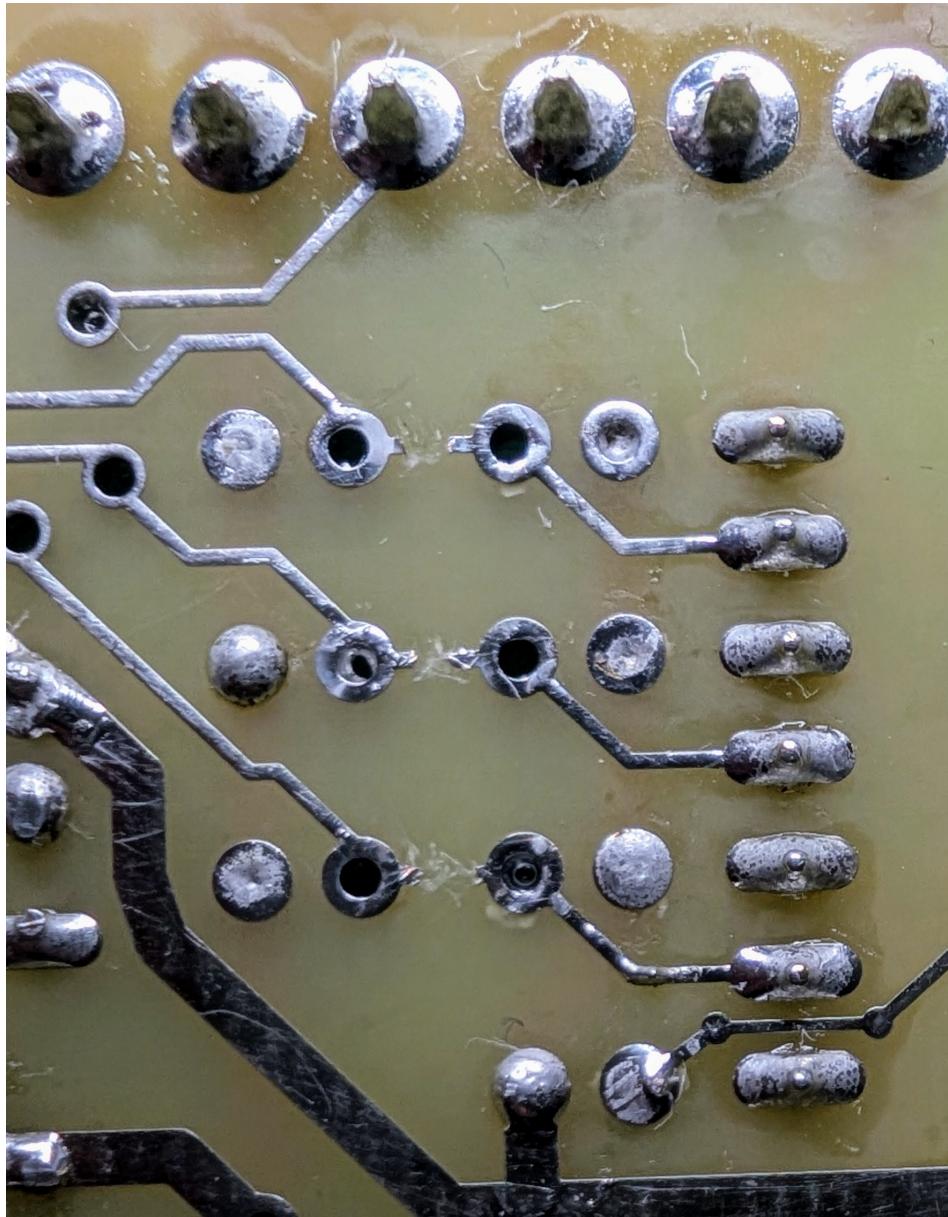


Figure 2.2: Links to be cut just next to U41 on solder side.

The serial interface typically runs at 300 baud with 8 data bits, no parity and 2 stop bits.

Link W3 (see schematic) connects an input presented to J3 pin 7, to be connected to either CTS or DCD on the ACIA if required. With the link in the default position, DCD and CTS inputs to the ACIA are held active (low).

Link W2 connects the transmit clock output to the receive clock input providing a simple method of setting the receive clock to match the transmit clock. The default position of the link makes this connection.

## 2.3 Monitor Mapping

### 2.3.1 Overview

The OSI Monitor ROMs often contain monitor programs for a multitude of machine configurations. Socket U15 on the 502 board allows specific parts of the monitor ROM to be selected as required.

For example a 502 serial system might use the 65A monitor code loaded at FE00 i.e. page 6 of the ROM, and the 65AB Basic Boot code at FF00 i.e page 7 of the ROM. Alternatively a system without ROM basic might simply use the 65A monitor located at FF00 (page 7). Each of these options can be configured using the links at U15.

### 2.3.2 Decoding

The upper address pages (FDxx, FExx, FCxx) are decoded into separate signals, which are then directed to a 8 line priority encoder (U14). The output of U14 provides the three addresses lines to the ROM. The signals are jumpered to map a particular memory page to a particular ROM page address using the U15 link area.

The output of U14 is inverted, meaning that an input to U14 of '00000000' produces an output of '111'. The outputs are fed as address lines to the monitor ROM. See **Fig. 2.3** for details.

Therefore, to map FE00 to page 6 of the ROM and FF00 to page 7 of the ROM, jumpers would be placed on U15 pin 3 to pin 7 and U15 pin 2 to pin 8 (see below).

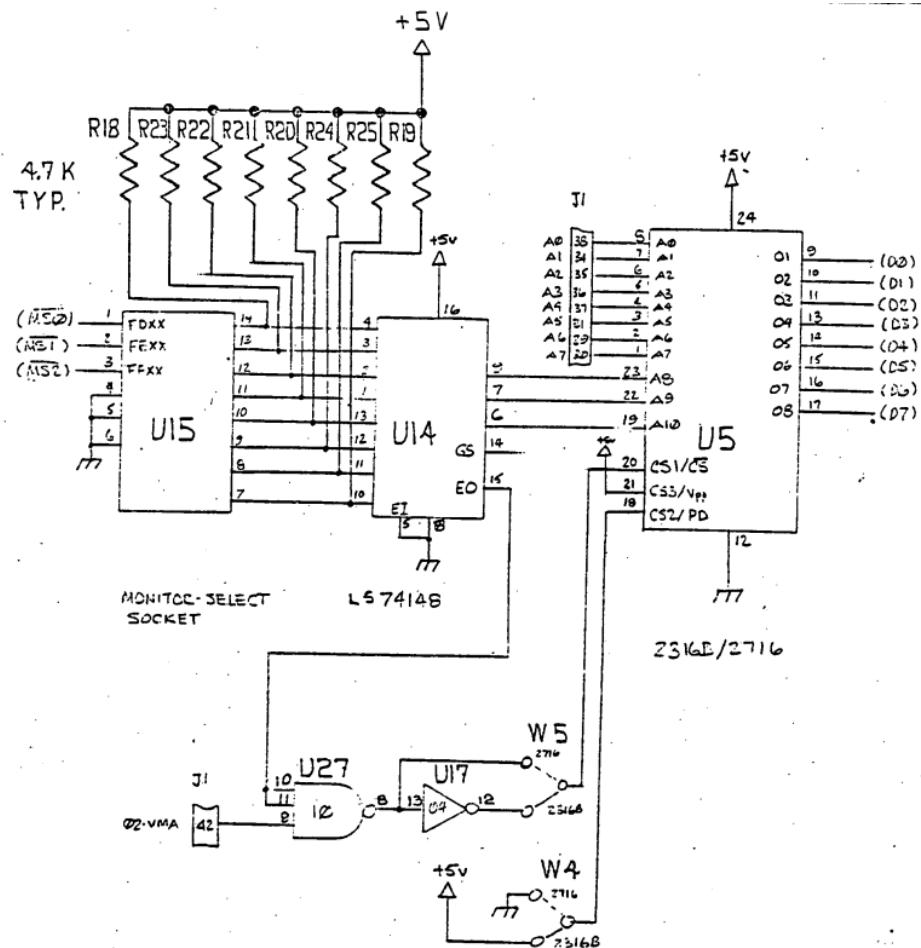


Figure 2.3: OSI 502 Priority Decoder.

### U15 Pinout

```

1 = FDxx selected
2 = FExx selected
3 = FFxx selected
4 = Gnd
5 = Gnd
6 = Gnd
7 = ROM select page 7
8 = ROM select page 6
9 = ROM select page 5
10 = ROM select page 4
11 = ROM select page 3
12 = ROM select page 2
13 = ROM select page 1
14 = ROM select page 0

```

#### 2.3.3 SYNMON page layout

Page 0 FE00 OSI 440 board 65V monitor (ASCII KB).  
 Page 1 FF00 OSI 440 board C/W/M BASIC boot (ASCII KB).  
 Page 2 \*FD00 C2/540 Polled Keyboard routine.  
 Page 3 \*FE00 C2/540 65V Monitor.  
 Page 4 \*FF00 C2/540 BASIC Boot (C/W/M?).  
 Page 5 FD00 initializes HDisk controller (CD74/CD36 winchester HD).  
 Page 6 FE00/FF00 OSI 65A Serial Monitor.  
 Page 7 \*FF00 C2/540 disk boot (H/D/M?) works with serial or video.

#### 2.3.4 SYN600 - page layout

page 000 'H/D/M' maps to \$FF00 for a C2/C4 540Vid disk system.  
 page 100 keypoller maps to \$FD00 for a C2/C4 540Vid system.  
 page 200 monitor maps to \$FE00 for a C2/C4 540Vid system.  
 page 300 'C/W/M' maps to \$FF00 for a C2/C4 540Vid tape system.  
 page 400 disk boot maps to \$FC00 for a C1 system.  
 page 500 keypoller maps to \$FD00 for a C1 system.  
 page 600 monitor maps to \$FE00 for a C1 system.  
 page 700 'D/C/W/M' maps to \$FF00 for a C1 system.

**2.3.5 65A-65AB Serial System - page layout**

This card, with the standard addressing scheme would have access to three pages only.

Page 5 Free  
Page 6 FE00/FF00 OSI 65A Serial Monitor.  
Page 7 FF00 Basic boot (C/W/M?).

Based on the above, a typical U15 link arrangement for the 502 board would be.

Pin 3 to Pin 7 (FF00)  
Pin 2 to Pin 8 (FE00)  
Pin 1 to Pin 9 (FD00)

# 3

## Calibration

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### 3.1 R17 TX Clock

With the input of the scope connected to U13, pin 3, adjust R17 for a full cycle width of 210uSec. See **Fig. 3.1**.

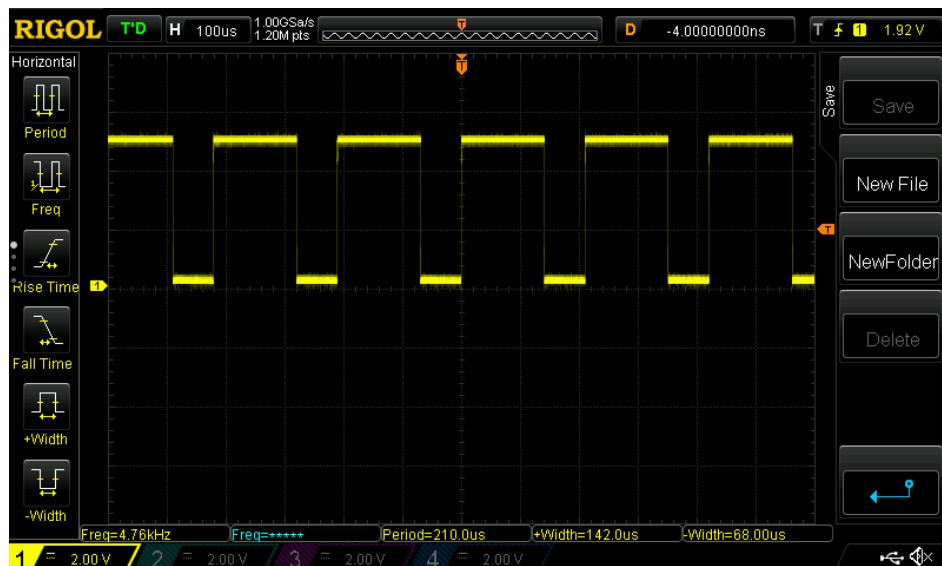


Figure 3.1: Adjusting R17.

### 3.2 Tape Pulse Duration

Connect a jumper between Pins 10 and 11 of J2, Cold start Basic and enter...

```
10 Print "U"  
20 GOTO 10  
SAVE  
RUN
```

With the input of scope connected to pin 5 of U22, adjust R75 for a positive pulse width of at least 500uSec, but not more than 640uSec. Disconnect the jumper.

### **3.3 Memory IC Allocation**

The minimum amount of memory that can be used to start the 502 as a standalone machine at the monitor is 1K (0000–3FFF). The following list shows how each pair of memory chips are addressed.

U40-U49	0000-03FF
U39-U48	0400-07FF
U38-U47	0800-0BFF
U37-U46	0C00-0FFF
U36-U45	1000-13FF
U35-U44	1400-17FF
U34-U43	1800-1BFF
U33-U42	1C00-1FFF

# 4

## Interfaces

### 4.1 Connectors

See Fig. 4.1 for details.

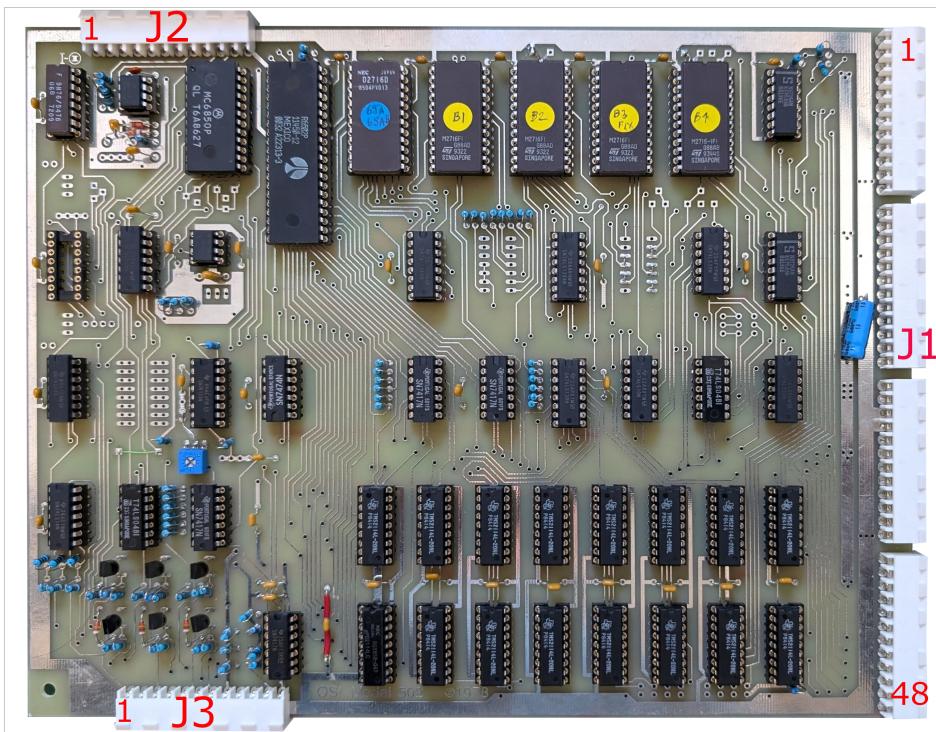


Figure 4.1: Connectors.

#### 4.1.1 Power

Power is connected via Connector J1 (Backplane Connector).

J1 pin 24 -9V (is this used ???)

J1 pin 25/26 +5V  
J1 pin 27/28 Gnd

The specification calls for +5v and -9v, however, -9v is only required for the RS232 serial port (TXD, TXCLK and RTS). Not supplying -9v and connecting the -9v rail to ground replicates the circuit used in later machines such as the Superboard II and Compukit UK101. The simplest way to achieve this is to replace C38 with a wire link. See **Fig. 4.2.**

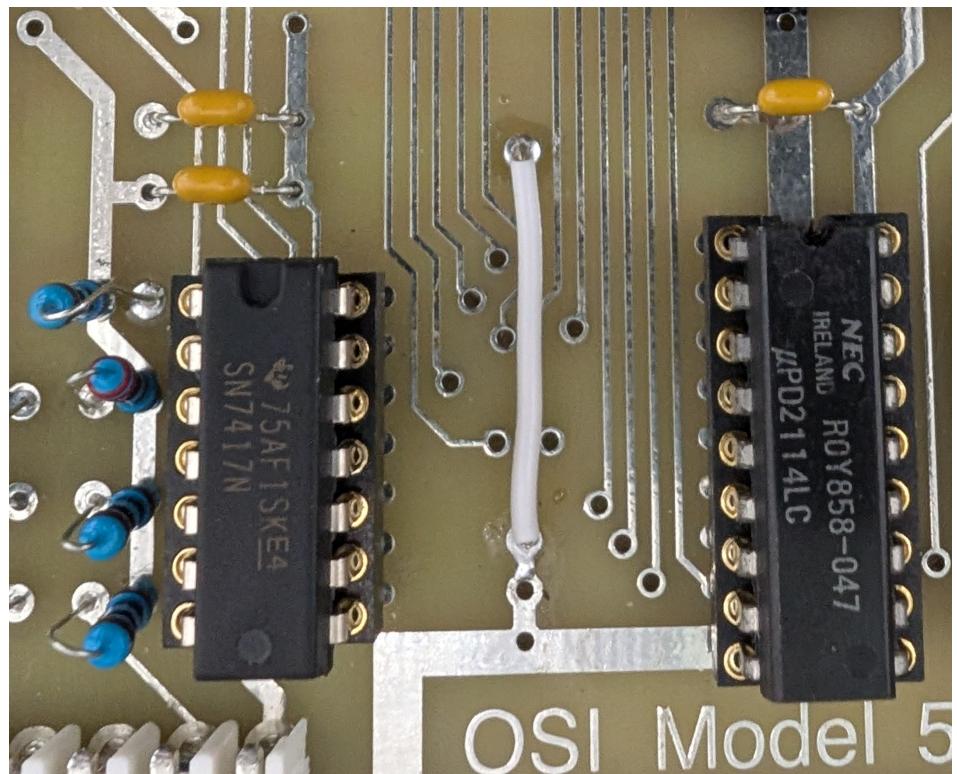


Figure 4.2: C38 replaced by a wire link.

#### 4.1.2 Cassette Interface

The Cassette Interface is available via connector J2 (with the backplane connector on the right, J2 is on the top).

J2 pin 3 Reset

```
J2 pin 8 cassette mic (output)
J2 pin 9 Gnd
J2 pin 11 cassette out (input)
```

#### 4.1.3 Serial Terminal

The serial terminal interface (RS232) is available via J3 (with the backplane connector on the right, J3 is on the bottom).

```
J3 pin 1 RXD
J3 pin 3 Receive Clock
J3 pin 5 ACIA SP.I (see below)
J3 pin 7 TXD
J3 pin 9 Transmit Clock
J3 pin 11 RTS
```

Pin 5 of J3 is an input that can be configured via W3 to connect to the ACIA CTS or DCD inputs.



# Notes:

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