

OSI 502 Replica Build Notes

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Introduction

This document describes the build, configuration and calibration of the OSI 502 board for standalone use with a serial terminal or terminal software.

This board was designed specifically for cassette-based systems. It has five ROM sockets, four for BASIC and one for a 2K monitor ROM that maps 256-byte segments into the memory space via a priority encoder. It uses 2114 RAM chips and can support 8K on board. A 300-baud cassette interface was included using an ACIA and associated analog circuitry was integrated. The C2-4P used this board. The same ACIA can be used for the on board RS232 interface.

The 502 CPU has an internal oscillator but often derives its clock from the 540 video card via the bus. This is selected by link W1.

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Construction

2.1 Component List

C1	68pf
C2,C3,C6	0.01uf
C4,C8	82pf
C5	150pf
C7	22nf
C9,C20-26,C28-38, C40-45	0.1uf
C10	0.001uf
C27	??
C39	47uf 16V
D1-D5	1N914
Q1-Q3	2N3906 pnp
Q4-Q6	2N3904 npn
R1,R14,R16,R74,R76	1K
R2,R4,R10,R12,R26, R52,R54,R55,R57, R58,R60,R61,R63, R65	10K
R3	100K
R5-R9,R15,R18-R25,R62, R64,R66	4K7
R11,R13,R75	10K POT
R17	5K POT
R27	100
R28-R45,R53, R56,R59,R67	470R
R46,R48,R50,R69, R71,R73	220R
R47,R49,R51,R68,R70, R72	390R (see note below)

R77-R84	???
U1	7476
U2	CA3130
U3	6850
U4	6502
U5-U9	2716/28C16
U10 , U19	8T26
U11	74LS123
U12 , U17 , U20 , U28 , U31	74LS04 (see 2716 mods below)
U13	NE555
U14	74LS148
U15 (Empty Socket)	
U16	74LS139
U18	74LS30
U21 (Empty Socket)	
U22	74123
U23	7474
U24 , U25 , U32 , U41	74LS17
U26	74LS138
U27	74LS10
U29	74LS20
U30	74LS14
U33-U40	2114

The following Components are not needed if the RS232 is not required (*Adding the RS232 Interface*).

D3-D5
Q1-Q6
R46-R66
U20
U30

The following components are not needed if an external, clock is to be used.

C4
C8
R10-13
U11

Set Jumper W1 for internal or external clock as required.

2.2 Modifications

2.2.1 Board Modifications

The modifications described here required are required to get the board to function correctly.

- Cut trace from U22-6 to R75 center pin
- Install jumper R75 center pin to C9
- Install Jumper in square holes near R26
- Fix missing trace on U16 pin 14. It connects to neighbouring trace on top of PCB

2.2.2 Using 2716 EPROMS

The modifications described here are to allow the board to support 2716 EPROMS or 28C16 EEPROMS.

- Cut trace between U6-18 and U6-21 topside
- Connect U6-18 to U5-18 on bottomside
- Above U7: cut bridge at W4 topside and connect center of W4 to other position i.e. ground.
- Above U9: cut bridge at W8a topside (there should be no link on W8a see below)
- Above U9: connect U9-18 to U8-18 on bottomside
- Remove U17 (74LS04)
- Add jumpers on U17 socket: pin 3–4, pin 5–6, pin 8–9, pin 10–11, pin 12–13

W8 is in fact two links, W8a and W8b. Whilst viewing the board with the 48 way bus connector on the right, W8a is the link on the left with W8b being the one on the right.

2.2.3 Adding the RS232 Interface

The 502 card supports either a cassette interface or a serial interface. In addition, the serial interface can be configured to be TTL levels or RS232 levels.

Fitting resistors R46-R51 and R68-R73 provide a TTL serial I/O at J3 in addition to the cassette interface at J2.

The cassette and the serial interfaces share the same connection to the ACIA and in theory can be used simultaneously. However, in practice this can be problematic if using a terminal as the display and keyboard.

To make the serial interface compatible with an RS232 serial device, the following components need to be fitted.

D3-D5
Q1-Q6
R46-R66
U20
U30

Note the orientation of the transistors as the through holes on the circuit board are positioned the opposite way round for transistors typically supplied in the TO92 package.

In addition R46-R51 and R68-R73 should not be present and the following links should be cut.

When configuring the system for RS232 compatibility it may be prudent to isolate the cassette interface. This can most easily be done by removing U23 and U1.

The serial interface typically runs at 300 baud with 8 data bits, no parity and 2 stop bits.

Link W3 (see schematic) connects an input presented to J3 pin 7, to be connected to either CTS or DCD on the ACIA if required.

Link W2 connects the transmit clock output to the receive clock input providing a simple method of setting the receive clock.

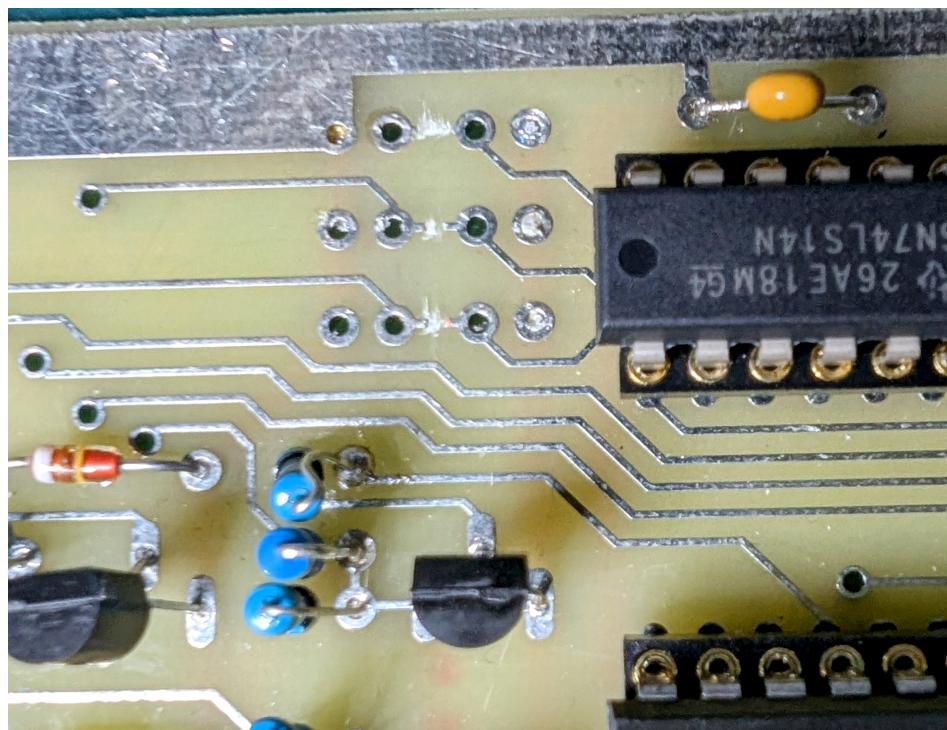


Figure 2.1: Links to be cut just next to U30 on component side.

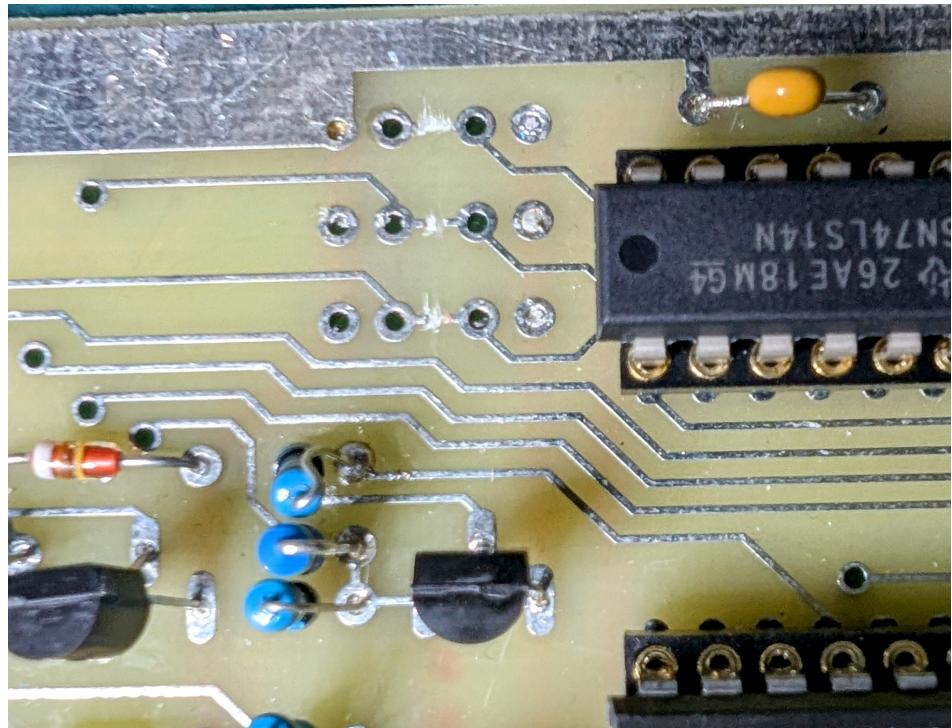


Figure 2.2: Links to be cut just next to U41 on solder side.

2.2.4 R75 Tape Pulse Duration

2.3 Configuration

Links, missing IC, 2716 etc.

2.4 Calibration

2.4.1 R17 TX Clock

Input of scope to U13, pin 3. Adjust R17 for a full cycle width of 210uSec.

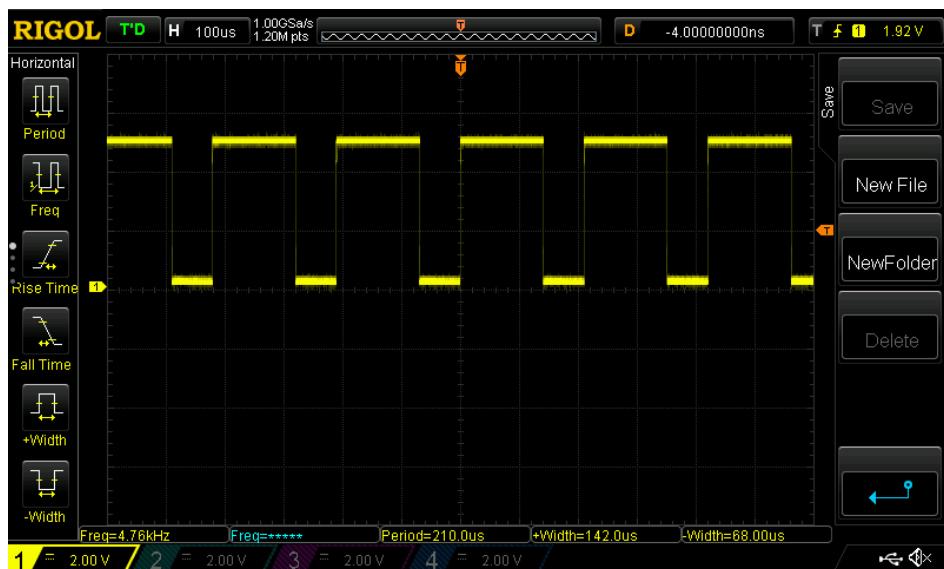


Figure 2.3: Adjusting R17.

2.4.2 R75 Tape Pulse Duration

Connect jumper between Pins 10 and 11 of J2, Cold Start Basic and enter:

```
10 Print "U"
20 GOTO 10
SAVE
RUN
```

Input of scope to pin 5 of U22. Adjust R75 for a positive pulse width of at least 500uSec. But not more than 640uSec. Disconnect the jumper.

Memory IC Allocation

U40-U49	0000-03FF
U39-U48	0400-07FF
U38-U47	0800-0BFF
U37-U46	0C00-0FFF
U36-U45	1000-13FF
U35-U44	1400-17FF
U34-U43	1800-1BFF
U33-U42	1C00-1FFF

Interfaces

3.1 Connectors

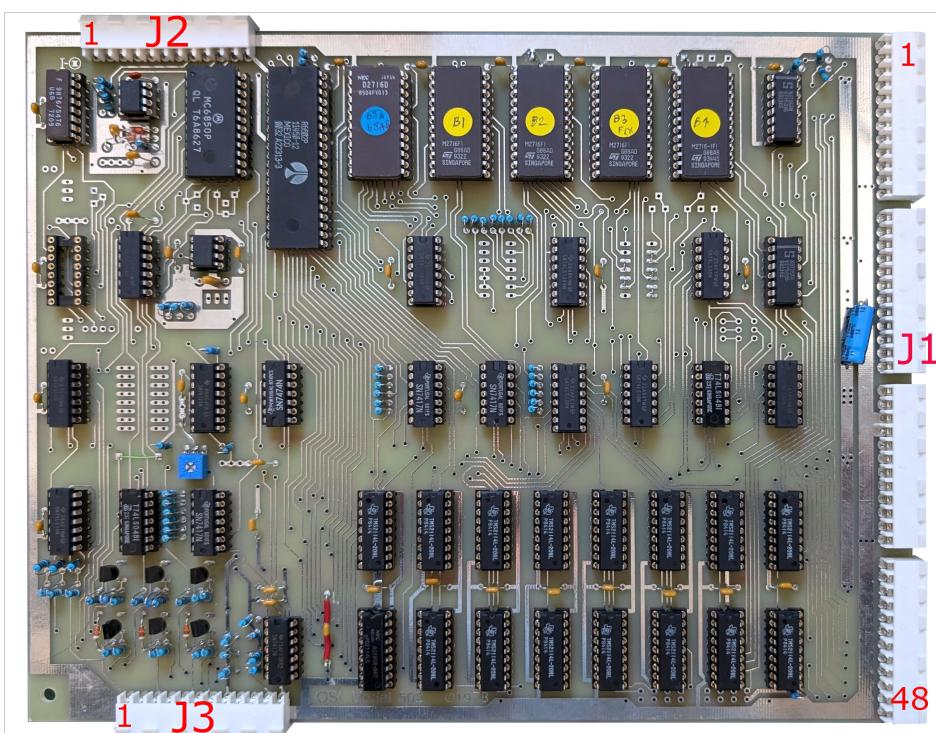


Figure 3.1: Connectors.

3.1.1 Power

Power is connected via Connector J1 (Backplane Connector).

J1 pin 24 -9V (is this used ???)
J1 pin 25/26 +5V
J1 pin 27/28 Gnd

The specification calls for +5v and -9v, however, -9v is only required for the serial port outputs (TXD, TXCLK and RTS). Connecting the -9v rail to ground replicates the circuit used in later machines such as the Superboard II and Compukit UK101. The simplest way to achieve this is to replace C38 with a wire link. See **Fig. 3.2**.

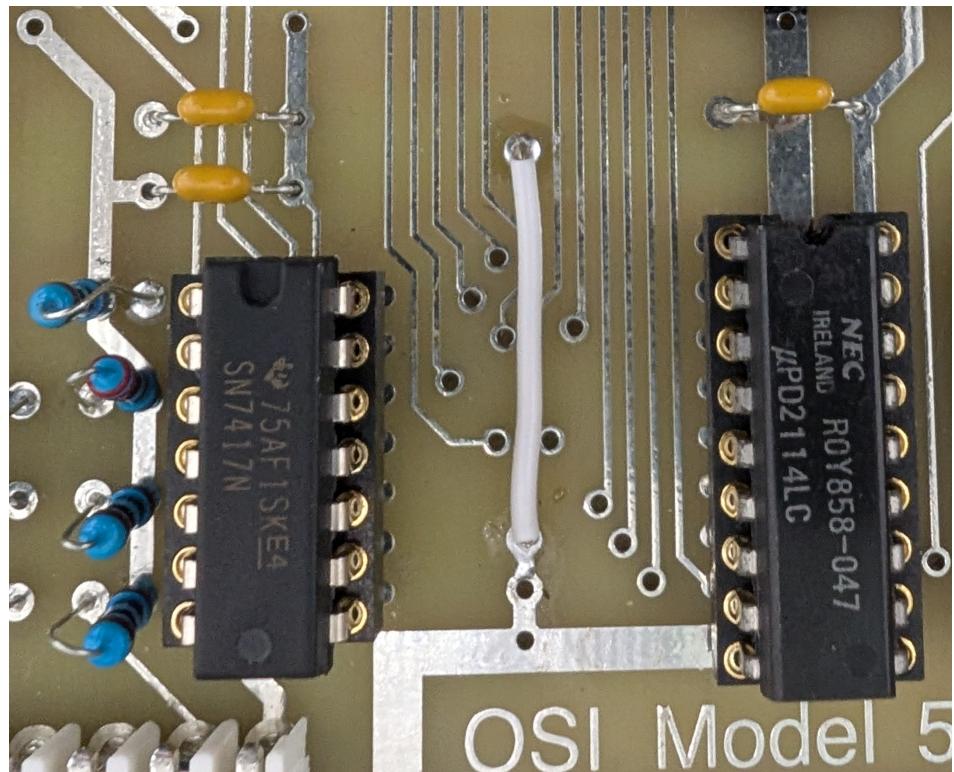


Figure 3.2: C38 replaced by a wire link.

3.1.2 Cassette Interface

The Cassette Interface is available via connector J2 (with the backplane connector on the right, J2 is on the top).

J2 pin 3 Reset
J2 pin 8 cassette mic (output)
J2 pin 9 Gnd
J2 pin 11 cassette out (input)

3.1.3 Serial Terminal

The serial terminal interface (RS232) is available via J3 (with the backplane connector on the right, J3 is on the bottom).

```
J3 pin 1 RXD  
J3 pin 3 Receive Clock  
J3 pin 5 ACIA SP.I ???  
J3 pin 7 TXD  
J3 pin 9 Transmit Clock  
J3 pin 11 RTS
```


Notes:
