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* GENERAL OPERATING INSTRUCTIONS FOR THE *
*         MAP 256K DYNAMIC RAM CARD     *
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256K DYNAMIC RAM BOARD

INTRODUCTION

The MAP 80 256K Ram board has been designed around the 80-BUS system and is therefore compatible with the NASCOM and GEMINI range of products. However due to the requirement to provide MEM EXT and to disable RAM in the lower 4k this card is not suitable for use with a NASCOM 1. The board utilises the 4864 64k dynamic ram chip arranged in four blocks of 64k bytes thus allowing the board to be supplied in four sizes i.e. 64/128/192/256k bytes.This also means that expansion of the smaller sizes is only a matter of adding additional ram chips, since decoding for the full 256k is provided even with the smallest configuration. Up to eight MAP 80 256k ram boards can used in one system giving up to 2 megabytes on line.
To facilitate the use of memory which is outside the addressing range of the Z80 processor, circuitry has been included to allow full memory mapping and flexible page mode operation thus offering the end user a wide range of options depending on how the board is configured.

COMMISSIONING

Carefully unpack your MAP 256 K RAM and examine it for any mechanical damage. In the event of any damage please inform your dealer immediatly.
Your new RAM card will have been shipped to you fully tested and working. If your system is only to have one 256K RAM card and is to be used on either a Nascom 2 or a GEMINI G811 then the card need only be plugged into the system. For other combinations read the section on link blocks.

THEORY OF OPERATION

IC46 is an 8 bit latch (74LS273) addressed at port FE, on power up or reset all bits are reset to 0. This leaves port FF for paging of existing Gemini/Nascom RAM/ROM cards, their paging system permits only 4 pages which is far too restrictive. Bits from IC46 are then further decoded by IC47 (74LS138 3 to 8 line decoder), LB1 is used to link Q1,Q2 and Q3,from IC46 directly to SA,SB and SC (Select A,B,C) on IC47, further decoding is provided by Q4 and Q5 which are linked to the EN and /EN of IC47, (either Q4 or Q5 can be inverted by linking through IN and OUT on LB1). This then provides a 5 bit decode or 2 Megabytes!!! IC47 provides 8 page selects to LB2 (P0 to P7). P0 thru P3 are linked to select RAM blocks R0 thru R3 on the first of each pair of cards, and P4 thru P7 to select R0 thru R3 on the

second .
This system provides for paging of 64k pages, with the controlling program residing in EPROM or "priority RAM" e.g Nascom 2 workspace RAM or Gemini "Bytewide sockets".

This we consider is not an efficient way to control additional RAM. Memory mapping is probably the best way but requires hardware modifications to existing equipment, we have therefore devised a scheme to page 32k blocks. Using this system either the upper or lower 32k of page 0 will remain within the main Z80 memory map at all times, and any 32k block from any 64k page can be placed in the other half. Setting the appropriate bits of IC46 selects the required paging system. BIT 7 reset (0) selects 64k paging, set (1) selects 32k paging. BIT 6 reset (0) selects the lower 32k of page 0 as permanent with other 32k blocks being paged into the upper 32k, or set (1) selects the upper 32k of page 0 as permanent with other 32k blocks being paged into the lower 32k. BITs 1 thru 4 select the required 64k page and BIT 0 selects the upper/lower 32k block from that page. If BIT 7 is reset BITs 0 and 6 have no effect. It takes a while for the full implications of this to sink in, but it is possible to control up to 1 Megabyte of RAM, using the 32k mode to transfer information and program control between 64k pages, which can be run independently of each other using the 64k mode.

In order to achieve this a few changes are made to the link blocks. When BIT 7 of IC46 is set 32k paging comes into operation, if BIT 6 is 0, whenever the Z80 calls for access to the lower 32k (addresses 0000 to 7FFF) pin F0 (Force page 0) on LB1 will go low, this is connected to EN to disable all pages of RAM (Q5 becomes redundant), The same signal is then used to enable page 0 (The F0 select on LB2 is ANDed with F0 by diverting it through IN and OUT. If BIT 6 is 1, F0 will go low when addresses 8000 to FFFF are accessed. BITs 0 and 6 are XORed ORed and ANDed as required in 32k page mode in order to invert A15 if required so that the upper 32k of a page can be paged into the lower 32k of the Z80 memory map and vice versa.

Summary of port FE bits

BIT 0 — SET: select upper 32k block
RESET: select lower 32k block
(Not operative if bit 7 is reset)

BIT 1)
BIT 2)
BIT 3) Selects 64k page (BIT 5 not used in 32k mode)
BIT 4)
BIT 5)

BIT 6 — SET: select upper 32k of page 0 as permanent
RESET: select lower 32k of page 0 as permanent
(Not operative if bit 7 is reset)

BIT 7 — SET: select 32k page mode
RESET: select 64k page mode

MEMORY MAPPING

Memory mapping is a system where a fast TTL RAM is placed in between the Z80 and the bus, this RAM decodes A12 thru A15 to provide A12 thru A19, and it is therefore possible to map any 4k block into any 4k slot in the Z80 memory map. Note ANY block into ANY slot.

In order to utilise this system the link blocks are set up to use A16 thru A19 to select which 64k page is to be used (this page will vary according to what 4k slot is being addressed by the Z80 [A12-15]. Note that A12-15 put out on to the bus may well be different to that put out by the Z80.

The Gemini G813 memory mapped CPU card provides A19 but does not put it on to the bus!!! Therefore only 512k bytes can be addressed before resorting to paging (messy). If more RAM is required when using the G813 details of modifications to provide A19 can be supplied on request. Note also that this card uses port FE to address the TTL RAM, so L2 has to be linked b to c so that paging is addressed on port FF.

COMPATABILITY WITH OTHER PRODUCTS

As mentioned above the MAP 256 K RAM card can be used with most of the existing 80 Bus/Nasbus systems. For example without modification a MAP 256K RAM card can used on a Nascom 2 whilst still retaining the existing monitor and workspace. A Gemini G811 system can also incorporate these new cards without any hardware modifications to the computer. Simply remove your existing RAM card and insert the MAP RAM 256. The Gemini/Nascom paging system uses port FF whereas our card uses port FE, this leaves port FF for the paging of, for example, EPROM cards as before. Details for incorporating existing RAM cards can be found later.

LINK BLOCKS AND STANDARD CONFIGURATIONS

All the memory patching is carried out on two link header blocks. Each header block is linked in a different way depending upon each card's position within a system and depending upon the modes used. The followins series of examples will be the most frequently used. The MAP 256K RAM card is supplied as set up in example 1 (Card Number One).

If existing RAM cards are to be incorporated, DO NOT enable rows of RAM on LB2 which do not exist.

EXAMPLE 1 STANDARD CONFIGURATION (NASCOM 2 & GEMINI G811)

32K/64K Page Mode System.

Card Number 1

	LB1			LB2	
A16 1		20 SA	P0 1		16 IN
A17 2	4-20	19 SB	P1 2	1-16	15 OUT
A18 3	5-19	18 SC	P2 3	15-13	14
Q1 4	6-18	17 /EN	P3 4	2-12	13 R0
Q2 5	9-17	16 A19	P4 5	3-11	12 R1
Q3 6	15-13	15 EN	P5 6	4-10	11 R2
Q0 7		14 OUT	P6 7		10 R3
IN 8		13 F0	P7 8		9
Q4 9		12 Q5			
10		11 Q6			

Card Number 2

	LB1			LB2	
A16 1		20 SA	P0 1		16 IN
A17 2	4-20	19 SB	P1 2	5-13	15 OUT
A18 3	5-19	18 SC	P2 3	6-12	14
Q1 4	6-18	17 /EN	P3 4	7-11	13 R0
Q2 5	9-17	16 A19	P4 5	8-10	12 R1
Q3 6	15-13	15 EN	P5 6		11 R2
Q0 7		14 OUT	P6 7		10 R3
IN 8		13 F0	P7 8		9
Q4 9		12 Q5			
10		11 Q6			

Card Number 3

	LB1			LB2	
A16 1		20 SA	P0 1		16 IN
A17 2	4-20	19 SB	P1 2	1-13	15 OUT
A18 3	5-19	18 SC	P2 3	2-12	14
Q1 4	6-18	17 /EN	P3 4	3-11	13 R0
Q2 5	8-9	16 A19	P4 5	4-10	12 R1
Q3 6	15-13	15 EN	P5 6		11 R2
Q0 7	17-14	14 OUT	P6 7		10 R3
IN 8		13 F0	P7 8		9
Q4 9		12 Q5			
10		11 Q6			

Card Number 4

LB1				LB2			
A16 1		20 SA		P0 1		16 IN	
A17 2	4-20	19 SB		P1 2	5-13	15 OUT	
A18 3	5-19	18 SC		P2 3	6-12	14	
Q1 4	6-18	17 /EN		P3 4	7-11	13 R0	
Q2 5	8-9	16 A19		P4 5	8-10	12 R1	
Q3 6	15-13	15 EN		P5 6		11 R2	
Q0 7	17-14	14 OUT		P6 7		10 R3	
IN 8		13 F0		P7 8		9	
Q4 9		12 Q5					
10		11 Q6					

EXAMPLE 2 GEMINI G813 (Memory Mapper)

Note BIT Q0 on LB1 is set to 1 by RP/M on the G813

Card Number 1

LB1				LB2			
A16 1		20 SA		P0 1		16 IN	
A17 2	1-20	19 SB		P1 2	2-13	15 OUT	
A18 3	2-19	18 SC		P2 3	3-12	14	
Q1 4	3-18	17 /EN		P3 4	4-11	13 R0	
Q2 5	7-15	16 A19		P4 5	5-10	12 R1	
Q3 6	16-17	15 EN		P5 6		11 R2	
Q0 7		14 OUT		P6 7		10 R3	
IN 8		13 F0		P7 8		9	
Q4 9		12 Q5					
10		11 Q6					

Card Number 2

LB1				LB2			
A16 1		20 SA		P0 1		16 IN	
A17 2	1-20	19 SB		P1 2	6-13	15 OUT	
A18 3	2-19	18 SC		P2 3	7-12	14	
Q1 4	3-18	17 /EN		P3 4	8-11	13 R0	
Q2 5	7-15	16 A19		P4 5		12 R1	
Q3 6	16-17	15 EN		P5 6		11 R2	
Q0 7		14 OUT		P6 7		10 R3	
IN 8		13 F0		P7 8		9	
Q4 9		12 Q5					
10		11 Q6					

Card Number 3

	LB1			LB2	
A16 1		20 SA	P0 1		16 IN
A17 2	1-20	19 SB	P1 2	1-13	15 OUT
A18 3	2-19	18 SC	P2 3	2-12	14
Q1 4	3-18	17 /EN	P3 4	3-11	13 RO
Q2 5	7-8	16 A19	P4 5	4-10	12 R1
Q3 6	14-17	15 EN	P5 6		11 R2
Q0 7	15-16	14 OUT	P6 7		10 R3
IN 8		13 FO	P7 8		9
Q4 9		12 Q5			
10		11 Q6			

Card Number 4

	LB1			LB2	
A16 1		20 SA	P0 1		16 IN
A17 2	1-20	19 SB	P1 2	5-13	15 OUT
A18 3	2-19	18 SC	P2 3	6-12	14
Q1 4	3-18	17 /EN	P3 4	7-11	13 RO
Q2 5	7-8	16 A19	P4 5	8-10	12 R1
Q3 6	14-17	15 EN	P5 6		11 R2
Q0 7	15-16	14 OUT	P6 7		10 R3
IN 8		13 FO	P7 8		9
Q4 9		12 Q5			
10		11 Q6			

INCORPORATION OF AN EXISTING RAM CARD

RAM A

Does not utilise paging and cannot be used.

RAM B and G802

These cards can be incorporated to a limited extent. Firstly ensure that these cards are fitted with the ICs necessary for paging,(see RAM B or G802 manual), then enable them on a page other than 0 (so that they are not selected on reset).