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*     MAP 80 SYSTEMS LTD    *
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*          MPI MANUAL       *
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CONTENTS
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SECTION 1 - INTRODUCTION

This manual has been written to introduce you to your new MPI (Multi Purpose Interface) for the 80 bus/Nasbus range of computers. Read all sections and be sure you understand its operation before you proceed. If you have purchased the kit version, a seperate assembly manual will have been supplied. Read it carefully before you start assembly.

The MAP MPI has been designed so that it will work with all the existing Nasbus/80 Bus computers. The card can optionally use a WD2793 or WD2797 for interface to a mixture of 8" and/or 5" floppy disk drives, probably several of the new 3" drives too. Links are provided so that the 2793 option can link the card to the Nascom FDC format or the 2797 to the MAP format. A SASI interface is also provided, which will normally be used to provide interface to a Winchester hard disk. When linked for a 2797 the card can be used as a direct replacement for the Gemini G829, and when linked for a 2793 as a functional replacement for the Nascom FDC. The card can also support serial communications via a standard Z80 CTC and SIO combinations, Channel A of the SIO communicates via a standard RS232 interface and Channel B via a high speed multi-drop interface (proposed standard RS485). Clocking for the SIO can be routed via the CTC to provide software selectable baud rates, the clocks being provided by system clock division, RS232 input or the user can obtain two frequencies on board by inserting crystals into oscillator circuitry provided. Clocking options are selected on LB1 (marked 1C19 !!).

SECTION 2 - MPI PORT ASSIGNMENTS

The MPI uses a total of 16 ports, these can be link selected to an even 16 port boundary i.e 0,2,4,6,8,A,C,E. The card has been supplied with a port allocation of E0 to EF and this configuration is assumed in subsequent notes. The card can be located at a different port boundary but special software will have to be written.

PORT ALLOCATION (Note all Port addresses are in HEX)

The following list of ports are for the MPI with links set for standard M.A.P. 80 and Gemini systems. This information is also for Nascom systems using either M.A.P. 80 or Gemini software.

E0	Read	2797 Status register
E0	Write	2797 Command register
E1	Read or Write	2797 Track register
E2	Read or Write	2797 Sector register
E3	Read or Write	2797 Data register
E4	Read	Read 2797 pins DRQ,INTRQ and RDY
E4	Write	Select drive
E5	Read or Write	SASI Data
E6	Read	SASI Status
E6	Write	SASI Control
E7	Not used	
E8	Read or Write	CTC Channel 0
E9	Read or Write	CTC Channel 1
EA	Read or Write	CTC Channel 2
EB	Read or Write	CTC Channel 3
EC	Read or Write	SIO Channel A Data
ED	Read or Write	SIO Channel B Data
EE	Read or Write	SIO Channel A Control
EF	Read or Write	SIO Channel B Control

The following list of ports are for the MPI with links set for standard Lucas Nascom systems using Lucas Nascom software.

E0	Read	2793 Status register
E0	Write	2793 Command register
E1	Read or Write	2793 Track register
E2	Read or Write	2793 Sector register
E3	Read or Write	2793 Data register
E4	Read or Write	Drive select/density/clock
E5	Read	Read 2793 pins DRQ,INTRQ and RDY
E6	Read or Write	SASI Data
E7	Read	SASI Status
E7	Write	SASI Control
E8	Read or Write	CTC Channel 0
E9	Read or Write	CTC Channel 1
EA	Read or Write	CTC Channel 2
EB	Read or Write	CTC Channel 3
EC	Read or Write	SIO Channel A Data
ED	Read or Write	SIO Channel B Data
EE	Read or Write	SIO Channel A Control
EF	Read or Write	SIO Channel B Control

FDC PORTS E0 through E3

Ports E0 through E3 directly access the 2797/2793 registers, the function of these are complex and data can be best obtained from Western Digital's application document.

FDC PORT E4 (Card linked for 2797 M.A.P 80 or Gemini format)

When written to, the least significant 4 bits of port E4 select one of 4 drives, bit 0 set enables drive 0, bit 1 drive 1 etc. only one bit should be set at any time. Bit 4 is used to set the 2797 to either single density FM (set 1) or double density MFM (reset 0), bit 5 is used to select 5" (reset 0) or 8" (set 1) operation, this bit can also be set when operating 5" drives in order to double the FDC clock at head step time and permit head step at 3ms. bits 6 and 7 are unused. When port E4 is read access is allowed to three 2797 pins, bit 0 holds the INTRQ (pin 39) line, bit 1 inverted READY (pin 32) and bit 7 DRQ (pin 40), all other bits are tied low. The WD2797 is an upgrade from the WD1797 but has on chip data separation and write pre-compensation.

FDC PORT E4 (Card linked for 2793 Nascom format)

When written to, the least significant 4 bits of port E4 select one of 4 drives, bit 0 set enables drive 0, bit 1 drive 1 etc. only one bit should be set at any time. Bit 4 is used to select side for double sided disk operation, Bit 5 is unused, Bit 6 is used to set the 2793 to either single density FM (set 1) or double density MFM (reset 0), and Bit 7 is used to select 5" (reset 0) or 8" (set 1) operation, this bit can also be set when operating 5" drives in order to double the FDC clock at head step time and permit head step at 3ms. When port E4 is read the status of bits last output to port E4 can be read.

SASI PORTS

The SASI interface utilises two ports a read/write data port and a read status/write control port. On a M.A.P 80/Gemini 2797 card the SASI data port is E5 and the control/status port is E6. On a Nascom 2793 card the data port is E6 and the control/status port is E7. Writing to the SASI data port latches output data for the external device to read, reading the SASI data port inputs data from an external device and acknowledges receipt via the SASI ACK line. Note that the SASI has and inverted bus but non-inverting buffers have been used to retain compatability with existing systems, user software therefore must invert data before output and after input.
Writing to the SASI control/status port causes an active strobe to be sent to SASI control lines RST,SEL and ATN if the corresponding bit of the output data is reset. Reading the SASI control/status port inputs the status of the SASI I/O,C/D,MSG,BSY and REQ lines, the upper 3 bits are normally pulled high but are sometimes changed to act as console ID on networking systems, user software should ensure that these bits are masked when reading SASI status.
The SASI interface was designed using the Xebec Winchester disk Controller and this is the controller that we recommend.

Bit assignment

Control Port	Bit 0	ATN (Not used by Xebec)
	Bit 1	SEL
	Bit 2	RST
	Bit 3	Not used
	Bit 4	"
	Bit 5	"
	Bit 6	"
	Bit 7	"
Status Port	Bit 0	REQ
	Bit 1	I/O
	Bit 2	C/D
	Bit 3	MSG
	Bit 4	BUSY
	Bit 5	ID 0
	Bit 6	ID 1 Network identification
	Bit 7	ID 2

SECTION 3 - MPI PIN ASSIGNMENTS

50 way connector SASI (J1)

Pin	
2	Data 0
4	Data 1
6	Data 2
8	Data 3
10	Data 4
12	Data 5
14	Data 6
16	Data 7
18	
20	
22	
24	
26	
28	
30	
32	ATN
34	
36	BUSY
38	ACK
40	RST
42	MSG
44	SEL
46	C/D
48	REQ
50	I/O

4 way connector RS485 (J2)

Pin	
1	DATA
2	DATA
3	CLOCK
4	CLOCK

16 way connector RS232 (J3)

Pin	
1	
2	+12V
3	TX Data
4	NC
5	RX Data
6	-12V
7	RTS
8	NC
9	CTS
10	NC
11	DCD
12	Spare RS232 Output
13	Signal Ground
14	DTR
15	Spare RS232 Input
16	NC

34 way connector FDC (J4)

Pin	
6	See Note 1
8	Index pulse
10	Drive select 0/A
12	Drive select 1/B
14	Drive select 2/C
16	Motor on
18	Direction select
20	Step
22	Write data
24	Write gate
26	Track 0
28	Write protect
30	Read data
32	Side select
34	See Note 1

50 way connector FDC (J5)

Pin	
4	Motor on
6	Motor on
8	
10	
12	
14	Side select
16	
18	
20	Index pulse
22	
24	
26	Drive select 0/A
28	Drive select 1/B
30	Drive select 2/C
32	
34	Direction select
36	Step
38	Write data
40	Write gate
42	Track 0
44	Write protect
46	Read data
48	Read data
50	

Note 1 - Pin assignments differ between drives for pin's 6 & 34. The chart below gives details for several commonly used drives.

DRIVE TYPE	PIN 6	PIN 34
Teac FD-55	Drive select 3/D	Ready
Pertec FD250	Drive select 3/D	Spare
Micropolis 1015	Ready	Drive select 3/D

These drives can all be accomodated by appropriate linking of Link 4. See Section 7 for details.

Note 2 - All odd pins on the 50 way connector (J1) are grounded.
All odd pins on the 34 way connector (J3) are grounded.
All odd pins on the 50 way connector (J5) are grounded.

SECTION 4 - MAP 80 / NASCOM CHANGES

To set the MPI up to run as a Lucas Nascom compatable controller, a WD2793 controller must be fitted instead of the normally used WD2797. Links marked a->m<-n on the board must be set to a->m for a MAP 80 Gemini controller and must be set to a->n for a Nascom controller. The SASI port select L18 is also different, link c - 7 and d - 6 for Nascom format or c - 6 and d - 5 for MAP Gemini format.

SECTION 5 - LINKS

L1	SASI ATN (Not required by Xebec controller)	
L2	8" Motor enable	
L3	8" Side select	
L4	Drive/Ready select (Ready in or drive select out)	
L5	8" Read data	
L6	2797 Density select	a-m MAP 80 a-n Nascom
L7	Terminal ident 0	
L8	Terminal ident 1	
L9	Terminal ident 2	
L10	Ready input	
L11	Spare RS232 sync/ready	
L12	Write pre-compensation select	
L13	FDC clock select	a-m MAP 80 a-n Nascom
L14	Side select	a-m MAP 80 a-n Nascom
L15	FDC ready selected	a-b EXT a-b INT
L16	Port select	
L17	FDC port selection	b-c MAP 80 a-b,c-d Nascom
L18	SASI port select	c-6,d-5 MAP 80 c-7,d-6 Nascom
L19	IEI/OEO	
L20	IO-EXT	
L21	Clock select	
L22	Terminal ident 3	

LINK HEADER (IC 19)

2MHz Clock -1	20- CTC CLK 1
1MHz Clock -2	19- CTC CLK 2
Aux. Clock -3	18- CTC CLK 3
CTC (TO)2 -4	17- CTC CLK 0
CTC (TO)1 -5	16- SIO TxCa
CTC (TO)0 -6	15- SIO RxCa
RS485 CLK IN -7	14- SIO RxTxCb
500 KHz -8	13- RS485 CLK OUT
Aux. Clock 1 -9	12- Spare RS232 OUT
Spare RS232 IN -10	11- Aux. Clock 2

SECTION 6 - COMPONENT LIST

IC's	
1	74LS244
2	75175
3	1488
4	74LS273
5	81LS95/74LS465
6	75174
7	1489
8	7438
9	7406
10	81LS95/74LS465
11	74125
12	74LS14
13	74LS273
14	74LS367
15	Z80 CTC
16	Z80 SIO
17	WD2797/WD2793(Nascom)
18	74LS74
19	LINK HEADER
20	74LS138
21	74LS04
22	81LS95/74LS465
23	81LS95/74LS465
24	74LS163
25	74LS32
26	74LS11
27	74LS123
28	74LS123
29	74LS04
30	74LS245
31	74LS138
32	74LS139
33	74LS125
34	74LS244

FDC AND SASI ONLY - 1,4,5,8,9,10,11,12,13,14,17,18,22,23,27,28

SERIAL ONLY - 2,3,6,7,15,16,21,+link header block

RESISTORS
==========

1,2,13,14,21,22,23	9	150R
3,4,5,6,7,25,32,33,39,40		330R
8,9,10,11,12		220R
15,16,17,18,19,20,24,26,27,28,29,30,31,36		1K
34		560K
35		270K
37		100K
38		5K6
41,42,43,44		4K7
VR1		10K POT
VR2		50K POT

CAPACITORS
==========

31	1uf TANT
32	33pf
30	10uf TANT
29,34,39	47uf TANT
1,2	2.2uf TANT 16v
16	.22uf
VC1	5-65pf TRIMMER

ALL OTHER CAPACITORS ARE 0.01uf

MISC
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J1	50 WAY IDC
J2	4 WAY MOLEX
J3	16 WAY IDC
J4	34 WAY IDC
J5	50 WAY VERT IDC
D1	IN4148