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\* MAP 80 SYSTEMS LTD \*  
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\* CPU MANUAL \*  
\*  
\* PRELIMINARY \*  
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MAP 80 SYSTEMS LTD  
Chertsey Computer Centre,  
1 Windsor Street,  
CHERTSEY,  
Surrey. Tel 09328 64663  
Issue 1 18th November 1983.

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INTRODUCTION

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#### INTRODUCTION

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The MAP CPU is a NASBUS/80-BUS compatible card designed around a Z80A CPU running at 4Mhz. The card features extended memory addressing using the memory mapping technique to provide address lines A16 thru' A19. 64k of RAM is provided on board, but the extended addressing permits direct access to 1Mb of memory using MAP 256k RAM boards with additional memory available using 1Mb paging. A 4k EPROM is provided on board to initialise the memory mapping system and boot an operating system from floppy disk.

The standard Z80 family of ICs are used to provide 16 IO lines (PIO) dual RS232 serial channels (SIO) and Clock/Interrupt control (CTC) and facilities for a 7 or 8 bit parallel keyboard is provided, this input is controlled by the CTC to provide keyboard interrupt capability.

#### COMMISSIONING

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Unpack your CPU board carefully and examine it for any mechanical damage. In the event of any damage please contact MAP 80 or your dealer. The CPU card will have been despatched fully tested and working, and is ready for operation by plugging it into a NASBUS/80-BUS system, ensure that the slot in the CPU matches the keyway in the edge connector. NOTE if the CPU is to be used with a Gemini backplane or with one of their multiboard cards in the system, it will be necessary to isolate A19 from the bus as Gemini ground this line. This can be accomplished by cutting the etch on the solder side of the board at link LK8 (see section on links for full details). To ensure correct operation of the MAP CPU this bus line must be A19 or MUST be grounded with A19 on the CPU isolated.

## CPU SECTION

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The heart of the card is of course the Z80A processor, as supplied this is clocked at 4Mhz without WAIT states, the clock is derived from a crystal oscillator circuit designed around a pair of 74S04 gates. The frequency provided by the oscillator is divided by a 74LS163 to provide optional clock options. Versatility of clock selection is provided by link block LB2 where various options for system clock (0) auxillary clock and CTC clocks can be chosen, see full details later. In order to provide necessary amplitude and skew for the Z80 chip set, the system clock is condition by a standard configuration of TR1 and TR2.

Recommended circuitry is also used to provide system reset, on power up R51 and C55 provide a reset pulse of sufficient duration to initialise the system, furthur resets can be implemented by taking bus line 10 (reset switch) to 0v. IC42a and IC37a ensure that the subsequent reset pulse occurs at the right time and is of a duration which does not jeopardize the contents of dynamic RAM, full details can be found in the Zilog or MOSTEK technical manuals.

All of the CPU output signals, data, address and control are buffered and output to the NAS-BUS to provide for system expansion, if a system with a lot of cards is envisaged it is recommended that a properly terminated bus backplane is used.

To provide memory mapping address lines A12 thru' A15 are decoded by two fast TTL RAM chips (IC34 and IC39) to provide A12 thru' A19, on power up these chips contain undetermined values and require setting up, in order to achieve this the system reset pulse resets the two 74LS74 flip flop gates of IC27, these gates enable the on board EPROM IC35 such that it floods the memory map and is repeated at all 4k boundaries and will therefore be executed regardless of the address put out on A12 thru' A19. The first thing the program here will do is to set up the TTL RAM to give true address on A12 thru' A15 with A16 thru' A19 giving 0 (64k bank 0). Once this has been achieved it is no longer necessary for the EPROM to flood memory and this is achieved by outputting to port OF8H, this flips IC27a and the EPROM will only flood memory again after a reset. Outputting to port OF8H also clocks IC27b, but here the output depends on the value of D0, if D0 is reset the EPROM is left in the memory map but it now only occupies locations F000H thru' FFFFH, if D0 is set the EPROM is completely disabled. It is therefore possible to use the on board EPROM to for instance boot a disk operating system and then remove the EPROM from the memory map to leave a full 64k of RAM available to the operating system, this is indeed what the EPROM supplied does, it expects to see a MAP VFC or VFC and MPI from which it boots track 0 sector 0 from the first floppy drive.

## IO SECTION

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The IO section is based around a standard Z80 chip set of CTC,SIO and PIO together with a pair of 74LS257s to provide A 7 or 8 bit parallel ASCII keyboard input. A 74S472 PROM is used to provide on board port decode and data direction select during interrupt acknowledge. The PIO is uncommitted and all data and control lines are taken to the edge of the board at PL4. The 2 SIO channels are interfaced to the outside world via 2 separate RS232 driver/receivers

75188 and 75189. SIO Channel A is taken to the edge of the board at IDC A (PL2) and Channel B at IDC B (PL1). Link block LB1 selects clock options for the SIO from either 1) external clock input via an RS232 receiver 2) from the on board Xtal divider or 3) from one of the 3 CTC channels which provide time out pins. As supplied CTC channel 0 is clocked by 2 MHz and channel 1 by 1 MHz, both frequencies coming from the on board Xtal divider. CTC channel 0 is then used to clock SIO channel A and CTC channel 1 to clock SIO channel B. An external parallel ASCII keyboard can be connected to IDC PL3 to provide keyboard input and as supplied CTC channel 3 is clocked by the keyboard strobe so that the CTC can be used as an interrupt controller when keyboard entry is required. CTC channel 2 is spare.

The Z80,PIO,CTC and SIO are sophisticated devices deserving manuals of their own, full information is best obtained from the excellent technical manuals obtainable from ZILOG or MOSTEK.

#### Recommended literature.

1982/1983 Designers guide - MOSTEK or 1981 Data Book ----- ZILOG  
(Either of the above books contain basic versions of all four of the technical manuals)

Z80 programming manual ---- MOSTEK

Z80 Assembly Language Programming --- Lance A Leventhal

#### MEMORY SECTION

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64k of RAM is provided on board using 4164 64k\*1 dynamic RAM chips, control signals for this array is provided by IC33 a 74LS608 memory cycle controller, address lines are multi-plexed by a pair of 74157 selectors and the 64k bank is selected by a comparator IC14 which decodes A16 thru' A19. As supplied the on board bank is selected as bank 0 but this may be altered by changes made to links 3,4,5 and 6.

#### MEMORY MAPPING

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Memory mapping is a means of extending the address range of a Z80 beyond it's usual limit of 64k, this is achieved by decoding address lines A12 thru' A15 in a pair of TTL RAMs to produce address lines A12 thru' A19. A12-A15 on the bus will still select a 4k slot within a 64k bank (not necessarily the same 4k slot indicated by A12-A15 off the Z80) but now A16-A19 will select one of 16 banks of 64k within which that 4k block will be found. The Z80 is still only capable of directly addressing 64k at any one time, but by simply changing the decode in the TTL RAM it is possible to easily place any 4k block in any 4k slot in that 64k. The RAM board will of course have to be capable of decoding A16-A19, and at the moment only the MAP 256 is able to do this. Selecting a 4k block into the memory map is achieved by outputting the 64k bank and the 4k block to the mapping port (OFEH). The 64k bank is placed in the upper nibble and the 4k block in the lower nibble.

For example to select bank 1 block 8000H-8FFFFH

LD A,18H

OUT (OFEH),A

But this isn't the whole story, in the example above we haven't told the TTL RAM where to place the selected block. The TTL RAM in

normal use is being addressed by and thus decoding A12-A15 it is therefore necessary to address A12-A15 whilst outputting the block select byte above. This is achieved by using a feature of the OUT (C),r instruction, when this instruction is used the contents of register C is placed on address lines A0-A7 to select the required port, as a bonus however the contents of register B is placed on address lines A8-A15 and thus it is possible to address the TTL RAM whilst outputting to the mapping port by placing the slot we require in the upper nibble of register B, look on the instruction not as OUT (C),r but rather as OUT (BC),r.

Now to select bank 1, block 8000H-8FFFFH in slot 1000H-1FFFFH

```

LD BC,01FEH      ;B addresses 1000H-1FFFFH
                  ;C points to mapping port
LD A,18H          ;Upper nibble bank 1
                  ;Lower nibble 8000H-8FFFFH
OUT (C),A

```

As the OUT (C),A instruction is implemented A0-A7 holds OFEH addressing the mapping port enabling a write to the TTL RAM, A12-A15 holds 1 (from the upper nibble of B) addressing the TTL RAM and the data bus holds 18H which is written to the TTL RAM at location 1. Now whenever the Z80 outputs an address on it's address lines in the range 1000H-1FFFFH, A12-A15 will hold 1 which will address the TTL RAM, as we have just written the byte 18H at this location this byte will appear on the data outputs of the TTL RAM and it is this that is sent out to the NAS-BUS as address lines A12-A19, i.e the Z80 calls for the contents of address 18865H but the address bus selects 18865H.

At first this may seem confusing but once grasped you will find this the most versatile form of extended addressing for the Z80 enabling implementations of such things as MPM or CPM PLUS. (Provided of course you have a RAM board which supports it).

#### LINK BLOCKS

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#### SIO/CTC clock selection LB1

Clock/Trigger CTC channel 3 -1	20- Keyboard strobe
Clock/Trigger CTC channel 2 -2	19- Clock 2 from LB2 (1Mhz)
Clock/Trigger CTC channel 1 -3	18- Clock 1 from LB2 (2Mhz)
Clock/Trigger CTC channel 0 -4	17- Time out CTC channel 0
RX clock SIO channel A -5	16- Time out CTC channel 1
TX clock SIO channel A -6	15- Time out CTC channel 2
RX/TX clock SIO channel B -7	14- NC
Spare RS232 output (IDC A) -8	13- NC
Spare RS232 output (IDC B) -9	12- Spare RS232 input (IDC A)
Ground -10	11- Spare RS232 input (IDC B)

As supplied LB1 is linked as follows :-

- Pin 1 to pin 20 (keyboard strobe to CTC channel 3)
- Pin 19 to pin 3 (CTC 1 clocked at 1Mhz)
- Pin 18 to pin 4 (CTC 0 clocked at 2Mhz)
- Pin 17 to pin 5 and 6 (SIO A clocked by CTC 0)
- Pin 16 to pin 7 (SIO B clocked by CTC 1)

#### System clock selection LB2

XTAL output (4Mhz)	-1	16- NC
XTAL/2	-2	15- NC
XTAL/4	-3	14- On board system clock in
XTAL/8	-4	13- On board system clock out
XTAL/16	-5	12- Bus system clock
NC	-6	11- Bus AUX CLOCK
NC	-7	10- Clock 1 to LB1
Ground	-8	9- Clock 2 to LB1

As supplied LB2 is linked as follows :-

Pin 1 to pin 14 (On board system clock 4Mhz)

Pin 2 to pin 10 (2Mhz to LB1)

Pin 3 to pin 9 (1Mhz to LB1)

Pin 13 to pin 12 (System clock to bus)

#### LINKS

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Boards are supplied with standard link options selected during board manufacture, to change a link the existing PCB track found on the solder side of the board will need to be cut first and then the new option selected by soldering in a short wire link. Where a link comprises 3 holes the centre hole is connected to one of the outer holes, these outer holes are referred to by their cardinal point. Hold the CPU board with the IDC connectors towards you, then the edge connector is North the IDC connector South the RAM array East and the remaining side West.

LK1 -- Supplied not connected

This connects -12V to pin 15 of the keyboard IDC connector. Make this link only if your keyboard requires -12V

LK2 -- Supplied with link connected for 8 bit keyboard

When an 8 bit ASCII keyboard is used link Centre to South, this connects pin 14 (D7) of the keyboard IDC to the keyboard input buffer IC 5.

When a 7 bit keyboard is used link Centre to North, this provides a 0 input for D7.

LK3 - LK4 - LK5 - LK6 -- Supplied with on board RAM selected as bank 0

These 4 links select which 64k bank the on board RAM occupies, each link can be selected high (Centre to South) or low (Centre to North) a comparator IC 14 compares the state of these for links against address lines A16 thru' A19 and enables CAS to the on board RAM when a match is found (on board bank is being addressed). The on board bank will usually be selected as bank 0, but see the RAM 256 manual for exceptions to this. In order to select a bank other than 0 one or more of the links will need to be selected high as shown in a few examples below :-

A16	A17	A18	A19
LK6	LK5	LK4	LK3

BANK 0	0	0	0	0
BANK 1	1	0	0	0
BANK 2	0	1	0	0

BANK 3	1	1	0	0
BANK 6	0	1	1	0
BANK 8	0	0	0	1
BANK 15	1	1	1	1

LK7 -- Supplied connected for positive keyboard strobe

This links the keyboard strobe on to the card inverting it if a negative strobe keyboard is being used, for positive strobe keyboards link Centre to West, for negative strobe keyboards link Centre to East.

LKB -- Supplied with A19 connected to bus line 49

This links address line A19 to either bus line 49 or bus line 66, link Centre to West for connection to line 49 or Centre to East for bus line 66.

#### IDC CONNECTORS

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All external IO is brought to the edge of the card where simple connection can be made via standard IDC connectors.

PL1 RS232 SIO CHANNEL B  
and

PL2 RS232 SIO CHANNEL A

	IDC (DB25)	(DB25)	IDC
NC	-1	(1)	(14) 2- +12V
TX Data	-3	(2)	(15) 4- NC
RX Data	-5	(3)	(16) 6- -12V
RTS	-7	(4)	(17) 8- NC
CTS	-9	(5)	(18) 10- NC
DCD	-11	(6)	(19) 12- Spare RS232 Output
Signal Ground	-13	(7)	(20) 14- DTR
Spare RS232 Input	-15	(8)	(21) 16- NC

This arrangement has been chosen so that it is possible to quickly connect directly using crimp connectors to a standard DB25 plug, connect pin 1 of the IDC to pin 1 of the DB25 etc. Some pins in the DB25 will of course be left unconnected. The DB25 pin numbers are shown above in brackets.

#### PL3 ASCII KEYBOARD INPUT

+5v	-1	2-	Strobe
NC	-3	4-	0v
D5	-5	6-	D4
D6	-7	8-	0v
NC	-9	10-	D2
D3	-11	12-	D0
D1	-13	14-	D7
-12v	-15	16-	NC

Note. -12 volts is only available on pin 15 if link LK1 is made, do not make LK1 unless your keyboard requires it as if you accidentally insert the keyboard IDC plug in the wrong way round the

result could be exciting if -12v is connected, similarly ensure you do not plug the keyboard into an RS232 socket (PL1 or PL2)!!!.

#### PL4 PIO

B5	-1	2-	B4
B6	-3	4-	B3
B7	-5	6-	B2
A RDY	-7	8-	B1
B STB	-9	10-	BO
A STB	-11	12-	B RDY
AO	-13	14-	Ground
A1	-15	16-	Ground
A2	-17	18-	Ground
A3	-19	20-	+5v
A4	-21	22-	+5v
A5	-23	24-	A7
A6	-25	26-	Ground

#### IO PORT ASSIGNMENT

EPROM flood disable	OF8H or OFAH (Write only)
EPROM enable/disable	OF8H or OFAH (Write only)
Mapping RAM	OFEH or OFCH (Write only)
PIO A DATA	OB4H (Read/Write)
PIO B DATA	OB5H (Read/Write)
PIO A CTRL	OB6H (Read/Write)
PIO B CTRL	OB7H (Read/Write)
CTC CH0	OB8H (Read/Write)
CTC CH1	OB9H (Read/Write)
CTC CH2	OB AH (Read/Write)
CTC CH3	OB BH (Read/Write)
SIO A DATA	OB CH (Read/Write)
SIO B DATA	OB DH (Read/Write)
SIO A CTRL	OB EH (Read/Write)
SIO B CTRL	OB FH (Read/Write)

#### INTERRUPT PRIORITY

Priority in descending order
SIO channel A
SIO channel B
PIO port A
PIO port B
CTC channel 0
CTC channel 1
CTC channel 2
CTC channel 3

#### BUS DEFINITION

MP/M and CPM PLUS are trade marks of DIGITAL RESEARCH INC.  
NASBUS is a trade mark of LUCAS LOGIC LTD.  
BO-BUS is a trade mark of Gemini Microcomputers Ltd.