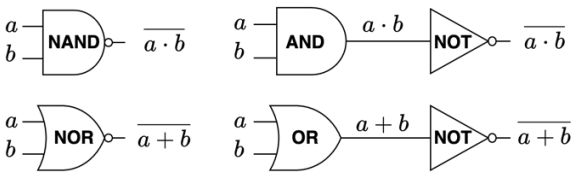
CS281 – Homework #1

1. The RISC-V processor does not contain instructions for the NAND and NOR logical operations because they can be implemented using other existing instructions. The digital circuit representation of NAND and NOR is shown below:



   Implement both of these operations using valid RISC-V instructions. Write valid RISC-V code in as few insructions as possible for the following expressions:

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a. s1 = s2 NAND s3
b. s1 = s2 NOR  s3
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2. RISC-V employs a load/store architecture. Describe the key principles of this model and discuss a significant trade-off it imposes on programmers, particularly in terms of memory manipulation and code complexity.

3. Suppose you are a capable hardware designer and just came up with a great idea for a novel new IoT device. You have the choice of custom designing the processor for your IoT device from scratch, or to incorporate an existing ISA such as Intel/AMD x64, ARM or RISC-V. Briefly describe why RISC-V would be a compelling option for your design versus designing from scratch or picking from alternatives like ARM or Intel/AMD.