2020 Digital IC Design Homework 3: Approximate Average

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NAME	高靖智						
Student ID	P76094088						
Simulation Result							
Functional simulation	Pass	Gate-level simulation	Pass 3729			372930 (ns)	
VSIM 212> run -all							
Synthesis Result							
Total logic elements				583			
Total memory bit				0			
Embedded multiplier 9-bit				0			
element							
Revision Name  Top-level Entity Name CS Sydone II Device EP2C70F896C8 Final Met timing requirements Total logic elements Dedicated logic registers Total registers Total pins Total virtual pins Total memory bits Embedded Multiplier 9-bit elements  CS CS CS CS CY Cydone II EP2C70F896C8 Final No 583 / 68,416 (< 583 / 68,416 (< 72 / 68,416 (< 72 / 68,416 (< 72 / 68,416 (< 73 / 68,416 (< 74 / 68,416 (< 75 / 68,416 (< 76 / 68,416 (< 77 / 68,416 (< 77 / 68,416 (< 78 / 68,416 (< 79 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6 / 68,416 (< 6				22:22:35 2020 10 SP 1 SJ Full Version			
Total PLLs 0/4(0%)					Min C	ycle: 187	
Description of your design							

## Description of your design

循序電路中 always@ (negedge clk),使用延遲 clk 的方式,獲得 9 個 input。接下來進入組合電路,算出 9 個 input 的 sum 後,算出 avg,再透過第一個迴圈計算出那些 input 小於 avg,並存在[8:0] jmp 這個變數中,方便了解哪個 input 比較小,接下來透過第二個迴圈,算出小於 avg 中最接近的 input,接下來再用(sum+該 input\*9)/8 即可得出正確 output。

Scoring = (583 + 0 + 9\*0) \* 372930(ns) = 217418190(ns)

Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) × (gate-level simulation time in  $\underline{ns}$ )