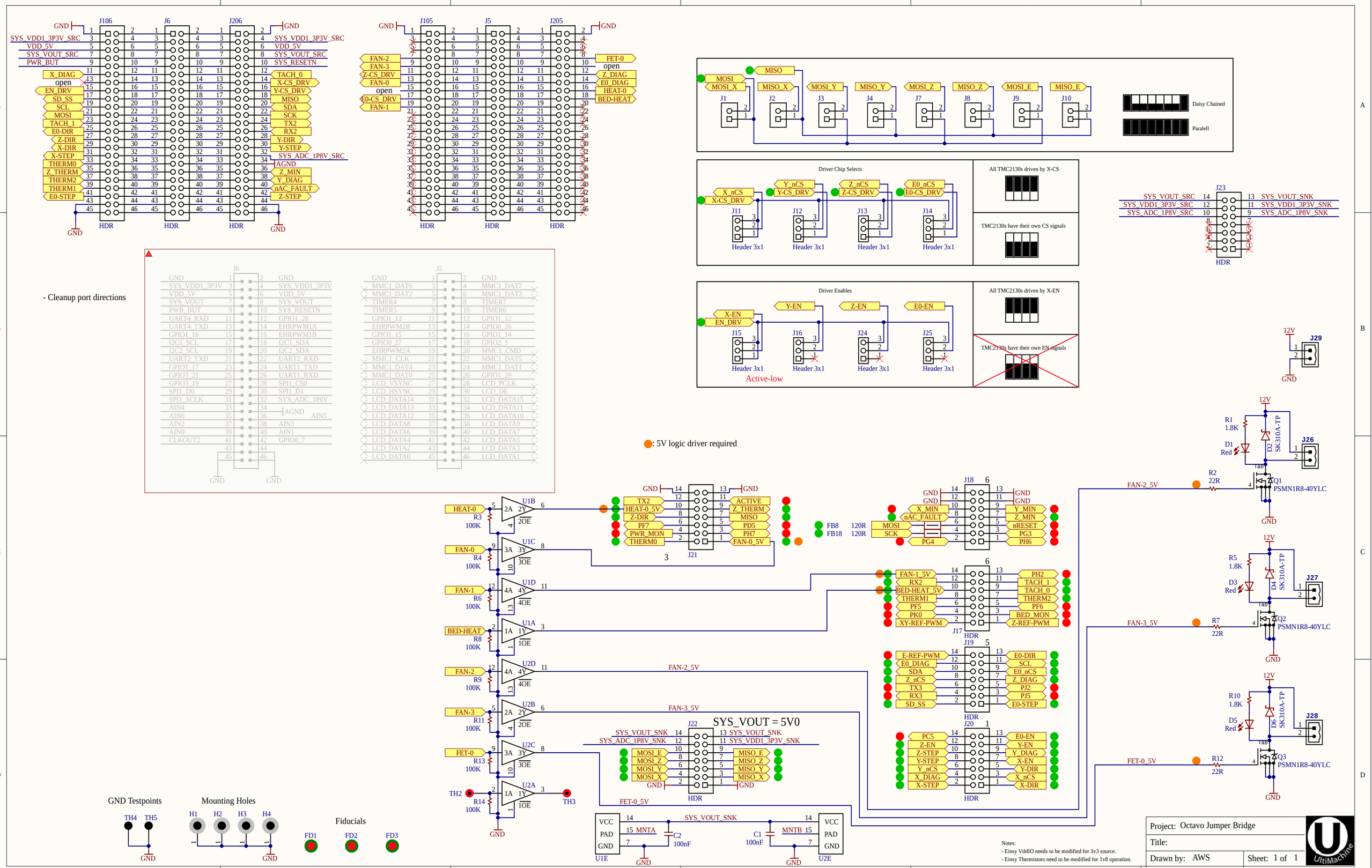
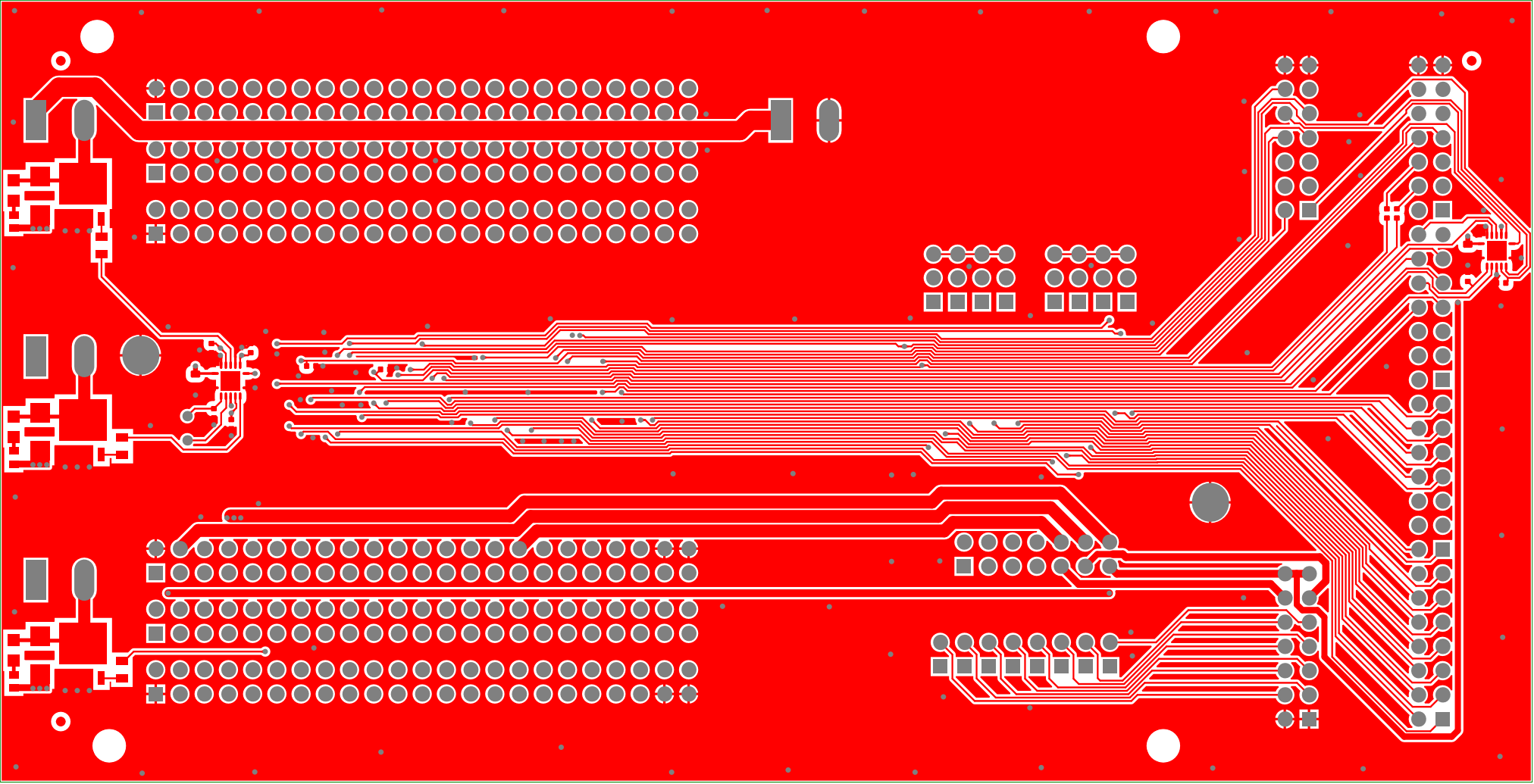
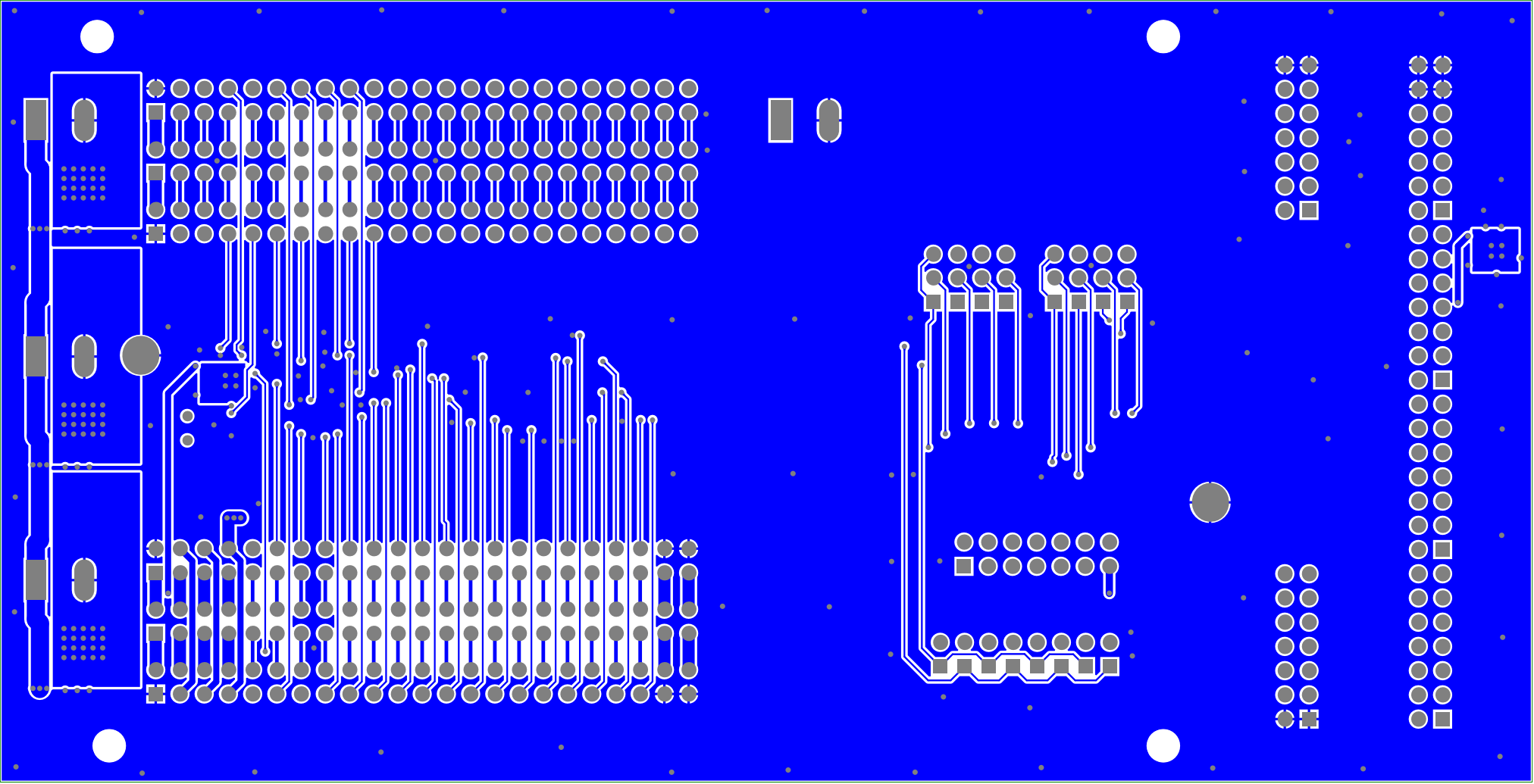
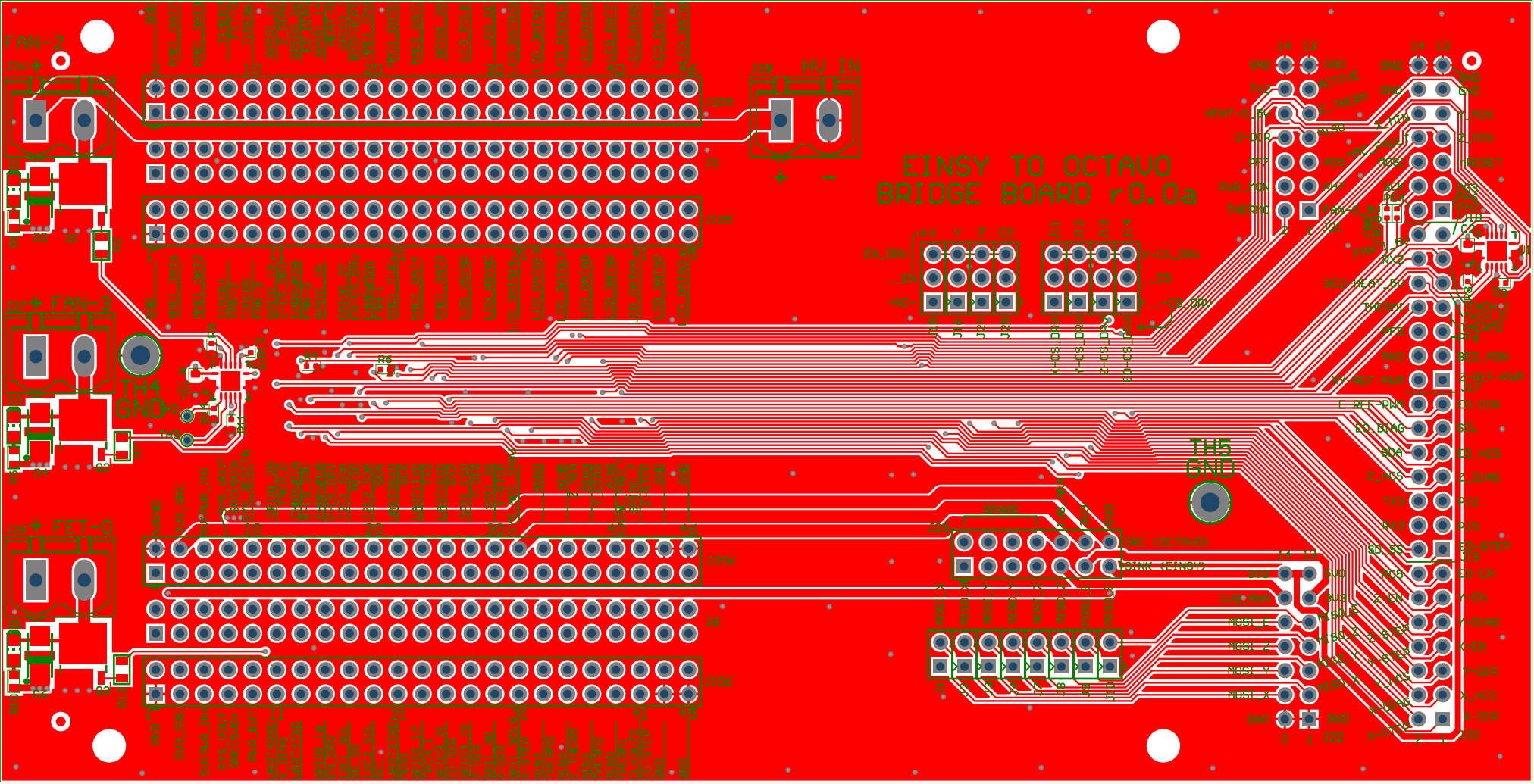

J106
J6
J206
J105
J5
J205
HDR
GND
SYS_VDD1_3P3V_SRC
VDD_5V
SYS_VOUT_SRC
PWR_BUT
X_DIAG
open
EN_DRV
SD_SS
SCL
MOSI
TACH_1
E0-DIR
Z-DIR
X-DIR
X-STEP
THERM0
Z_THERM
THERM2
THERM1
E0-STEP
TACH_0
X-CS_DRV
Y-CS_DRV
MISO
SDA
SCK
TX2
RX2
Y-DIR
Y-STEP
SYS_ADC_1P8V_SRC
AGND
Z_MIN
Y_DIAG
nAC_FAULT
Z-STEP
FAN-2
FAN-3
Z-CS_DRV
FAN-0
open
E0-CS_DRV
FAN-1
FET-0
open
Z_DIAG
E0_DIAG
HEAT-0
BED-HEAT
MOSI
MOSI_X
MISO
MISO_X
MOSI_Y
MISO_Y
MOSI_Z
MISO_Z
MOSI_E
MISO_E
J1
J2
J3
J4
J7
J8
J9
J10
Daisy Chained
Paralell
Driver Chip Selects
X_nCS
X-CS_DRV
Y_nCS
Y-CS_DRV
Z_nCS
Z-CS_DRV
E0_nCS
E0-CS_DRV
J11
J12
J13
J14
Header 3x1
All TMC2130s driven by X-CS
TMC2130s have their own CS signals
J23
SYS_VOUT_SRC
SYS_VDD1_3P3V_SRC
SYS_ADC_1P8V_SRC
SYS_VOUT_SNK
SYS_VDD1_3P3V_SNK
SYS_ADC_1P8V_SNK
Driver Enables
X-EN
EN_DRV
Y-EN
Z-EN
E0-EN
J15
J16
J24
J25
Active-low
All TMC2130s driven by X-EN
TMC2130s have their own EN signals
J29
12V
GND
- Cleanup port directions
J6
J5
GND
SYS_VDD1_3P3V
VDD_5V
SYS_VOUT
PWR_BUT
UART4_RXD
UART4_TXD
GPIO1_16
I2C1_SCL
I2C2_SCL
UART2_TXD
GPIO1_17
GPIO3_21
GPIO3_19
SPI1_D0
SPI1_SCLK
AIN4
AIN6
AIN2
AIN0
CLKOUT2
SYS_VDD1_3P3V
VDD_5V
SYS_VOUT
SYS_RESETN
GPIO1_28
EHRPWM1A
EHRPWM1B
I2C1_SDA
I2C2_SDA
UART2_RXD
UART1_TXD
UART1_RXD
SPI1_CS0
SPI1_D1
SYS_ADC_1P8V
AGND
AIN5
AIN3
AIN1
GPIO0_7
MMC1_DAT6
MMC1_DAT2
TIMER4
TIMER5
GPIO1_13
EHRPWM2B
GPIO1_15
GPIO0_27
EHRPWM2A
MMC1_CLK
MMC1_DAT4
MMC1_DAT0
LCD_VSYNC
LCD_HSYNC
LCD_DATA14
LCD_DATA13
LCD_DATA12
LCD_DATA8
LCD_DATA6
LCD_DATA4
LCD_DATA2
LCD_DATA0
MMC1_DAT7
MMC1_DAT3
TIMER7
TIMER6
GPIO1_12
GPIO0_26
GPIO1_14
GPIO2_1
MMC1_CMD
MMC1_DAT5
MMC1_DAT1
GPIO1_29
LCD_PCLK
LCD_DE
LCD_DATA15
LCD_DATA11
LCD_DATA10
LCD_DATA9
LCD_DATA7
LCD_DATA5
LCD_DATA3
LCD_DATA1
●: 5V logic driver required
U1B
U1C
U1D
U1A
U2D
U2B
U2C
U2A
HEAT-0
R3
100K
FAN-0
R4
100K
FAN-1
R6
100K
BED-HEAT
R8
100K
FAN-2
R9
100K
FAN-3
R11
100K
FET-0
R13
100K
TH2
R14
100K
TH3
TX2
HEAT-0_5V
Z-DIR
PF7
PWR_MON
THERM0
ACTIVE
Z_THERM
MISO
PD5
PH7
FAN-0_5V
J21
FB8
FB18
120R
MOSI
SCK
PG4
X_MIN
nAC_FAULT
Y_MIN
Z_MIN
nRESET
PG3
PH6
J18
FAN-1_5V
RX2
BED-HEAT_5V
THERM1
PF5
PK0
XY-REF-PWM
PH2
TACH_1
TACH_0
THERM2
PF6
BED_MON
Z-REF-PWM
J17
E-REF-PWM
E0_DIAG
SDA
Z_nCS
TX3
RX3
SD_SS
E0-DIR
SCL
E0_nCS
Z_DIAG
PJ2
PJ5
E0-STEP
J19
PC5
Z-EN
Z-STEP
Y-STEP
Y_nCS
X_DIAG
X-STEP
E0-EN
Y-EN
Y_DIAG
X-EN
Y-DIR
X_nCS
X-DIR
J20
FAN-2_5V
FAN-3_5V
FET-0_5V
SYS_VOUT = 5V0
J22
MOSI_E
MOSI_Z
MOSI_Y
MOSI_X
MISO_E
MISO_Z
MISO_Y
MISO_X
VCC
PAD
GND
U1E
U2E
MNTA
MNTB
C2
100nF
C1
100nF
SYS_VOUT_SNK
R1
1.8K
D1
Red
D2
SK310A-TP
J26
R2
22R
Q1
PSMN1R8-40YLC
R5
1.8K
D3
Red
D4
SK310A-TP
J27
R7
22R
Q2
PSMN1R8-40YLC
R10
1.8K
D5
Red
D6
SK310A-TP
J28
R12
22R
Q3
PSMN1R8-40YLC
Tab
GND Testpoints
TH4
TH5
Mounting Holes
H1
H2
H3
H4
Fiducials
FD1
FD2
FD3
Notes:
- Einsy VddIO needs to be modified for 3v3 source.
- Einsy Thermistors need to be modified for 1v8 operation.
Project: Octavo Jumper Bridge
Title:
Drawn by: AWS
Sheet: 1 of 1
UltiMachine






EINSY TO OCTAVO
BRIDGE BOARD r0.0a
FAN-2
FAN-3
FET-0
HV IN
TH4
GND
TH5
GND
J205
J105
J206
J106
J29
J26
J27
J28
J9
J6
J20
J22
J24
SPARE
SRC (OCTAVO)
SINK (EINSY)